Optimization of Tracking Performance of CMOS Monolithic Active Pixel Sensors

W. Dulinski, A. Besson, G. Claus, C. Colledani, G. Deptuch, M. Deveaux, G. Gaycken, D. Grandjean, A. Himmi, C. Hu, et al.

Optimization of Tracking Performance of CMOS Monolithic Active Pixel Sensors

Wojciech Dulinski, Auguste Besson, Gilles Claus, Claude Colledani, Grzegorz Deptuch, Michael Deveaux, Goetz Gaycken, Damien Grandjean, Abdelkader Himmi, Christine Hu, Kimmo Jaaskeleinen, Michal Szelezniak, Isabelle Valin, and Marc Winter

***Abstract*—CMOS Monolithic Active Pixel Sensors (MAPS) provide an attractive solution for high precision tracking of minimum ionizing particles. In these devices, a thin, moderately doped, undepleted silicon layer is used as the active detector volume with the readout electronics implemented on top of it. Recently, a new MAPS prototype was fabricated using the AMS 0.35 μm OPTO process, featuring a thick epitaxial layer. A systematic study of tracking performance of that prototype using high-energy particle beam is presented in this work. Noise performance, signal amplitude from minimum ionizing particles, detection efficiency, spurious hit suppression and spatial resolution are shown as a function of the readout pitch and the charge collecting diode size. A test array with a novel readout circuitry was also fabricated and tested. Each pixel circuit consists of a front-end voltage amplifier, capacitively coupled to the charge collecting diode, followed by two analog memory cells. This architecture implements an on-pixel correlated double sampling method, allowing for optimization of integration independently of full frame readout time and strongly reduces the pixel-to-pixel output signal dispersion. First measurements using this structure are also presented.**

***Index Terms*—CMOS, monolithic, pixel, tracking.**

I. Introduction

A MONOLITHIC Active Pixel Sensor (MAPS) integrates, on the same substrate, the detector element with the processing electronics. Such devices may now be fabricated using standard CMOS processes available through many commercial microelectronics companies. The idea of using MAPS for the detection of ionizing radiation, in particular for high-energy charged particle tracking, has been proposed by the IReS-LEPSI team in the beginning of 1999. The ability of the monolithic CMOS sensors to provide charged particle tracking has been demonstrated on a series of MIMOSA (standing for Minimum Ionizing MOS Active pixel sensor) chip prototypes [1]–[3]. The key element of this design is the use of an N-Well/P-Substrate diode to collect, through thermal diffusion, the charge generated by an impinging particle in the thin, undepleted silicon layer underneath the readout electronics. This solution allows 100% sensitive area (fill factor), as required in tracking applications [4]. It has been verified that both epitaxial and uniform high resistivity ($\sim$10Ω cm) substrates may be used for device fabrication [5]. The observed excellent tracking performance makes CMOS MAPS an interesting candidate for vertex detectors in future Particle Physics experiments and for ionizing radiation imaging in different applications, for example very promising application in Transmission Electron Microscopy (20 keV – 1 MeV electron energy range). Fig. 1 depicts a MAPS based option for the microvertex detector proposed for the STAR experiment upgrade in 2008 [6]. STAR is one of experiments using Relativistic Heavy Ion Collider (RHIC) facility at Brookhaven National Laboratory (Brookhaven, NY, USA).

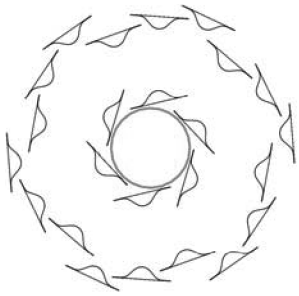

Fig. 1. Possible implementation of the STAR microvertex detector upgrade based on monolithic CMOS pixel sensors. Two layers of MAPS in cylindrical geometry around the beam pipe (shown in the center) are considered.

The proposed microvertex upgrade detector consists of two pixel sensor layers around the interaction point at the radius of 1.5 cm and 4.5 cm, respectively. It will be constructed out of 24 ladders (6 in inner and 18 in outer layer), each having a sensitive area of 2×20 cm^2. Ten individual, electrically and mechanically separate, CMOS monolithic pixel sensor arrays (2×2 cm^2) are assembled on a light support to form a ladder. All cabling is done from one side, in order to ease mechanical insertion. Power consuming electronics (long cable drivers, digital transceivers) is located at the extremity of each ladder. The pixel readout pitch of 30 μm has been chosen, to provide a spatial resolution of

Manuscript received November 15, 2004; revised March 13, 2006.

W. Dulinski, G. Claus, C. Colledani, and M. Szelezniak are with Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux (LEPSI), BP 20, 67037 Strasbourg Cedex02, France (e-mail: dulinski@lepsi.in2p3.fr, claus@lepsi.in2p3.fr, colledan@lepsi.in2p3.fr, deptuch@lepsi.in2p3.fr, szelezni@lepsi.in2p3.fr).

A. Besson, G. Gaycken, D. Grandjean, A. Himmi, C. Hu, K. Jaaskeleinen, I. Valin, and M. Winter are with Institut de Recherches Subatomiques (IReS), BP 20, 67037 Strasbourg Cedex02, France (e-mail: August.Besson@ires.in2p3.fr; Goetz.Gaycken@ires.in2p3.fr; Damien.Grandjean@ires.in2p3.fr; Abdelkader.Himmi@ires.in2p3.fr; Christine.Chu@ires.in2p3.fr; Isabelle.Valin@ires.in2p3.fr; Marc.Winter@ires.in2p3.fr).

G. Deptuch is with Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux (LEPSI), BP 20, 67037 Strasbourg Cedex02, France, on leave from UST-AGH, Al. Mickiewicza 30, 30-059 Krakow, Poland (e-mail: deptuch@lepsi.in2p3.fr).

M. Deveaux is with Institut de Recherches Subatomiques (IReS), BP 20, 67037 Strasbourg Cedex02, France and also with GSI, 64291 Darmstadt, Germany (e-mail: Michael.Deveaux@ires.in2p3.fr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2006.889167

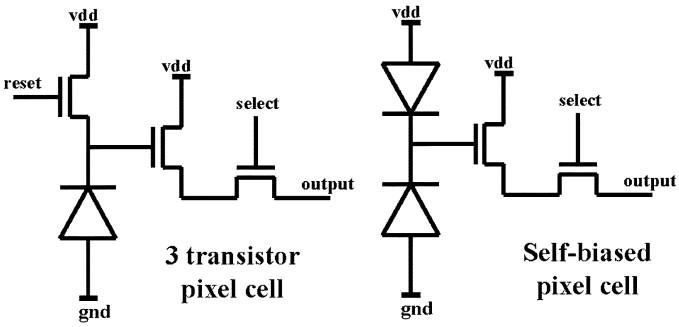

Fig. 2. Two versions of on-pixel readout architecture used for the Mimosa9 prototype.

below 10 μm. The total number of pixel elements in the system is close to 100 million. The entire detector must be read out in less than 4 ms. In the baseline readout architecture proposed for the STAR microvertex upgrade (continuous serial readout of all pixels, followed by digital Correlated Double Sampling (CDS) processing), the readout time is equal to the signal integration time. The detector will operate at room temperature with cooling based on flowing ambient air only. Estimated electrical power dissipation is of the order of 0.2 μW/pixel and is dominated by the analog output line drivers. The expected irradiation dose in the innermost layer is of order 10^{11} π/cm^2/year (up to 10 krad/year), depending on the experiment luminosity upgrade schedule.

Two different epitaxial CMOS processes are considered as promising candidates for the STAR microvertex upgrade sensor production. In this contribution, we present results measured with a prototype fabricated in AMS 0.35 μm OPTO process.

II. MIMOSA9 Prototype Device Design

The AMS-0.35 μm OPTO process has been chosen for several reasons. It is an advanced mixed-signal CMOS process, providing four metal layers, two polysilicon layers, high-resistivity polysilicon and two types of transistor gates (3.3 V and 5 V). The N-Well diodes are optimized for a low dark current at room temperature. The feature of a special interest is epitaxial layer having more than 10 μm thickness. Such a thick epitaxial layer should provide a comfortable charge signal from passing minimum ionizing particles (at least 50 to 100 electrons for the smallest MIP signal seen by the seed pixel in a few pixel cluster). The process is available through multi-project submission runs at Austria Micro Systems.

The Mimosa9 prototype contains four arrays of pixels with a pitch varying from 20 μm to 40 μm. A simple pixel read out architecture is used (Fig. 2). It consists of a 3-transistor pixel cell (one reference array for a direct dark current measurements) or a self-biased 2-transistor cell (three arrays dedicated for particle tracking). Charge collecting diodes of different sizes are used for each readout pitch, in order to optimize the signal-to-noise ratio and spatial resolution (Fig. 3).

The signal information from each pixel is serialized by a circuit (one per array), which was designed for a 40 MHz readout clock frequency and the noise figures should not be degraded at that maximum speed. However, all the results presented in this work were obtained with a 2.5 MHz clock, in order to have the full frame readout frequency comparable to that planned for STAR, with all problems connected to this (increase of the dark current shot noise contribution, due to the long integration time and room temperature operation). The chosen readout frequency during this tests provides a full frame readout time of 1.6 ms and 400 μs respectively for 64×64 pixel array (20 μm pitch) and for 32×32 pixel array (30 μm and 40 μm pitch). In this architecture, the frame readout time is equal to the signal integration window. Two consecutive frames were read out: one frame before and one frame after each trigger. A data analysis based on the correlated double sampling (CDS) method was used for hit reconstruction. Each prototype device was electrically tested in the laboratory and the gain calibrated using 5.9 keV X-rays from a ^{55}Fe source, prior to the high-energy particles tracking tests.

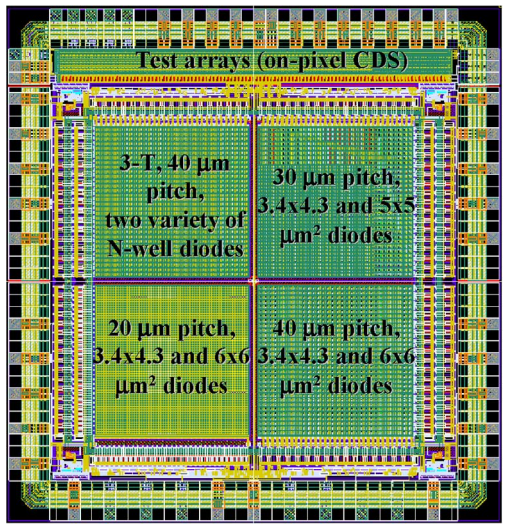

Fig. 3. Layout of Mimosa9: the overall dimension of this prototype is 4.1 $\times$ 4.3 mm^2.

The reference array for direct dark current measurements (3 transistors scheme) contain two varieties of charge collecting diodes. The first one is a very standard N-Well diode, having a dimension of 6×6 μm ^{2}. According to the process requirements, around the diode periphery there is a thick oxide structure (LOCOS), directly on top of the p-n junction. The second diode type has the N-well dimension of 3.4×3.4 μm ^{2}. In order to avoid thick oxide on top of the junction, the N-well periphery is in contact with an n+ diffusion, followed by an nMOS transistor gate at ground potential all around. This structure, compatible with the process design rules, has been designed to be more radiation tolerant in terms of a dark current increase. The irradiation tests results of both structures will be discussed later in this work.

III. Tracking Test Results

Tracking tests were performed using a 120 GeV/c pion beam from the SPS accelerator at CERN, Geneva, Switzerland. A high precision beam telescope based on silicon microstrip detectors was used to measure each particle track parameters [7]. After off-line alignment of a pixel device with the reference tracking system, tracks within the sensitive area of the pixel device were used to measure various parameters, such as minimum ionizing

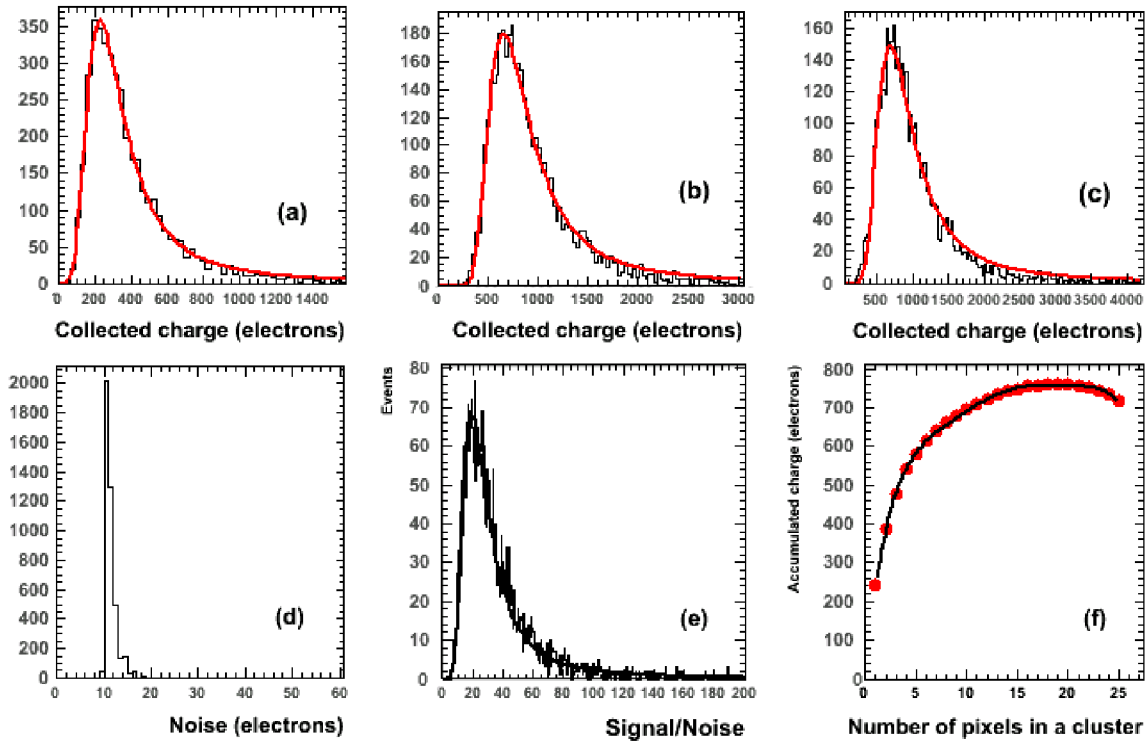

Fig. 4. Run summary page for 30-μm pitch, 5×5 μm^2 diodes array measured at 20°C. Upper plots: the distribution of charge collected on the central (seed) pixel of a cluster (a), the charge collected on the 3×3 pixel cluster (b) and on the 5×5 pixels cluster (c) around the seed one. Lower plots: the distribution of individual pixel noise (d), signal-to-noise ratio for the seed pixel (e) and the total collected charge versus the number of pixels included in the cluster (f).

particles signal-to-noise ratio, detection efficiency and spatial resolution.

Fig. 4 is a typical run summary page. The upper plots show the distribution of charge collected on the central (seed) pixel of a cluster (left), the charge collected on the 3×3 pixel cluster (middle) and on the 5×5 pixels cluster (right) around the seed one. The most probable value (MPV) of the Landau distribution is calculated in each case. The measured individual pixel noise (ENC) and signal-to-noise ratio for the seed pixel are shown below. The last plot (bottom, right) shows the total collected charge as a function of the number of pixels included in the cluster. As one may observe, the most of the charge is collected on about 10 pixels. The further rise and fall of the signal is explained by a pixel-ordering algorithm, which selects first the positive and then the negative noise fluctuation. The measured detection efficiency in this example was 99.8%, for S/N ratio seed pixel cuts of six.

Fig. 5 shows the measured equivalent noise charge (ENC) for all self-biased structures, versus charge collecting diode area for different temperatures (0, 20 and 40°C). The lowest noise of 9 electrons corresponds to minimum diode size and low temperature. Increased capacitance of larger diodes and increase of a dark current at higher temperatures are responsible for the degradation of the noise performance.

Fig. 6 shows the MIP signal charge, corresponding to the peak (most probable value) of the Landau distribution measured at the central (seed) pixel of a cluster. The signal is smaller for smaller collecting diodes and drops with an increase of the readout pitch. Although visible, the temperature dependence of the signal amplitude is very limited.

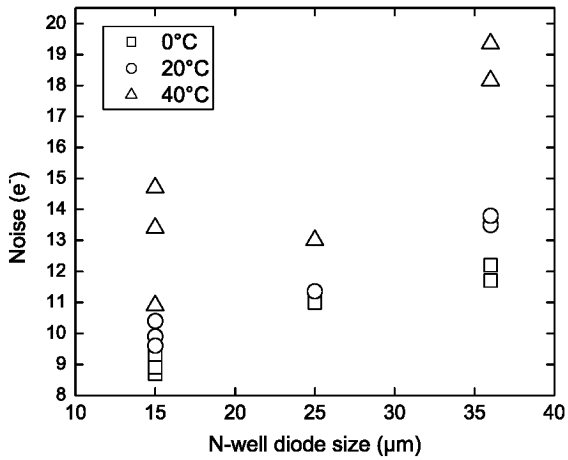

Fig. 5. Equivalent Noise Charge as a function of a collecting N-well diode surface and an operation temperature.

The relatively high S/N ratio measured on all structures allows for an efficient spurious (noise) hit rejection, still keeping the detection efficiency close to 100%. The algorithm chosen for hit selection also takes into account the large cluster size observed in MAPS due to its specific charge collection mechanism. To accept a hit, the signal-to-noise ratio of the seed pixel should be higher than n (typical 4 to 6) and the signal-to-noise ratio of eight surrounding neighbor pixels should be higher than k (typical 2 to 4). The total signal (noise) of neighbor pixels is calculated as a sum of signals (square root of quadratic sum of noise) of individual pixels forming the group. For the value of $\mathrm{n} = 6$ and $\mathrm{k} = 2$, the noise hit rejection should be higher

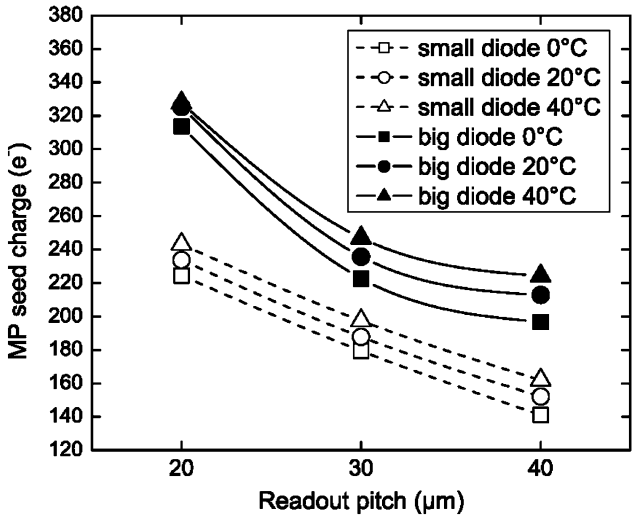

Fig. 6. Seed pixel charge (Landau peak) versus the readout pitch and the temperature.

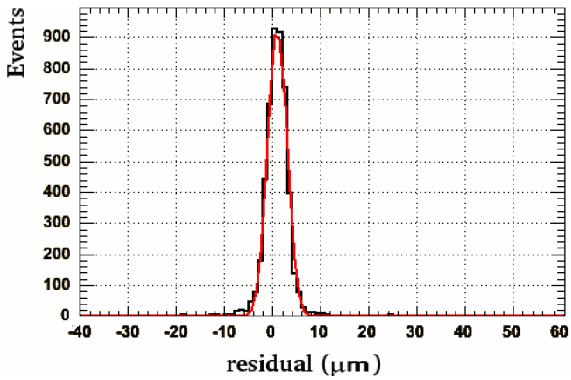

Fig. 7. Residual distribution measured with a 20 μm pitch, small diodes array at 20°C temperature. The spatial resolution of the device under test is calculated from this, accounting for the track error from the beam telescope.

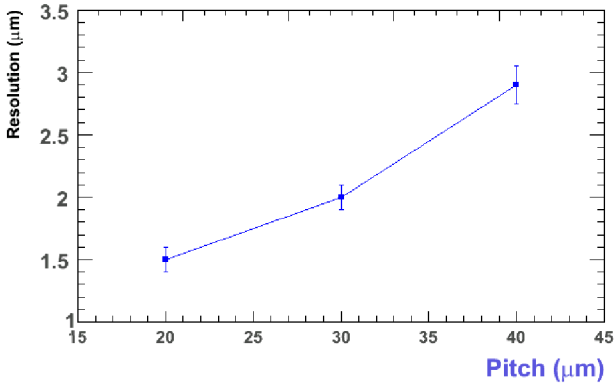

Fig. 8. Spatial resolution for minimum ionizing particles as a function of pixel pitch, measured with Mimosa9 prototype.

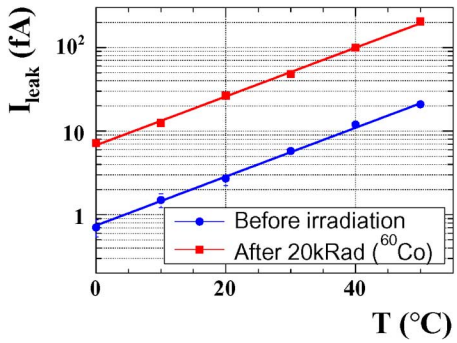

Fig. 9. Measured dark current of a 6 × 6 μm standard N-well diode as a function of temperature, before and after irradiation.

than 10^6, assuming a Gaussian noise distribution. In the case of Mimosa9 prototype, applying cuts corresponding to $\mathrm{n} = 6$ and $\mathrm{k} = 4$ ($\mathrm{n} = 5$ and $\mathrm{k} = 2$ for the 40 μm pitch array) results in a measured MIP detection efficiency of more than 99.5%, without any correction for non-working (or excessively noisy) pixels.

Fig. 7 shows an example of residual distribution and Fig. 8 the spatial resolution of the Mimosa9 different arrays, as a function of their pixel pitch. Due to the high S/N ratio, the position measurement of a particle track is greatly improved using the charge distribution in the cluster. For 20-μm pitch, the resolution reaches 1.5 μm and is still between 5 and 6 μm for a large 40-μm pitch. In all cases, this value is much better than the one required by the STAR microvertex detector upgrade.

The total charge collected from the epitaxial layer in the case of Mimosa9, taking into account estimated charge losses (device simulation and experience with previous prototypes), indicates the epitaxial layer thickness in the AMS 0.35 μm OPTO process to be slightly above 10 μm.

IV. Dark Current Before and After Co^{60} Irradiation

The degradation of the performance of the prototype MIMOSA9 chip after absorption of radiation dose was studied using γ rays from Co^{60} source. Fig. 9 shows the dark current measured for the standard N-well diode before and after irradiation, as a function of temperature. An order of magnitude increase of the dark current was observed after 20 krad of the absorbed dose. This may be a critical factor for STAR's microvertex detector upgrade. The shot noise contribution (corresponding to the dark current) to the total ENC before irradiation would be 12 electrons for the STAR operating condition, i.e., temperature of 30°C and 4 ms signal integration time. This is still acceptable, because the total noise would be less than 20 electrons in this condition. However, after irradiation the shot noise contribution would rise to 39 electrons according to the dark current measurements and will affect the detection efficiency.

In order to allow for a safe STAR microvertex detector operation, two approaches for the sensor modification may be considered. In the first approach, a different layout of the charge collecting diode is proposed. One promising candidate is the diode with the layout shown below (Fig. 10). In order to avoid a radiation sensitive thick oxide on top of the junction, the N-well is covered by an area of n+ diffusion on top, extending around the N-well area. This is followed by a circular nMOS transistor gate (polysilicon on top of a thin oxide) at ground potential. The layout is fully compatible with the process design rules. According to measurements, the dark current after 20 krad dose absorption is only 50% higher in this case. The drawback of this solution is much higher junction capacitance (factor of two

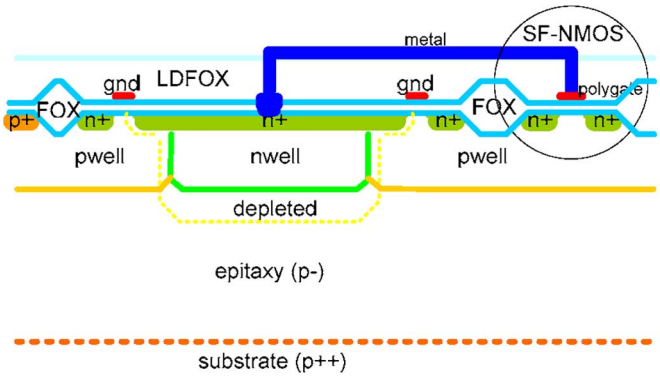

Fig. 10. Cross-section of an N-well diode having no thick oxide on top of the p-n junction.

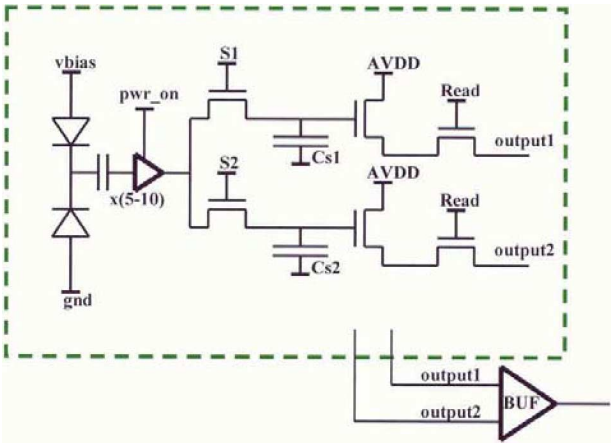

Fig. 11. Pixel electronics circuitry implementing on-device CDS processing through storage of two consecutive readout frames on the integrated analog memory cells.

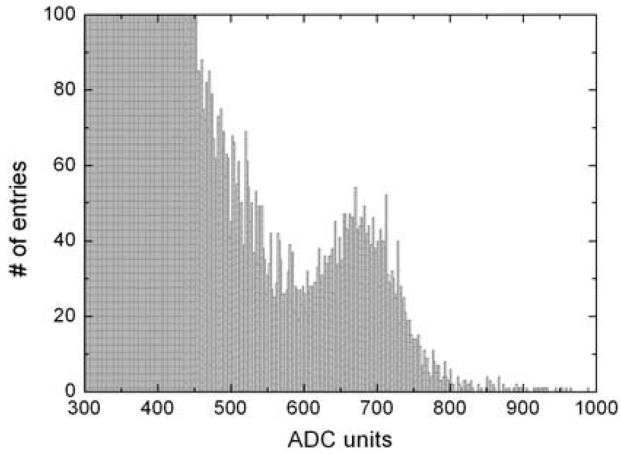

Fig. 12. Seed pixel, Fe^{55} photon spectrum) measured with a new readout structure (on-pixel information storage using two analog memory cells). The arrow shows a peak corresponding to 5.9 keV photons converted in fully depleted region close to the N-well diode junction. The position of this calibration peak, which corresponds to signal of 1640 electrons, is used for the electronics readout chain conversion factor (electronics gain) estimation. Knowing this conversion factor, an Equivalent Noise Charge (ENC) is calculated from the single pixel signal amplitude variance (RMS). Please note that the width of the calibration peak is substantially wider than expected for a typical, 20 electrons ENC. This may be explained by the gain dispersion between pixels (not corrected for) and by the fact that the depleted layer around diodes is very thin (less than 2 μm), so some charge losses are anticipated.

with respect to the standard one), but further optimization of the present layout may be still considered.

The other approach to limit degradation of the pixel device performance after irradiation is based on the use of new pixel architecture, as discussed in the next paragraph. In this approach, the signal integration time may be reduced by an order of magnitude, resulting in strong reduction of the shot noise contribution.

V. On-Pixel CDS Processing Using Analog Memory Cells

A test structure with a novel readout circuitry was proposed and included in the design of Mimosa9 prototype. It consists of a front-end voltage amplifier, capacitively coupled to the charge collecting diode and followed by two analog memory cells (Fig. 11). The information from two successive frames is continuously stored in the analog memory during the acquisition phase. After trigger arrival, the readout phase is initiated. During this phase, each pixel is individually addressed and the signal difference stored in two memory cells is read out in one clock cycle. This architecture implements an on-pixel correlated double sampling method, allowing for optimization of integration independently of full frame readout time and strongly reduces the pixel-to-pixel output signal dispersion. Requirements for the precision of the data transmission and digitization are released in this solution, which is of importance for higher readout clock frequencies. Several versions of this amplifier are tested in Mimosa9. The basic one allows a voltage gain of five by applying a simple cascode structure. An integrated capacitive coupling between the charge-collecting element and the amplifier is essential for an independent and optimal biasing (through V_{bias} and V_{inp}) of the N_well diode and of the cascode. The amplifier version with a higher gain (x10) uses thicker gate oxide transistors available in that fabrication process. The layout of this simple circuit fits easily a 30 μm pixel pitch, with storage capacitors values allowing precise signal sampling.

Preliminary experimental results obtained with the new structures are promising, even if the measured voltage gains were smaller than anticipated. This discrepancy is still to be understood. The storage capacitors show a comfortably long signal discharge time of several seconds and a small switching generated noise. After device calibration using Fe^{55} 5.9 keV photons (Fig. 12), the total ENC was measured and found to be below 20 electrons. This is close to the final requirements and may be still improved by a careful design optimization.

VI. Conclusion

A monolithic active pixel sensor for charged particle tracking has been fabricated using modern CMOS process providing thick epitaxial layer. Excellent minimum ionizing particle tracking performance has been measured with this device, for a readout pitch varying from 20 μm to 40 μm. Using the measured MIP signal, the equivalent epitaxial layer thickness was found to be slightly above 10 μm. The observed N-well diode dark current before irradiation does not limit a comfortable S/N ratio for room temperature and long integration time operation.

Irradiation using Co^{60} photons induce a ten-fold increase of the dark current, after a modest (20 krad) dose absorption. This may prevent the use of a long integration time at room temperature in the STAR experiment environment. A new proposed layout of the N-well diode with only a thin oxide contacting the junction shows a strongly improved immunity for the irradiation damage. In order to decouple the signal integration time from the readout cycle, a new pixel architecture is proposed. In this approach, two consecutive readout frames are continuously stored using two analog memory cells integrated in each pixel, allowing on-device implementation of CDS processing. The first tests results with this structure are promising.

REFERENCES

[1] R. Turchetta, "A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology," *Nucl. Instrum. Methods Phys. Res. A*, vol. A458, pp. 677–689, 2001.

[2] G. Deptuch, J. D. Berst, G. Claus, C. Colledani, W. Dulinski, U. Goerlach, Y. Gornushkin, Y. Hu, D. Husson, G. Orazi, and R. Turchetta, "Design and testing of monolithic active pixel sensors for charged particle tracking," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 2, p. 601, Apr. 2002.

[3] G. Deptuch, G. Claus, C. Colledani, M. Deveaux, A. Gay, W. Dulinski, Y. Gornushkin, C. Hu-Guo, and M. Winter, "Development of monolithic active pixel sensors for charged particle tracking," *Nucl. Instrum. Methods Phys. Res. A*, vol. A511, pp. 240–249, 2003.

[4] B. Dierickx, G. Meynants, and D. Scheffer, "Near 100% fill factor CMOS active pixel," in *Proc. IEEE CDD&AIS Workshop*, Brugge, Belgium, Jun. 5–7, 1997.

[5] W. Dulinski, J.-D. Berst, A. Besson, G. Claus, C. Colledani, G. Deptuch, M. Deveaux, A. Gay, D. Grandjean, Y. Gornushkin, A. Himmi, C. Hu, J.-L. Riester, I. Valin, and M. Winter, "CMOS monolithic active pixel sensors for minimum ionizing particle tracking using non-epitaxial silicon substrate," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 4, p. 1613, Aug. 2004.

[6] H. Wieman, STAR Collaboration at RHIC, BNL. Private comunication. Berkeley, CA, Lawrence Berkeley National Lab (HHWieman@lbl.gov).

[7] C. Colledani, W. Dulinski, R. Turchetta, F. Djama, A. Rudge, and P. Weilhammer, "Submicron precision beam telescope," *Nucl. Instrum. Methods Phys. Res. A*, vol. A372, pp. 379–384, 2004.