# Temperature sensitivity of the AMS RICH front end chip

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## 1. Introduction

A Ring Imaging Cherenkov (RICH) counter for the AMS experiment [1] is under development. A first integrated circuit was designed in 1998 to process the signals from the RICH PMTs [2]. A complete study prototype, including trigger and tracker detectors as well as DAQ system, it was implemented in [3]. This prototype was tested in laboratory with cosmic rays and a beam test was carried out at GSI Darmstadt in 1999 with a light ion beam [4]. In this preliminary design, single anode PMTs were used, and the front end chip was processing groups of 3 PMTs. In order to improve the spatial resolution of the detector (by reducing the pixel size), 16-anode PMTs (R7600-M16 model from Hamamatsu [5]) were chosen to equip the finaly count and the second generation prototype. A new 16 channel chip in CMOS technology (*AMS*) was submitted in 2000 [6]. This chip used the Austria Mikro Systeme 0.6 µm technology, it was successfully tested in the laboratory and an engineering run was ordered in 2001. The second generation RICH prototype currently under test at the ISN-Grenoble is equipped with these chips.
The aim of the present study was to quantify the effect of the temperature on the electronic response of the chip, especially about a possible drift of the pedestal amplitude with temperature. The tests have been conducted on the latest of the chip version, i.e. without external current converter.

## 2. Measurement procedure

The chip has been tested first in the dedicated test bench of the chip[7], and then with the associated electronics and PMT on the PMT test bench. In order to perform these measurements, a temperature monitored chamber was used in which the cell including front-end electronics and PMT was placed. The range of temperature available with this type of chamber is from -40 °C to 180 °C.

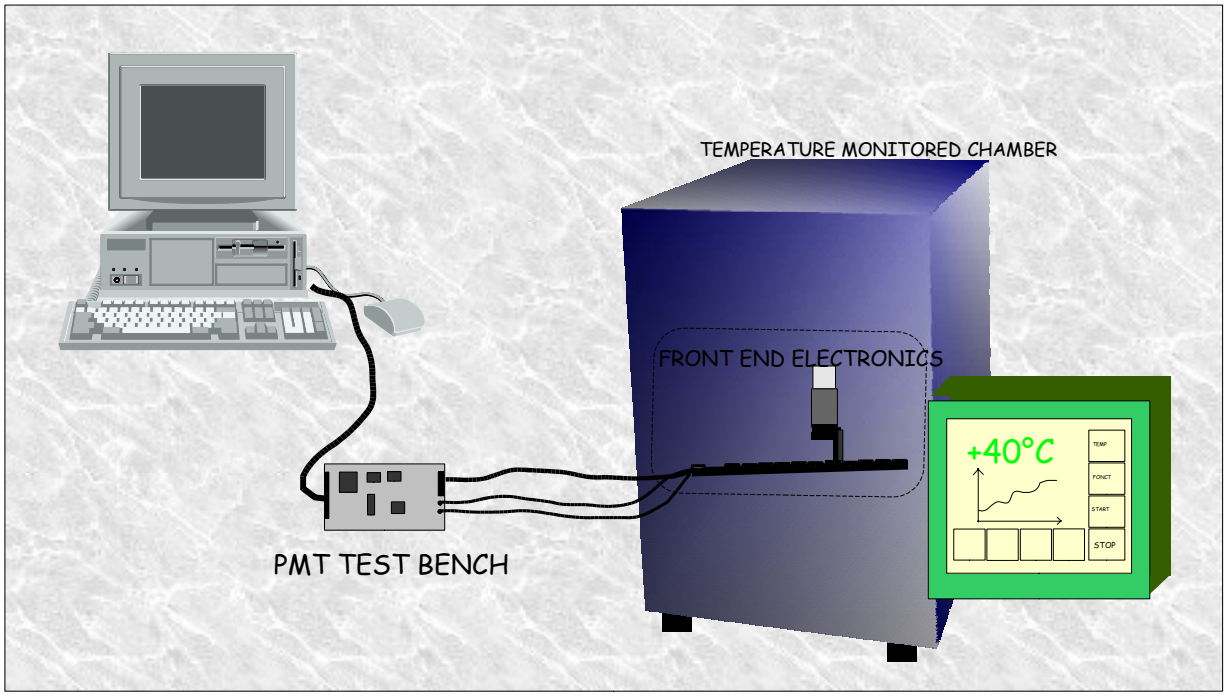


Figure 1. Temperature test bench setup

The accuracy on the value of the temperature is approximately 0.1°C after 2.5 minutes of stabilization. A stabilisation time of 15 minutes was used. The analysis of the measurements provided the pedestal evolution between -30°C and 50°C.

## 3. TEMPERATURE EFFECTS

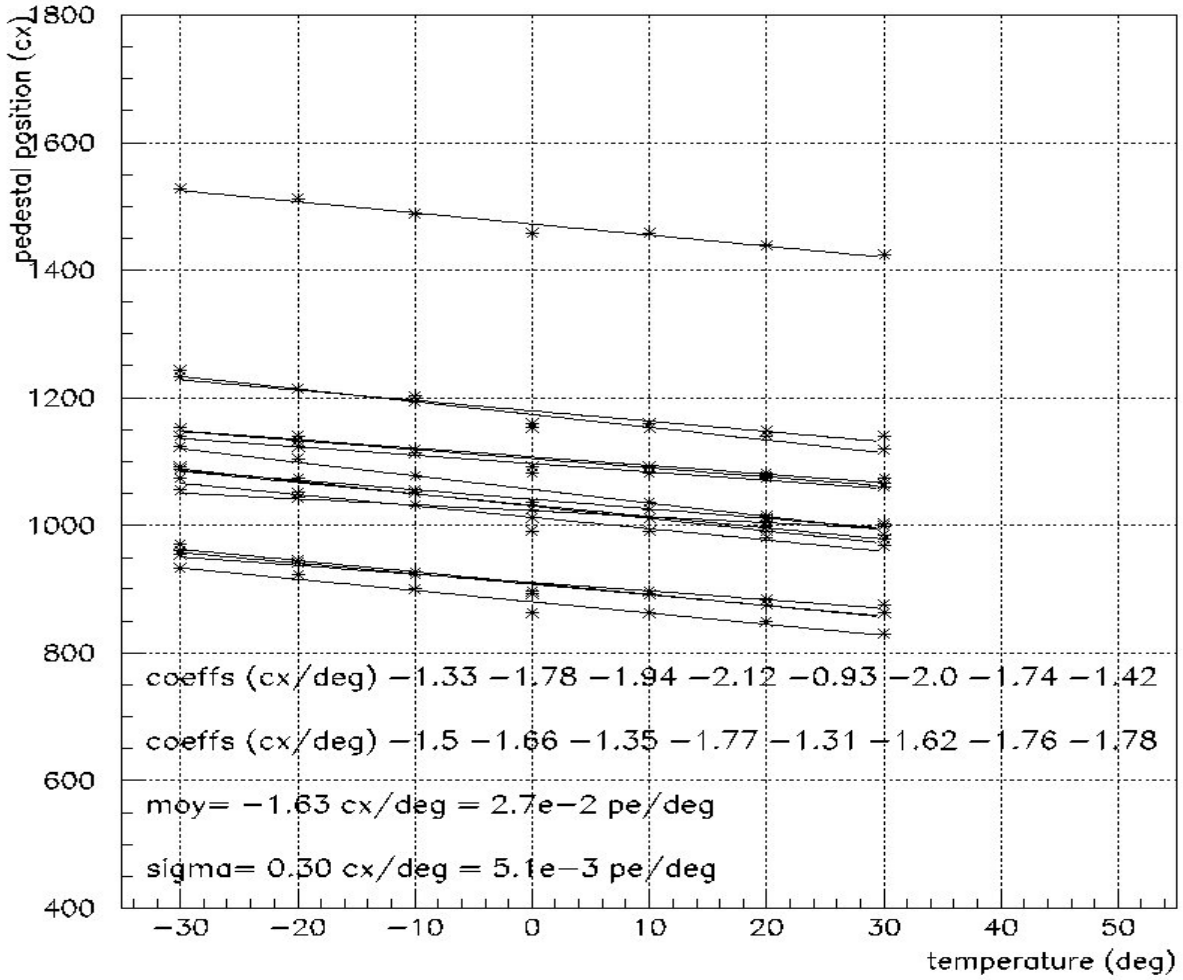


Figure 2. Temperature effects on the pedestal

Figure 2 shows that an evolution of the average pedestal of -1.63 ADCchannel per degrees in gain five was observed. Such a shift, even small, could lead to some errors in the single photo electron amplitude determination and, as a consequence, to a bad calibration of the detector. Fot this reason, a technical solution has been considered to correct the observed drift.

## 4. IMPROVEMENT AND RESULTS

. In the last version of the chip, a modification has been brought on the setting of the pedestal level. In the schematics shown on figure 3, the internal resistor 'R' provides the drift of the pedestal, an injection current employed to add a DC level to the pedestal, by means of an external resistor R1, in order to have always positive pedestal value.

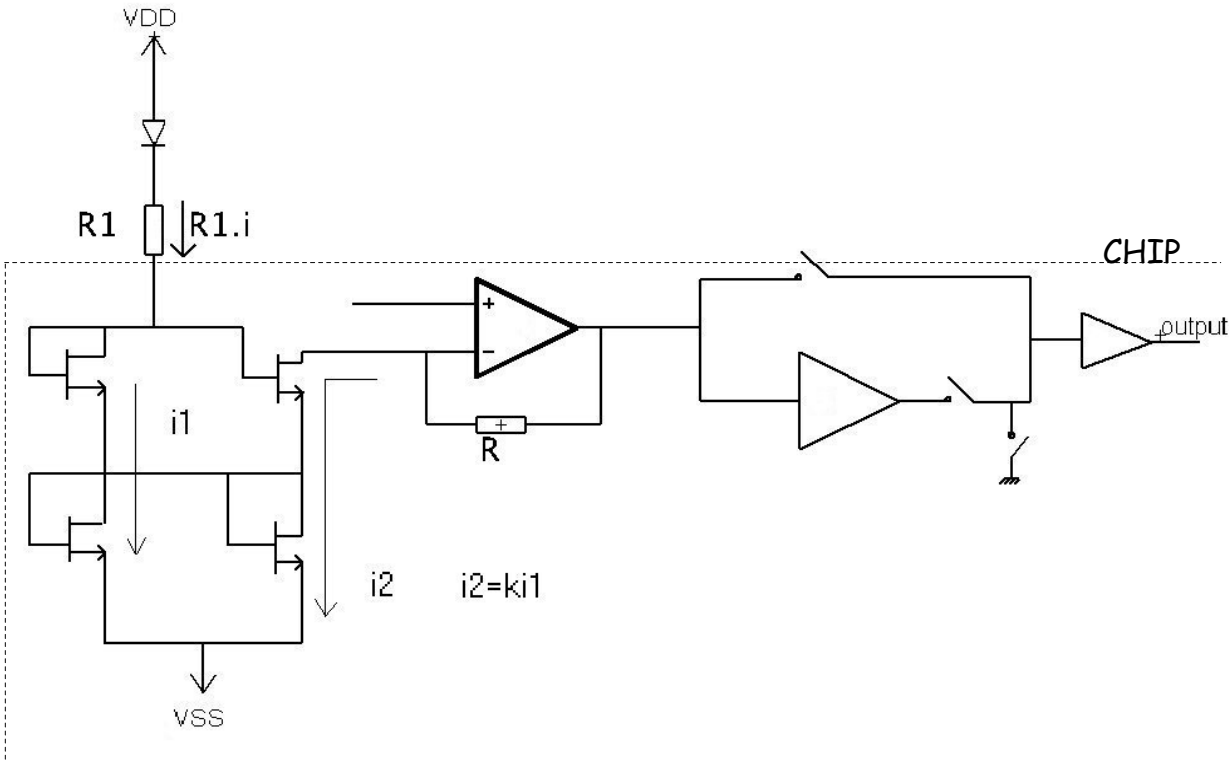


Figure 3. Pedestal Level Input Schematic

The improvement consists of using a diode, which brings the -2mV/°C sensitivity from the junction to compensate the pedestal drift. Then the current mirror composed of 4 mosfets (fig 3) is going to be proportional to the temperature, and the negative effect of temperature driven by amplifier with resistor R will be corrected.

With the same configuration for the test, a significant result has been observed. The pedestal corrected by the diode effect is brought down to 0.39 ADCchannel/°C on average (see figure_4) i.e., a factor of about 4 smaller than with the uncorrected circuit.

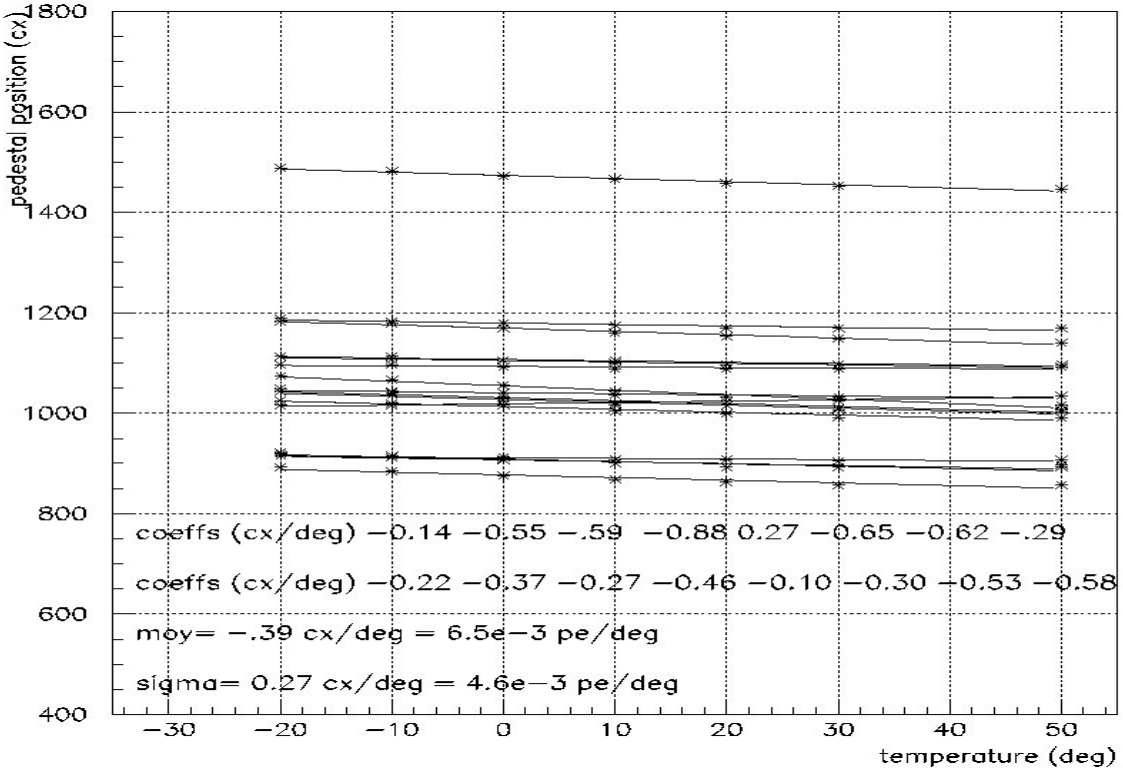


Figure 4. Effects of the correction

Once in orbit, the gradient of temperature of the detector will drift by 1 to 2 °C in 90 min. Without correcting diode, the effect of the temperature is 1 ADCchannel/°C which corresponds approximately to 2.7% of the single photo-electron amplitude, would afect the reponse of the chip. With the diode compensation, this value droops to 0.65%.

## 5. CONCLUSION

The aim of the present study was to quantify the effect of the temperature on the electronic response of the chip, specially about a possible drift of the pedestal amplitude with temperature. The tests have been carried out the latest chip version, i.e., without external current converter.

The chip has been tested with the PMT test bench associated to a temperature monitored chamber, and measurements have been perfomed between -30°C and 50°C. The observed drift due to the temperature of the average pedestal was about one channel per degree for gain five. To improve this drift, we added a diode on the pedestal level input of the chip. The diode brought a sensibility of -2mV per degree in the pedestal level input, resulting in a correction of -0.39 channel per degree on the average.

This study was necessary to quantify the effect of the temperature on the electronic response.

The use of a diode improved the sensibility of the pedestal shifting between -30°C and 50°C corresponding to 0.76% of the single photo-electron. In this way, the calibration of the detector will not be depending on the temperature.

However, the uncorrected effect was small and with minor contribution to the drift spreading, 0.78 channel over the expected range of temperature (see the grid temperature figure 5 [7]), compared to the pedestal sigma which is of the order of 4 channels, and the modification may not be necessary. So we plan to implement the correction in the microcircuit electronics front end.

## GRID TEMPERATURE

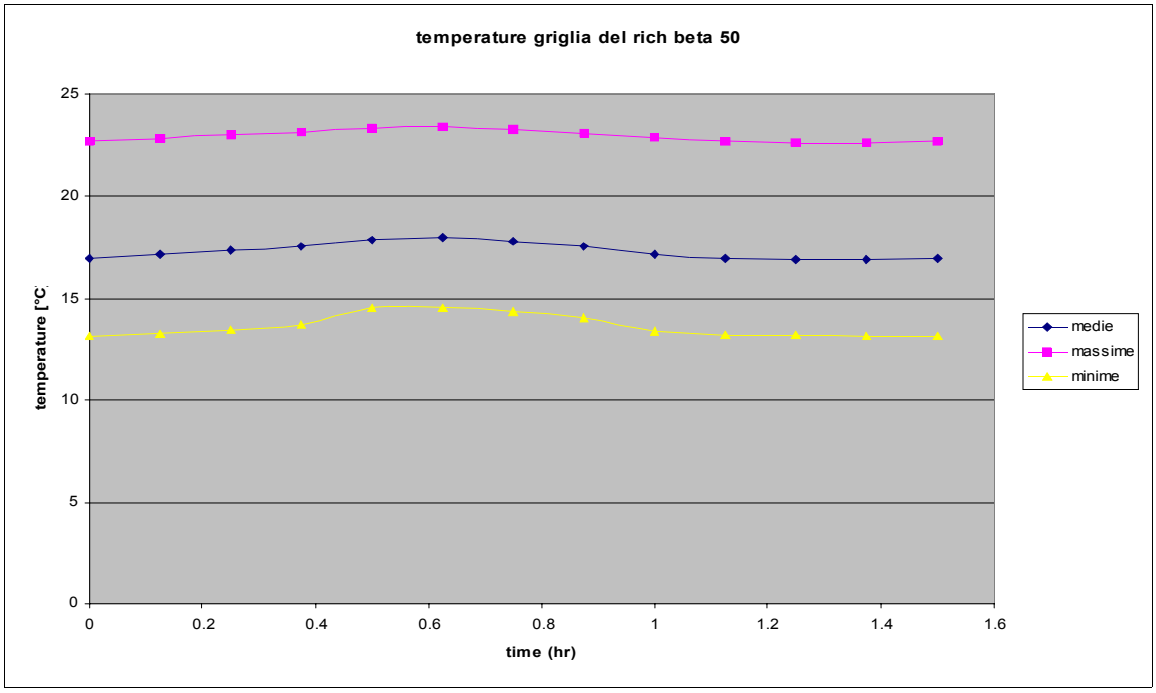


Figure 5 a. Beta 50° is the hot case

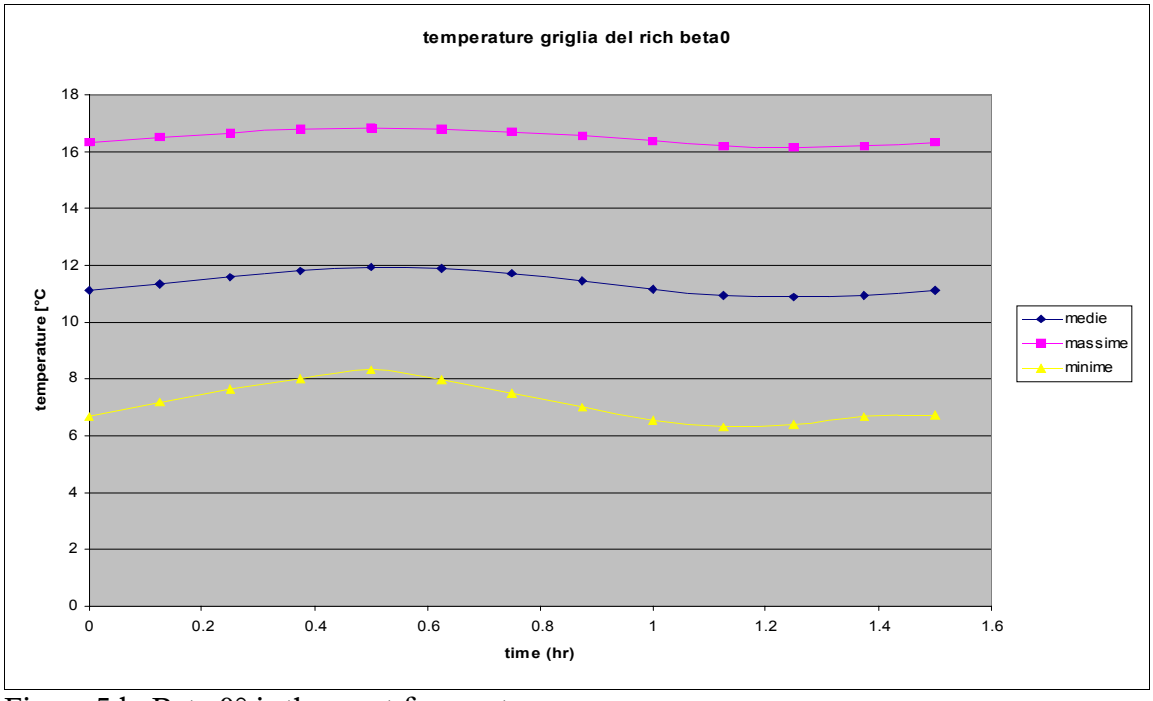


Figure 5 b. Beta 0° is the most frequent case.

## 6. REFERENCES


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[5] :More details can be found at the following address : http://www.hamamatsu.fr/

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