A selective gate for very high-rate analog pulses

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A gate for analog pulses has been developed which allows to perform a precise time-selection among a very high-rate flow of incoming signals.

1. The experimental problem

Experiment NA38 [1] has been designed to study the production of prompt muon pairs with incident ion beams. The small cross section of hadronic-muon pair production requires very high luminosities which induce, in some of the detectors, counting rates as high as 5×10^6 per second whereas the corresponding number of trigger-selected interesting events amounts only to about 200 per second. Under such severe conditions, which could be similar to those foreseen with future high-luminosity accelerators, analog signals had to be treated with special care in order to reduce the high level of piled-up events. On the other hand, the choice of a commercial, accurate, charge sensitive ADC with short conversion time (55 μs) was limited, in our case, to the module LRS 2249 A which suffers of inter-channel crosstalk when the amplitude or rate of input signals do not comply with specifications. As a consequence, the following three stage system was developed (fig. 1).

A linear filter acts as a time compressor. It was designed to reduce the pile-up effect due to the time broadening of the analog pulses in the 140 m of KX4 cable connecting the detectors to the electronics units. It is described in section 2.

A linear gate is used to reduce the pulse rate on the converters down to the few hundreds per second which are correlated with the trigger. Full details are given in section 3.

Finally, a pulse-stretcher, described in section 4, is used to match the output of the linear gate to the input specifications of the ADC.

2. The filter

The time dependence of the analog pulses given by the detectors at the end of 140 m of cable can be well described by te^{-t/τ_0}. The filter consists of two identical cascaded bridged-T networks (fig. 2). The transfer function of this filter is:

$$T(p) = \left(\frac{1+\tau_0 p}{k+\tau_0 p}\right)^2.$$

The corresponding output signal is given by te^{-kt/τ_0}, k being the time compression factor. The characteristic

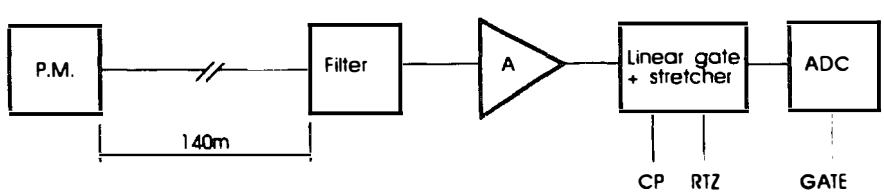


Fig. 1. Detection channel configuration.

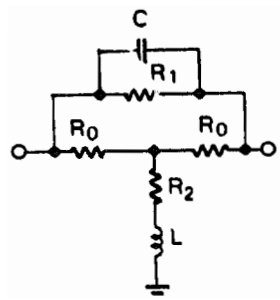


Fig. 2. Half filter cell.

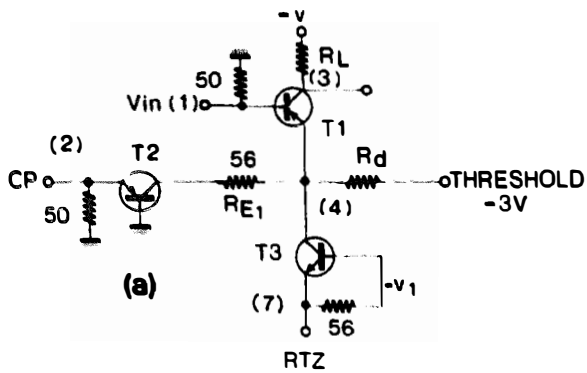
impedance is real and equal to R_0 (50 Ω). The filter components depend on the time characteristic τ_0 of the input signal and on the choice of k through the following expressions:

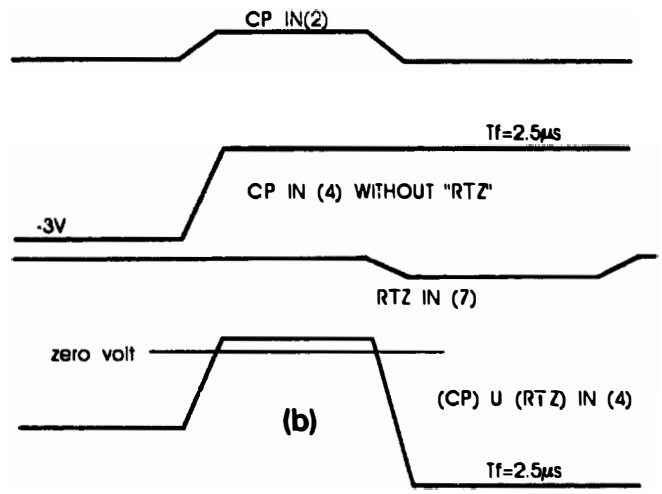
$$C = \frac{\tau_0}{R_0(k-1)},$$

$$L = CR_0^2,$$

$$R_1 = R_0(k-1),$$

$$R_2 = \frac{R_0}{(k-1)}.$$





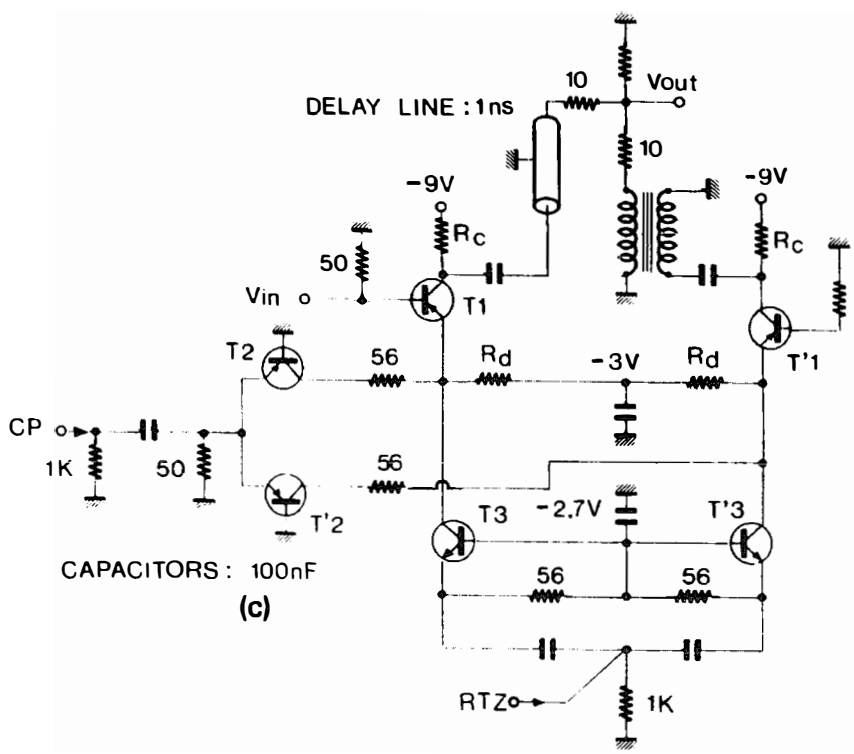


Fig. 3. (a) The gate principle. (b) Internal timing for the T1 emitter charge evacuation signal. (c) The linear gate circuit.

3. The linear gate

3.1. Principle

A schematic diagram of the gate itself is given in fig. 3a. The gate is driven by a switching transistor T2 which is off in the rest state. On a command through an external control pulse (CP), T2 saturates so that the gate transistor T1 switches to the on state and becomes a serial feedback amplifier. At the end of the CP, the carrier density near the collector junction of T2 decreases slowly ($T_1 = 2.5$ μs) due to the high value of the resistance R_d (100 kΩ). In order to avoid a resulting increase of the opening time of the gate, the charge on the emitter of T1 is rapidly drained away through a transistor T3 by a negative pulse, called RTZ, synchronized with the end of the CP (fig. 3b), so that both the rise time and the fall time of the internally generated CP are close to 0.7 ns [2]. The recovery time of this RTZ is 2.5 μs which is negligible compared to the 55 μs conversion time of the ADC.

The polarization of the transistor T2 induces a pedestal level on the collector of T1 given by $\Delta V = \Delta I_c R_L$. To avoid a significant decrease of the available dynamic range of the ADC, this pedestal is subtracted as follows. A similar and synchronized channel T'1, T'2 and T'3 provides on the collector of T'1 the same pedestal as on T1, the transistors of T1 and T'1 being matched for this purpose. The pedestal level on T'1 is inverted via a transformer and then added to the corresponding level of T1. This addition is performed on a couple of small value resistors (10 Ω) so as to preserve the bandwidth of the whole system (fig. 3c). Unmatched rise times and time dispersion of the two signals that are added can result in short-width (1.5 ns) parasitic output signals with an amplitude of a few mV and zero average-value integral charge. They are correlated with the switching times of the CP and independent of the input signal.

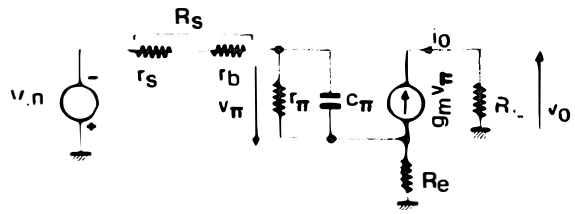


Fig. 4. Small signal equivalent circuits of T1.

3.2. Characteristics

3.2.1. Gain

The gain of the gate is a function of the gain of the circuit made of transistor T1 with its inverse feedback loop. The transconductance of this circuit is:

$$i_0/V_{in} = \frac{g}{(1+gf)}.$$

Following ref. [3] the forward transconductance is:

$$g = g_m \frac{Z}{(Z + R_s + R_e)},$$

where g_m is the transconductance of T1, $Z = r_\pi // (1/jC_\pi\omega)$ and $R_s = r_s + r_b$ (fig. 4). The two diodes of the switching transistor T2 are forward biased during the constant level CP and their low impedance is constant. The feedback f is given by $f = R_e = R_{E1} + r_{so}$ where r_{so} is the impedance of T2 and R_{E1} is equal to 56 Ω. The voltage gain is $G_v = v_0/V_{in}$ with:

$$G_v = -g_m \frac{R_L Z}{((1+g_m R_e)Z + R_s + R_e)},$$

where R_L is the load resistor. In the bandwidth where $|Z| \gg R_s + R_e$

$$G_v \sim -g_m \frac{R_L}{(1+g_m R_e)},$$

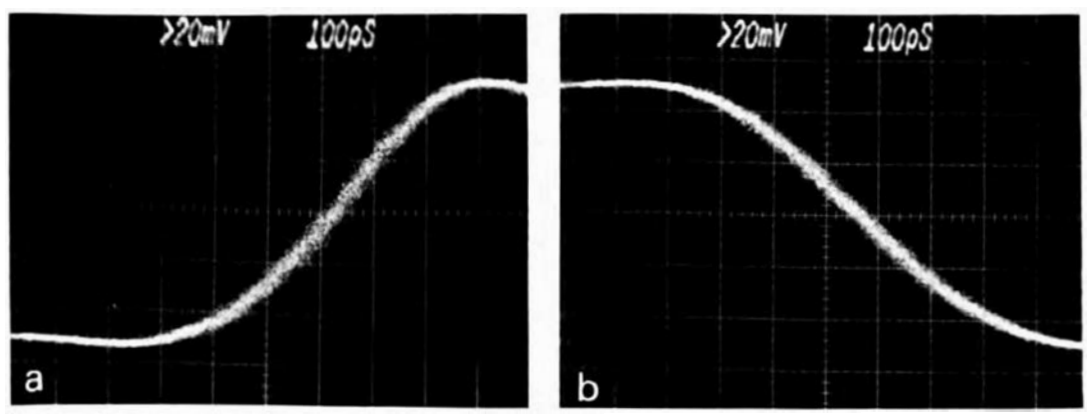


Fig. 5. Effect of the gate on a dc level.

which leads to $G'_v = V_{out}/V_{in} \sim 0.86G_v \sim -0.4$, in good agreement with simulation results and with real measurements.

3.2.2. Bandwidth

The measured cutoff frequency is 600 MHz. This is a consequence of the low values of the gain, the impedances and the Miller capacitor feedback to the input which is given by $0.3(1 - G_v)$ in pF. This high cutoff frequency is well matched to the 5 ns typical rise time of the input pulses as shaped by the upstream filter. It can be noted that the transition times of the internal CP signal amount to 0.7 ns (peak to peak from −3 V dc to 0.7 V dc). As a consequence, the effective internal gate is widened up to 0.7 ns for −1.5 V, the upper limit of the input-signal dynamic range. Fig. 5 shows the effect of the gate on a dc input level.

3.2.3. Noise

The output noise level, simulated with SPICE 2G6, amounts to 50 μV rms within the bandwidth of 600 MHz as defined by the cutoff frequency. It has been traced back to the noise of the gate transistors T1–T2 and T'1–T'2 and to the noise due to the resistor environment.

4. The pulse-stretcher

The pulse-stretcher reshapes the signals coming out from the gate and is intended to comply with the specifications of the analog-to-digital converter which, in our case, are a maximum amplitude of 1 V and a whole dynamical range of 256 pC.

Since the width of the actual input pulses is small, a good approximation of a pulse-stretcher well suited for the ADC which follows, is a circuit which gives, for a δ function input pulse, an output pulse analytically described [4] by:

$$h(t) = -\frac{h_0}{\tau} e^{-t/\tau} \sin^4\left(\frac{kt}{2\tau}\right),$$

with $k = 0.8$ and $\tau = 10$ ns so that:

$$\frac{\int_0^{60\text{ ns}} h(t)\,dt}{\int_0^{\infty} h(t)\,dt} = 0.998.$$

With $h(t)$ normalized to unity ($\int_0^{\infty} h(t)\,dt = 1$), the Laplace transformation leads to:

$$H(p) = -\{(1+\tau p)(1 + 2\xi_1\tau_1 p + \tau_1^2 p^2)(1 + 2\xi_2\tau_2 p + \tau_2^2 p^2)\}^{-1},$$

with:

$$\tau_1 = \tau/(1+4k^2)^{1/2} \quad \xi_1 = \tau_1/\tau,$$

$$\tau_2 = \tau/(1+k^2)^{1/2} \quad \xi_2 = \tau_2/\tau.$$

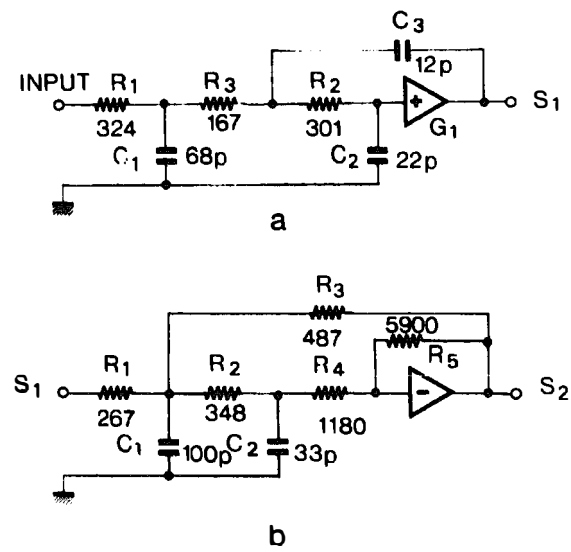


Fig. 6. (a) The third order integrator circuit. (b) The second order inverter filter.

This function $H(p)$ can be simply implemented with only two active circuits. The first one (fig. 6a) is a third order integrator circuit, made of a first order RC structure combined with a Sallen–Key second order structure. Its transfer function is given by:

$$\begin{aligned} T_1(p) = G_1\{&R_1R_2R_3C_1C_2C_3p^3 \\ &+[R_2C_2[R_1(C_1+C_3)+R_3C_3] \\ &+R_1R_3C_1[C_2+C_3(1-G_1)]]p^2 \\ &+[R_1(C_1+C_2)+(R_2+R_3)C_2 \\ &+(R_1+R_3)C_3(1-G_1)]p+1\}^{-1}. \end{aligned}$$

The second one (fig. 6b) is a second order inverted filter with a transfer function given by:

$$\begin{aligned} T_2(p) = -G_c\Big\{&\frac{R_1R_2R_3R_4C_1C_2}{K_c}p^2 \\ &+\frac{1}{K_c}[(R_1+R_2)R_3R_4C_2 \\ &+(R_2+R_4)R_1R_3C_1 \\ &+R_1R_2R_4C_2]p+1\Big\}^{-1}, \end{aligned}$$

with:

$$G_a = R_5/R_4,$$

$$K_c = (R_1+R_2+R_4)R_3 + R_1(R_2+R_4) + R_1R_4G_a,$$

$$G_c = R_3R_4G_a/K_c,$$

where G_c is the direct gain of the circuit and G_a is the loop gain of the amplifier which operates in the high frequency domain where the impedance of C_2 is low.

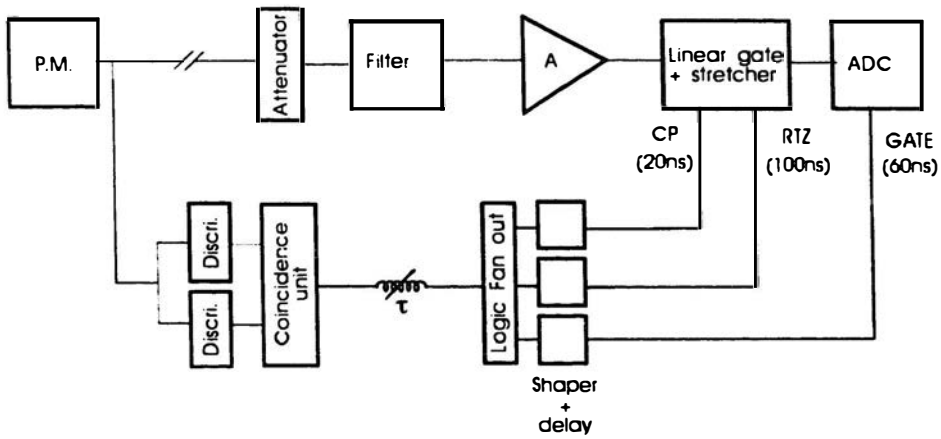


Fig. 7. The test setup.

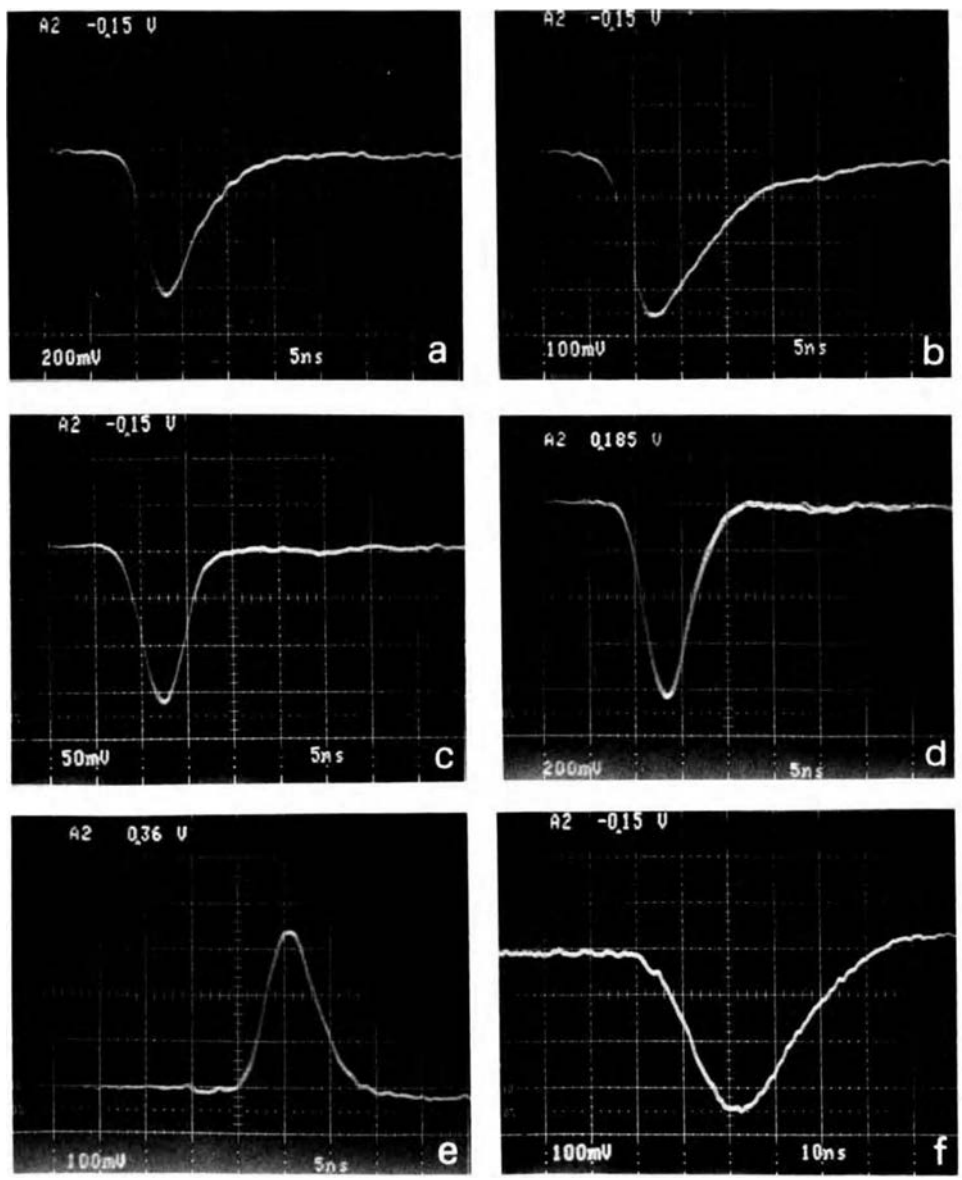


Fig. 8. Photomultiplier output pulse: (a) directly from the anode, (b) after 140 m of coaxial cable, (c) after the filter, (d) after the amplifier, (e) after the linear gate, and (f) after the stretcher.

The overall transfer function is $T(p) \equiv T_1(p)T_2(p) = G_1G_cH(p)$.

With G_1 and G_a equal to 5, which is an appropriate value for the AD5539 amplifier used in both circuits, and with G_c equal to 1, the resulting overall gain is -5. For given values of the capacitors, the values of the resistors R_1, R_2 and R_3 are then determined using a numerical method.

5. Design checks and performances

The experimental setup implemented for test purposes is schematically represented in fig. 7. It includes:

- a variable attenuator in order to measure the linearity of the whole system;
- a discriminator system which selects a small energy band of an electron source (^{90}Sr) in order to simulate a crude trigger logic.

The pulse shape at different stages of the analog part of the setup is shown in fig. 8. The effects due to the 140 m long cable are clearly visible, namely an attenuation by a factor of 2 in the pulse height and a widening of the signal shape (figs. 8a and 8b). The filter (with $k = 2$) gives a time compression factor and an attenuation factor both equal to 2, in good agreement with theoretical expectations (fig. 8c). The output signal of the filter is amplified by a factor 5 (fig. 8d). Fig. 8e shows the pulse shape at the linear gate output with no visible deformation introduced by this stage (cf. fig. 8d). Finally the signal at the output of the stretcher is given in fig. 8f.

A propagation delay of 1.5 ns has been measured for the linear gate stage whilst the overall delay between leading edges of input and output signals is equal to 25 ns. From the characteristic recovery time of the RTZ pulse, i.e. 2.5 μs, it follows that the circuit can operate at a maximum CP rate of ~ 0.2 MHz which is several orders of magnitude above actual trigger rates. The width of the CP pulse can be set between 10 and 50 ns. With a 20 ns width for this pulse we have been able to achieve a double pulse resolution of 15 ns. For lower values of this width and lower values of signal pulse duration better performances can be achieved.

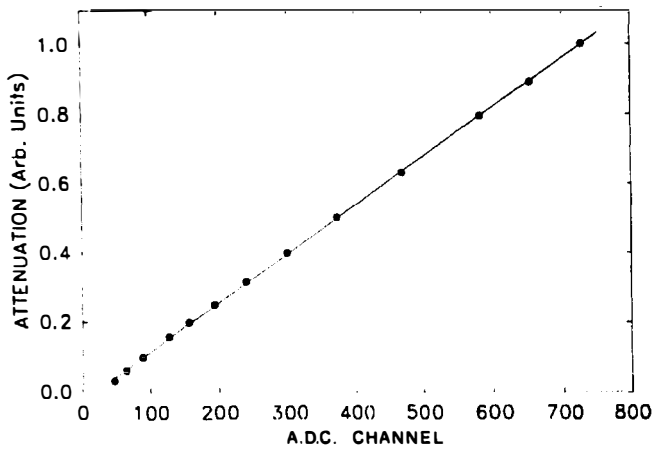


Fig. 9. The linearity curve. ADC channel content vs attenuation of the analog pulse.

The low values of opening and closing times of the internal CP result in a widening of this signal by less than 0.7 ns. This allows a good rejection of an out of time input signal.

The linearity curve is displayed in fig. 9. For the type of signal used in experiment NA38, the whole system is perfectly linear for pulse heights less than 1.5 V (attenuation factor 1 of the variable attenuator in fig. 7). This upper limit corresponds to ~ 0.5 V at the ADC input, well below the maximum amplitude that can be used with the module LRS 2249 A.

Acknowledgement

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