The ATLAS LAr calibration board

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LAPP-TECH-2003-04
October 2003

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Presented by

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at the 9th Workshop on Electronics for LHC Experiments
Amsterdam, 29 September - 3 October 2003

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Abstract

In order to calibrate the ATLAS Liquid Argon calorimeters to an accuracy better than 1%, over 16 bits dynamic range, 2 prototype boards with 128 pulse generators have been built using DMILL components.

The logic of control is able to enable the required channels, to load the DAC value, to delay and send the calibration command. The DAC voltage is distributed to the 128 channels in order to produce the 2 μA – 200 mA precision current. The voltage to current conversion uses a low-offset opamp and a 0.1% 5Ω resistor.

Exhaustive measurements have been performed on this prototype (uniformity, linearity, jitters …) and will be presented in detail.

I. INTRODUCTION

120 LAr calibration boards, which are located right on the cryostat in dedicated front-end crates, house 128 pulsers which generate accurate pulses to simulate the detector signal over the full 16 bits dynamic range.

To equip a prototype calorimeter, 10 boards have been extensively used in the test beam for the last 4 years [1]. Their performance has met the requirements in particular in terms of uniformity. However, they make use of many COTS (commercial components rad hard qualified).

Since then, several developments have been realised in order to design the "final" ATLAS calibration board, based on the same architecture but completely radiation tolerant, by migrating most of the COTS into DMILL ASICs [2].

Thus, this paper reminds the requirements and the principle of the calibration, describes the prototype built fall 2002 and the measurements performed.

II. REQUIREMENTS AND PRINCIPLE

A. Requirements

The calibration board is used to inter-calibrate the 200 000 readout channels. Thus, each calibration channel must generate accurate pulse to simulate the detector signal over the full 16 bits dynamic range (from 2μA to 200 mA). It is based upon 128 0.1% precision DC current sources and HF switches which transform the DC current into fast pulses (rise time below 1 ns) with a 400 ns exponential decay. To keep the constant term in the energy resolution better than 0.7%, the accuracy of the calibration must be good and so the integral non linearity lower than 0.1% and the non uniformity between channels better than 0.25%. The timing between real physics signal and the calibration pulse must be within ± 1 ns.

B. Principle

1) Analog part

The fast output voltage pulse is obtained by interrupting a precise DC current that flows in the inductor. When a fast TTL command pulse is applied on the NPN transistor (fig 1), the PMOS transistor is OFF and the current is diverted to ground. The magnetic energy stored in the inductor produces a voltage pulse with an exponential decay. The pair PMOS-NPN is referred as the HF switch.

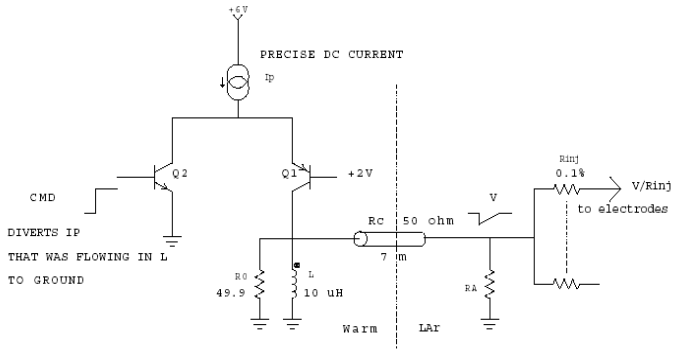

Figure 1: Pulser principle

To generate the precise DC current from 2 μA to 200 mA, a 16 bit DAC (R/2R ladder DAC) is necessary. The DAC voltage which varies from 16 μV to 1V is distributed to the 128 pulsers (fig 2) thanks to a low offset operational amplifier in voltage follower configuration.

The voltage to current conversion is built upon a low offset op amp in voltage to current converter configuration and a precise 0.1% 5Ω resistor.

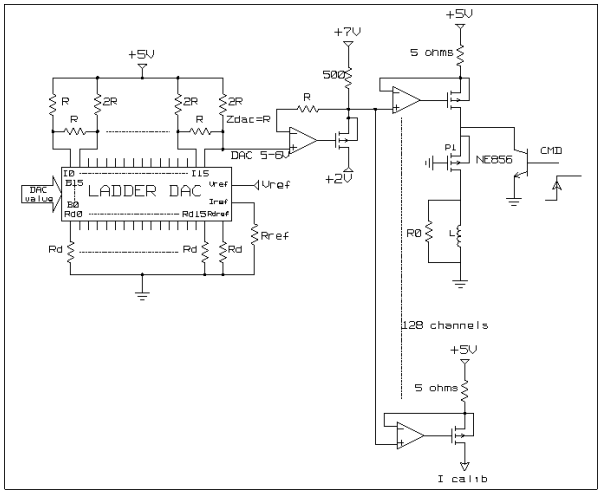

Figure 2: Simplified schematics of the full analog part

2) Digital part

The slow control of the board can be done trough the SPAC way (Serial Protocol for the ATLAS Calorimeter) [3]. The SPAC master located in the Read Out Crate sends information to the SPAC slave mounted on the calibration board which is used like an I2C (serial protocol) master. Thus this I2C master (fig 3) can enable the chosen channels among 128 channels via 4 ASICs configured in 32 bits output register (REG0-3). It is also able to load he DAC value through an ASIC configured in 16 bits output register (DAC). In order to compensate the cable lengths the calibration command can be delayed by step of 1 ns trough 2 ASICs (Delay0-1) managed by I2C. Each delay line (total of 8) distributes the calibration command to 16 channels.

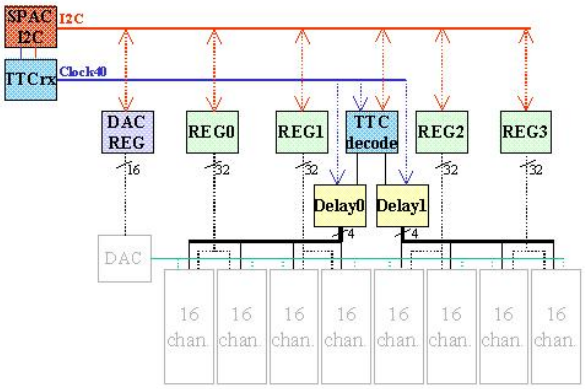

Figure 3: Schematics of the digital part.

As the calibration board must generate commands synchronous to the LHC machine, a TTCRx [4] is mounted on the board to interface the TTC system (Timing and Trigger Control distribution) to our application. So an ASIC (TTC decode) is dedicated to decode several TTCRx commands like reset or calibration command.

III. CALIBRATION BOARD DESIGN

The calibration board is divided in 2 groups of 8 rows of 8 operational amplifiers. The correct star distribution of the DAC (fig 4) with respect to the VP6 requires careful attention. In particular, the 5V reference (VP6) is made with a common point on board center (dimension 2 x 1 cm = 1 mΩ). All the lines connecting the 5 Ω resistors to the reference VP6 taken for the DAC should be equalized in resistance and cannot be shared between channels; DAC variation with the number of enabled channels hasto be avoided. 5 layers are necessary to route this VP6 with equalized lengths .

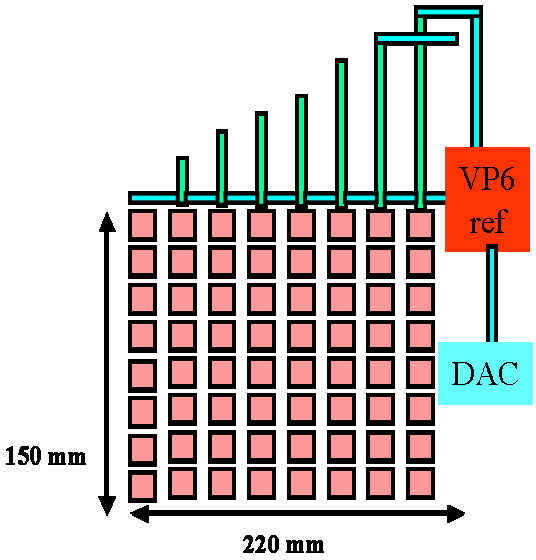

Figure 4: VP6 star distribution for a group of 8x8 op. amp.

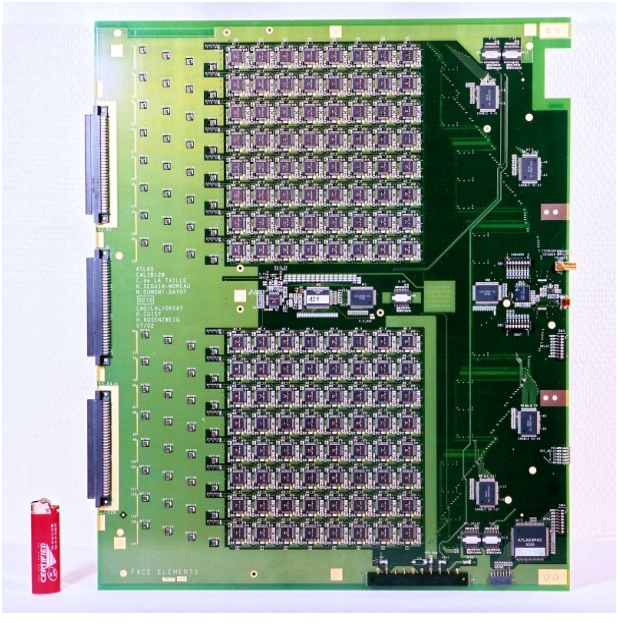

Figure 5: Calibration board prototype (49.5 x 40.5 cm).

IV. MEASUREMENTS RESULTS

Exhaustive measurements have been performed in order to fully validate the calibration board in terms of electrical or timing characteristics.

A. *Signal shape before shaping*

The signal shapes have been studied over the full DAC range (100µV-1V, up to 5V pulses in 50 Ω resistors). The figure 6 shows that the fall time remained below 2 ns with few variations. We can also note that HF ringings are present for small DAC values and are due to the parasitic inductance package.

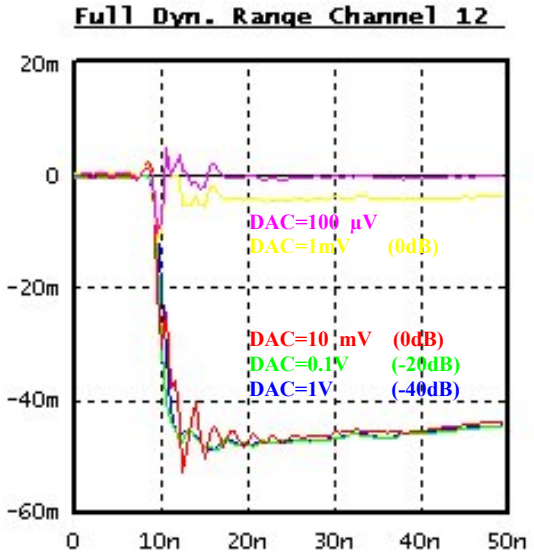

Figure 6: Pulse shape before shaping.

B. *Parasitic Injected Charge*

The small signal obtained when setting DAC=0 (or close to zero) is referred to as "Parasitic Injected Charge" (PIC). This parasitic charge injection is due to the parasitic inductance between the PMOS located inside the op amp package and the external NE856 transistor which makes a resonant circuit with the gate-source capacitance (C_{GS} ~20 pF).

After shaping (CRRC2 shaper with tp=50 ns), the PIC contribution is very small: it is equivalent at its peak to a DAC setting of 30 µV and at the maximum of the signal, to a DAC setting of 15 µV (1 LSB). The PIC contribution to the signal has been decreased by a factor 10 with respect to the testbeam boards.The dynamic range of the calibration output pulses is 60000 or 5V/ 75 µV.

C. *Uniformity*

1) *DC uniformity.*

The DC uniformity (fig 7) has been measured by monitoring the DC output current of the 128 channels for a 10mV DAC value using a precise 16 bits multimeter. This uniformity shows a mean of 1973.5µA with 6.17 of RMS (blue and green plot). Taking into account of the operational amplifier offset distribution this value falls to a mean of 1970.8 with 1.04 RMS (red and yellow plot) (σ=0.05%). So the DAC voltage is well distributed all over the board.

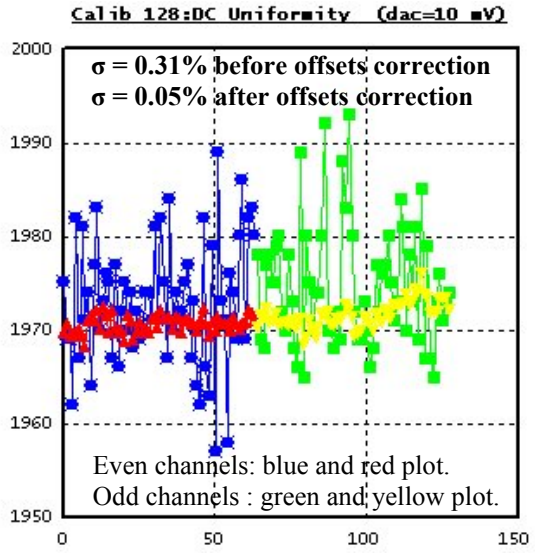

Figure 7: DC uniformity

2) *Pulse uniformity*

The pulse amplitude uniformity (fig 8) has been measured with a 12 bits ADC after a CRRC2 shaper (tp=50 ns) for a 10mV DAC value. This measurement shows a RMS of 0.43% before shaping and 0.33% after shaping. An another study underlines the fact that the pulse and DC uniformity are well correlated.

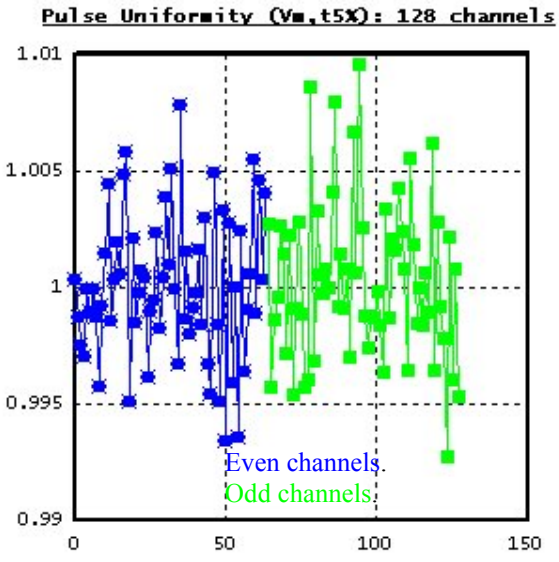

Figure 8: Pulse uniformity after shaping

D. Linearity

The DC linearity has been measured with a precise 16 bits multimeter and the pulse linearity with a 12 bits ADC sampling the signal at the peak after a CRRC2 shaper (tp=50 ns). These measurements were performed over the 3 shaper gains (1,10,100) (fig 9).

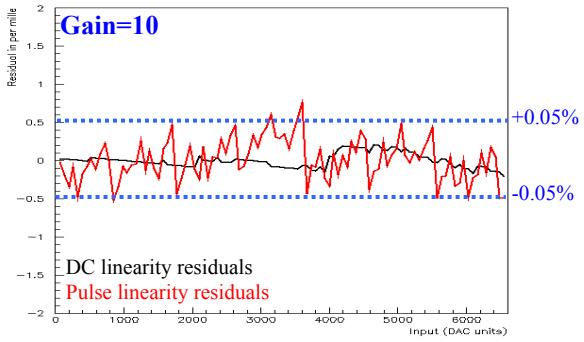

Figure 9: Linear fits residuals of the DC and pulse linearity (gain=10)

For all the 3 gains the DC and the pulse residuals are within ±0.05%. Thus the DC and dynamic linearity performances are in the same range.

E. Preliminary noise study

Preliminary noise studies have been done inside the front end crate using one front end board (shaper followed by 12 bits ADC) in order to read the overall 128 output channels. The noise has been characterised powering or not the calibration board. The noise ratio comparing the noise induced by the calibration powered or not is nearly 1 with small dispersion overall the channels and is presented in table 1.

	Noise (Calib. ON / Calib OFF)	σ
Channels OFF	1.005	0.001
Channels ON	1.002	0.001

Table 1: Noise study

This preliminary study shows that calibration board does not introduce sizeable noise. Of course this study is preliminary and must be developed later.

F. Timing characteristics

All the timing characteristics have been investigated using a Wave Pro 950 Lecroy (1Ghz analog bandwidth, 16Gsa/s) scope. This instrument contains a full toolkit very useful to histogram different values like timing delay.

1) Timing uniformity.

The timing uniformity over the 128 channels has been done measuring the delay between the channel0 and the others for a 30 mV DAC value at a -20mV trigger level (fig 10).

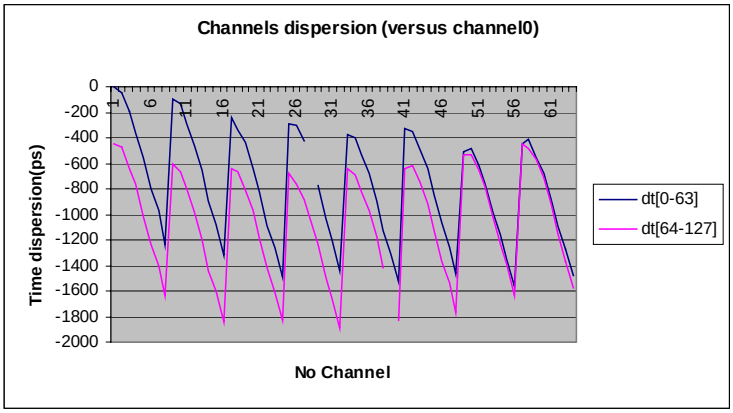

Figure 10: Timing uniformity

As a same calibration command signal serves a full row of 8 operational amplifiers there is a large dispersion around 1.2 ns inside a same row (channel<0-7>, channel<8-15>,…..). We can also note that a time dispersion remains between rows because all the calibration lines are not equalised in lengths. This will be corrected in the next prototype layout.

2) Jitters study

This study has been done in order to characterise the total jitters induced by the full calibration setup (from the TTC 40Mhz clock to the output calibration signal). This has been measured recording the histogram of the delay between the 40Mhz TTCvx (TTC optical to electrical conversion) output clock rising edge and the falling edge of the output calibration signal for the output channel 0. As the calibration command can be delayed playing with coarse delay (step of 1 ns delivered by the delay chip) or fine delay (step of 104 ps delivered by the TTCRx) the jitters have been characterised scanning the fine or coarse delay.

The figure 11 and 12 shows that the jitters remains between 45 and 55 ps scanning the TTCRx delay and between 48 to 53 ps scanning the Delay chip delay from 0 to 24 ns.

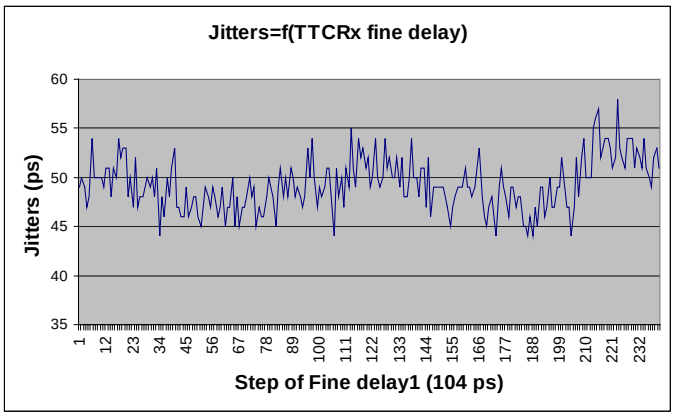

Figure 11: Jitters according fine deskew1 delay (TTCRx)

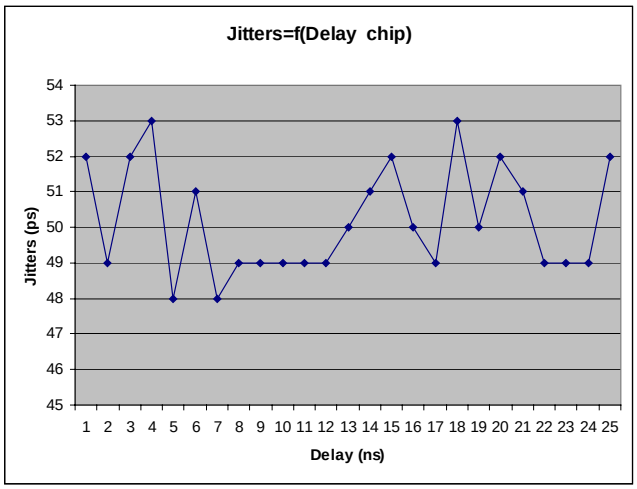

Figure 12: Jitters according coarse delay (Delay chip)

These results are very encouraging as we expected a value around 100 ps.

V. Front End Crate installation

One calibration board has been successfully installed inside the prototype of the front end crate (FEC) at BNL (Brookhaven National Laboratory-USA) in march 2003. Different measurements (uniformity, linearity, noise …) have been done in order to characterise the calibration board inside this environment. These analog measurements showed that there are few differences between the ones performed at BNL and at Orsay.

Since then the calibration board is currently used to test and validate the full front end crate installation.

VI. Conclusion

Extensive measurements have been done in order to fully characterise the calibration board and the results respond to the specifications needed. However a final version has been designed in order to correct minor problems and is expected fall 2003. The next and final step will be the production of 130 boards starting spring 2004 as the front end electronics installation is foreseen end 2004.

VII. References

[1] G.Perrot : The ATLAS calorimeter calibration board (LEB5-Snowmass).

[2] N.Seguin-Moreau : Calibration boards for the ATLAS Lar calorimeters (LEB8-Colmar).

[3] B.Laforge :Implementation of a Serial Protocol for the liquid argon Atlas Calorimeter (SPAC) (LEB6-Crakow).

[4] T.Toifl : Measurements of the radiation effects on the Timing, Trigger and Control Receiver (TTCRx) Asic (LEB6-Cracow).