ATLAS LARG online data acquisition system Read out drivel level

G. Ionescu, R. Lafaye, L. Poggioli, I. Wingerter-Seez

To cite this version:

G. Ionescu, R. Lafaye, L. Poggioli, I. Wingerter-Seez. ATLAS LARG online data acquisition system Read out drivel level. IEEE NPSS Real Time Conference, May 2003, Montreal, Canada. in2p3-00014088

HAL Id: in2p3-00014088

http://hal.in2p3.fr/in2p3-00014088

Submitted on 30 Oct 2003

LAPP-EXP-2003-13
September 2003

ATLAS LARG Online Data Acquisition System
Read out driver level

G. Ionescu, R. Lafaye, L. Poggioli and I. Wingerter-Seez

LAPP-IN2P3-CNRS
9 chemin de Bellevue - BP. 110
F-74941 Annecy-le-Vieux Cedex

Presented at the 13th IEEE NPSS Real Time Conference

Montreal, Canada, May 18-23, 2003

ATLAS LARG Online Data Acquisition System
Read Out Driver Level

Gelu Ionescu, Rémi Lafaye, Luc Poggioli and Isabelle Wingerter-Seez

Abstract-- **The purpose of this paper is to present the hardware and software architecture of the Liquid Argon (LARG) Online Data Acquisition System. We will emphasize especially: the software system use cases (i.e. physics, calibration, data monitoring and system monitoring), the central role played by the DSP in achieving those goals, the embedded software solution working inside the DSP and the modular and flexible OO framework developed to control the various electronic boards working in different VME crates. The tests already performed and future software validation stages will also be presented.**

I. INTRODUCTION

THE main goal of the ATLAS experiment at the Large Hadron Collider (LHC), located at CERN, is to study the evidence of new physics especially the search for the Higgs boson. The LARG calorimeter plays a central role in ATLAS; it is designed to trigger on and to provide precision measurements of electrons, photons, jets and missing transverse energy (ET). The LARG Front End electronic system has to read out several units (presampler, EM calorimeters, hadronic end-cap and forward calorimeters) for a total of ~ 200000 independent channels. The deposited energy (from 30 MeV up to 3 TeV) arising from proton-proton interactions induces a proportional current on the detector electrodes. The read-out system samples the signals at 40 MHz. Signals from the detectors are processed by various stages before being delivered to the DAQ system. A critical stage of this processing is the analog summation to build Trigger Towers. Conditions on local energy deposits are applied (minimum ET, isolation) to Trigger Towers to define a triggered event called “Level-1 trigger”. The maximum Level-1 trigger rate is limited to 100 kHz due to different system constraints. These events are delivered, after digitization, to the Read Out Driver (ROD) level via optical links. It is the role of the LARG Online Data Acquisition System (i.e. a subsystem of the overall DAQ system) to supervise the data processing and the ROD system behavior. It can be seen as a distributed real-time system deployed on: 6 work stations, 6 VME partition crates, 16 VME ROD crates and ~ 1600 DSPs.

In the next section the digital electronics involved in the system control and configuration will be described. Section III will be dedicated to the embedded software running into the ROD's processing unit. In Section IV, we will describe the general software framework responsible for controlling and monitoring the data acquisition. The performed tests and the future software validation stages will be presented in Section V.

II. HARDWARE DESCRIPTION

The global LARG electronics system [1, 2] will be split in six logical partitions: two for the half-barrel electromagnetic calorimeters (EMB), two endcap electromagnetic calorimeters (EMEC), the hadronic calorimeter (HEC) and the forward calorimeter (FCAL). Each logical partition can be run in stand-alone mode. From the software point of view this partitioning mirrors the overall system granularity. Table I gives the hardware deployment over those six partitions and Fig. 1 shows the interconnection of various digital electronic elements involved in data processing and partition control.

The following sections provide more details on digital electronic elements that can be configured by software. This electronics is situated near the detector or off the detector in the control room.

A. Central Trigger Processor

Situated in the ATLAS trigger cavern, the Central Trigger Processor (CTP) receives trigger information mainly from the calorimeters and muon trigger processors [3]. It makes the Level-1 decision (L1A) based on a trigger menu and is conditioned by the BUSY signal provided by the ROD system. The Timing, Trigger and Control (TTC) system distributes the L1A decision together with the 40 MHz clock (i.e. LHC Bunch Crossing BC), other trigger information (i.e. Orbit Reset, Bunch Crossing ID, Event ID and Trigger Type) and control commands to the detector front-end electronics. The Readout Driver Busy Tree (BUSY) is a hierarchically structured fast feedback network, which receives the BUSY signal from the detector's RODs and sends it to the CTP. The TTC and BUSY system of the ATLAS experiment can be partitioned. Each TTC and BUSY partition can be run with the central ATLAS timing and trigger signals, or independently with their own specific timing and trigger signals.

Manuscript received May 17, 2003.

G. Ionescu, R. Lafaye, L. Poggioli and I. Wingerter-Seez are with Laboratoire d'Annecy le Vieux de Physique de Particules (LAPP), 74941 Annecy le Vieux, France (telephone: (33)450091600, e-mail: ionescu@lapp.in2p3.fr, lafaye@lapp.in2p3.fr, poggioli@lapp.in2p3.fr, isabelle@lapp.in2p3.fr.

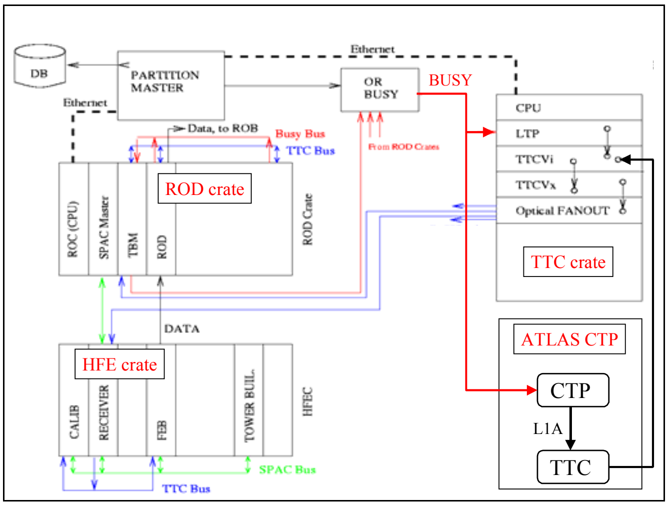

Fig. 1. Block diagram of the partition read-out electronics. This drawing shows the minimal hardware configuration of a partition. *A. System Synchronization*. The overall system synchronization is under the control of the CTP. The Partition crate distributes, through the TTCvi, all the synchronization signals to the subjacent ROD and HFE crates. In stand-alone mode the role of the CTP is played by the LTP. The CTP stops to send L1A pulses when the ROD system asserts the BUSY signals. *B. Data Path*. The analog data digitized by the FEB are sent by optical fibers to the ROD modules. The results calculated by the DSPs are sent afterward to the ROB modules. *C. Configuration Path*. Working in master/slave architecture, the SPAC module is used to set-up parameters into the HFEC's boards.

B. *Half Front End Crate*

The sensitive analog electronics is housed in the Half Front End Crate (HFEC) attached to the cold to warm feedthroughs. The maximal configuration of the HFEC is shown in Table II. This crate contains the following type of boards:

1. **Front End Controller (FEC).** The controller board's role [4] is to receive and distribute the LHC BC, the L1A signal, as well as other fast synchronous signals, and to receive and distribute control information to configure and control the various boards in the HFEC.
2. **Calibration board.** This board was conceived in order to calibrate the LARG calorimeters to an accuracy level better than 1%, over 16 bits dynamic range [5].
3. **Front End Board (FEB).** This board contains the electronics for amplifying, shaping, sampling, pipelining and digitizing the LARG calorimeter signals. The control of this board is done by the Switched Capacitor Array Controller (SCAC) element. One FEB will process 128 independent signal channels.
4. **Tower Builder (TB).** This board performs the final level of analog summation to form trigger tower analog signals [6] and transmit them to the Level-1 cavern for digitization and processing by the Level-1 trigger processor.

C. *TTC Crate or Partition Crate*

As shown in Fig. 1, the TTC crate houses digital electronics responsible for supervising the partition behavior.

1. **CPU.** The crate's CPU is connected to the network and coordinates both the crate activity and the partition's front-end electronics behavior.
2. **TTCvi.** Fully programmable by VME, this device is the key component of the TTC distribution system. Actually, it represents the interface between the CTP and the partition's electronics. Each slave module in the TTC network will be equipped with a TTCrx receiver.
3. **Local Trigger Processor (LTP).** ATLAS is divided in 36 partitions, each of them having its own TTC network, controlled by its own TTCvi. When the partition runs in stand-alone mode the LTP ensures that the local TTC signals are kept separated from the main ATLAS central DAQ system.

D. *Read Out Crate*

As shown in Fig. 1, the LARG off-detector electronics is located in the Read Out Crate (ROC). Each ROC houses the digital signal processing units and several VME modules involved in the system control (see Table III for the maximal crate configuration).

1. **CPU** The crate's CPU is connected to the network and coordinates the ROD crate activity and the associated HFEC as well via the SPAC module.
2. **SPAC** The front-end electronics of the LARG calorimeters will be driven through a serial link between the counting room and the front-end boards. This link, known as SPAC (Serial Protocol for the ATLAS Calorimeters), is used to configure the various registers and memories of the HFEC boards [4]. Each serial network consists of one master and multiples slaves.
3. **TTC and Busy (TBM).** This module receives the TTC information from the partition's TTCvi, fans it out to the RODs and collects their BUSY signals.
4. **Read Out Driver (ROD)**. This module [7] receives raw data from eight FEBs and extracts the signal parameters (i.e. energy, time and shape quality factor). The results are then sent to the Read Out Buffer (ROB) modules.

III. DSP EMBEDDED SOFTWARE

To have a complete understanding of the data acquisition (DAQ) system, a short explanation of different constraints on analog and digital data taking is necessary. Afterwards the complete DSP embedded software solution will be explained.

A. *Read-out Architecture*

After analog processing in the FEBs, the calorimeter signals are sampled at the BC frequency of 40 MHz and stored in switched-capacitor array (SCA) analog pipelines during the Level-1 trigger latency. The SCA provides 144 storage cells for each signal channel. As shown in Fig. 2, the SCA is controlled by a SCAC. Note that two absolutely independent SCACs exist, each of them controlling 64 calorimeter cells. The SCAC receives trigger information through the TTCvi / TTCrx channel and starts the signal digitization upon the L1A pulse reception. After digitization, a programmable number of samples (typically 5 or 7) will constitute the channel event packet. Roughly, the FEB event data consists of a header (start of event marker, bunch crossing ID – BCID, event ID – EVID), the data zone (128 channel data packets) and a trailer (end of event marker). The serialized FEB event is then sent by optical link.

The time necessary to transmit an event will fix the maximum event rate at the input of the ROD system. For a 5 samples event the data transmission takes 10 µs (a maximum event rate of 100 kHz can be expected).

TABLE I
HARDWARE DEPLOYMENT

Element	#	FEB	ROD	ROB	Crates
EMB A & C	2	896	112	448	8
EMEC A & C	2	552	70	276	6
HEC	1	48	6	24	1
FCAL	1	28	4	14	1
Total	6	1524	192	762	16 + 6

TABLE II
HFEC MAXIMAL CONFIGURATION

Controller	Calibration	FEB	TB
1	1	14	1

TABLE III
ROC MAXIMAL CONFIGURATION

Element	CPU	ROD	SPAC	TBM
VME 64x 6U	1			
VME 64x 9U		14	2	1
DSP & FEB		112		
Masters & HFEC			8	

B. L1A Generation Constraints

The L1 trigger latency is configurable between 14 and 125 clock cycles. A typical latency value of 2.5 µs means that 100 cells of the SCA analog pipeline will be reserved for trigger latency purposes. The CTP is supposed to prevent the overlapping events for normal data taking (for 5 samples, the maximum L1A rate should be 8 MHz and the SCA will contain 8 events. To prevent extra L1 trigger generation, the CTP will generate the LOCAL BUSY signal (see Fig. 2).

C. Processing Unit

The ROD module is the key element of the LARG read-out system. Each ROD module receives and processes data from up to 8 independent FEBs (1024 calorimeter cells). The architecture of this board is achieved in a modular way and consists of a VME 9U motherboard that houses 8 GLINK optical fibers connecting the ROD to the subjacent FEBs, 4 mezzanine boards called processing units (PU), 4 output controllers (OC) that formats the output event and 4 SLINK optical fibers connecting the ROD to the subjacent ROBs. The PU's architecture [8] is build around the S2P programmable component (FPGA) responsible for deserializing the incoming event and a TMS320C6414 DSP.

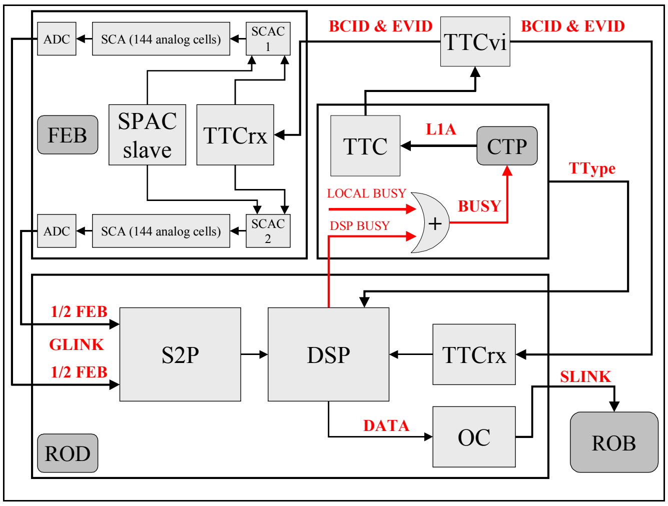

Fig. 2. Block diagram of data processing path and BUSY generation. When the conditions for L1A generation are met, the L1A pulse, BCID and EVID are distributed to the front-end electronics and to the ROD system. The data associated with the L1A is digitized, formatted and serialized are sent by optical link to the ROD digital signal processing module. An internal LOCAL BUSY signal will inhibit the L1A generation if the FEB's SCA has no more room for a new event. In the ROD module, the data is deserialized by the S2P chip and processed by the DSP. The DSP tasks consists of: verifying the synchronization of the TTC information (BCID/EVID identifier found in the event header and received from the TTCrx), processing and reformatting the data, sending the data to the ROB and generating a BUSY signal if the DSP cannot follow the input event rate.

D. PU's Data Flow and BUSY Tasks

The real-time digital data processing happens in the PU. In order to optimize the processing time, the tasks will be distributed between the S2P unit, the DSP and the OC unit.

1) Data consistency check

Various digital electronic elements are subjected to a flux of hadronic particles during operation, which can cause Single Event Upset (SEU). SEU are nondestructive changes of signals or stored status due to charge deposits in the silicon chip by ionizing particles. The main role of the S2P unit is to deserialize the incoming event and to reformat it as required by the algorithm running in the DSP. It is also involved in the data consistency check. In particular, the S2P unit checks the parity, verifies the synchronization of the two half FEB events and detects SEU errors. A status word will be send to the DSP to notify it about the event consistency. Upon reception of the status word, the DSP will warn the calorimeters control system if an error is detected.

2) TTC information check

The DSP receives TTC information from two channels: the header of the data event that contains the BCID/EVID identifier attached by the FEB and the BCID/EVID identifier sent by the CTP directly to the ROD system. It is the role of the DSP to verify the BCID/EVID synchronization and to try to resynchronize the data flow.

3) Data flow bandwidth optimization

The PU's output data bandwidth is less then half of the input data bandwidth. Consequently, the OC will combine the events generated by two DSPs and send them to the ROB through a single SLINK fiber.

4) *BUSY generation*

When the DSP cannot follow anymore the incoming event flow, it will generate a BUSY signal (in principle this signal should never be asserted). Raised up to the CTP, this signal will inhibit the L1A generation but the DSP should still be prepared to receive the L1A pulses already registered in the FEB (i.e. for 5 samples, up to 8 L1A can be pipelined). For this reason the incoming events are stored in an internal circular buffer providing enough room to overcome this situation. To prevent short spikes the BUSY signal behaves in a hysteresis manner i.e. the BUSY signal will be asserted when the security limit is touched (e.g. 8 events) and removed when a safe limit is guaranteed (e.g. 10 events).

E. Event Processing Inside the DSP

In physics mode the DSP accomplishes two computation tasks:

1. Extracts signal parameters (energy, time and the quality factor $\chi 2$) from the event samples s_i with the following formulas:

$$E=\sum_{i=0}^{n} a_i(s_i-p) \quad ; \quad Et=\sum_{i=0}^{n} b_i(s_i-p) \qquad (1)$$

$$\chi^2=\sum_{i=0}^{n}\left((s_i-p)-Eh_i\right)^2 \qquad (2)$$

   where p is the pedestal, a_i,b_i are constants calculated in the calibration process by optimal filtering method, h_i the expected shape and n the number of samples (typically 5 or 7).
2. Fills histograms used in the online data monitoring.

In choosing the DSP, an important constraint was imposed: an event should be processed (i.e. data input, parameter extraction, histogram computation and data output) in less than 10 µs corresponding to the maximum event rate. To achieve this goal, the processing code was written in linear assembly language and optimized with the Code Composer Studio (CCS) from Texas Instruments for TMS320C6414 DSP. As shown in Fig. 3, several scenarios were investigated to minimize the parameter extraction time and to maximize the number of provided histograms.

When running in calibration mode, the DSP computes the mean value m and the variance v of each channel with the following formulas:

$$m=\sum_{i=0}^{n} s_i \qquad v=\sum_{i=0}^{n} s_i^2 \qquad (3)$$

Those values will be transferred to the crate's CPU to calculate the calibration coefficients.

F. DSP Embedded Software

To manage the different tasks of the DSP we have created the Liquid Argon Real Time Executive (LaRTX). Written mainly in C, this small operating system (i.e. about 1.5 Kbytes) can oversee up to 32 tasks of different priorities following a preemptive strategy. The tasks are created statically at the system boot and the inter-task information exchange is done via classical services: messages, queues and semaphores. Two special services, immediate task resume or delayed task resume, were added to provide fast task registration in the *ready to run* task list.

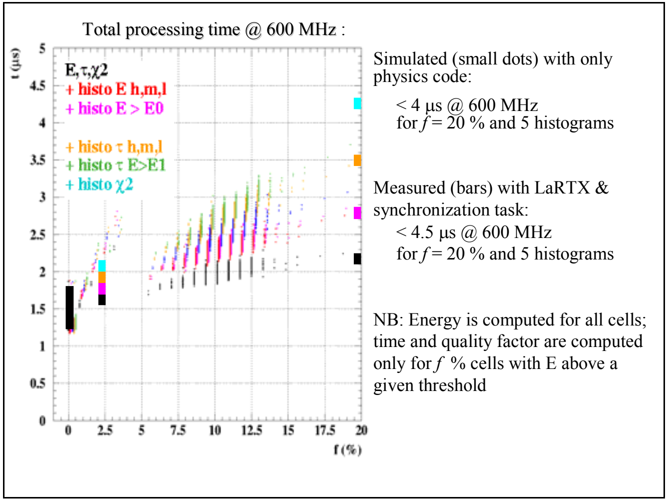

Fig. 3. Total processing time distribution. Several scenarios were simulated on a 600 MHz DSP and measured on a real DSP installed on the demonstration board.

IV. CONTROLLING AND MONITORING SOFTWARE

The LARG Online data acquisition system covers three main software aspects: the real time digital data processing (detailed in the previous chapter), the overall system control and the online data monitoring. The following sections provide more details concerning the last mentioned points.

A. High level uses cases

As shown in Fig. 4, the Read-out software system is a complement of Trigger Data Acquisition System (TDAQ). The TDAQ software can be seen as distributed online software responsible to send commands to all elements registered in the system (i.e. described by the configuration database). It is important to note that, all the operations (i.e. software and hardware configuration, system controlling, error reporting and data and system monitoring) should pass through the TDAQ system.

The overall acquisition system should provide interfaces at least for the following use cases:

1. **Physics run**. After the system configuration (i.e. new calibration constants loaded into the DSP), the data acquisition should happen without external intervention for about 10 hours. In this mode, the data follows the classical path: FEB, DSP, ROB.
2. **Data monitoring**. Closely linked to the physics run, this mode should allow the data validity check using histograms. Build by the DSP, the histograms are transferred and displayed using an internal support of the TDAQ software. Monitoring inside the DSP is mandatory, as some basic information will not be transmitted to higher processing levels.
3. **Calibration run**. Several calibration scenarios are presently considered. The basic one is executed at the ROC level before physics run and takes about 10 min.

The calibration parameters (3) calculated by the DSPs are transferred by VME to the crate's CPU where the calibration constants are calculated. At the end of the procedure, the constants are stored in the condition database accessible by the online and offline system.

4. **System monitoring**. The user of the Read-out system should have the possibility to verify the status of each element involved in the system.

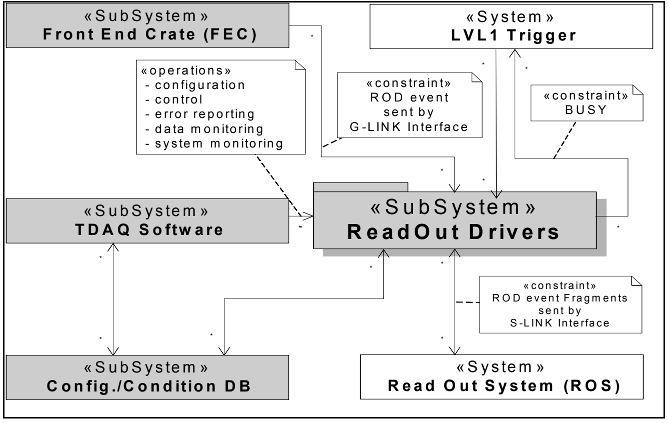

Fig. 4. Block diagram of the Read-out Software System. The Read-out sub-system can be seen as a complement of the TDAQ software. The synchronization signals are received from LVL1 Trigger. Roughly, its role is to extract signal parameters from the events sent by the front-end electronics and to send them to the ROS in a known format.

B. *LARG Online Framework*

The software developed in the LARG Online Framework is written in C++ and follows an Object Oriented (OO) technology applied to the partition structure. In this sense, three kinds of software objects were created: 1. VME controlled modules can be instantiated in both partition and ROD crates; they are used to interface VME modules; 2. SPAC controlled modules are instantiated in the ROD crate; they are used to control the HFEC via the SPAC module; 3. TTCvi controlled modules are instantiated in the partition crate; they are used to control the HFEC via the TTCvi module.

1) VME controlled modules

We based the development of this object on two main requirements: the software should run transparently on different VME platforms (e.g. RIO, VMIC, BIT3, Concurrent Technologies, etc.) and, several VME modules (e.g. ROD, SPAC, TTCvi) can be seen as a collection of identical sub-modules (e.g. the ROD boards houses 8 identical PUs and 4 identical OCs). As shown in Fig. 5, a concrete module will be designed in a layered approach: the root *LargObject* virtual class implements the object validity check and the TDAQ default interface and the *Module* virtual class contains all the primitives used to interface a concrete module with the VME platform. Finally, the module itself, RODdemo in Fig. 5, is a container controlling the construction/destruction mechanism for all the subjacent sub-modules and overseeing the board behavior. The sub-module in counterpart (e.g. PU and OC) implements all specific low level functions.

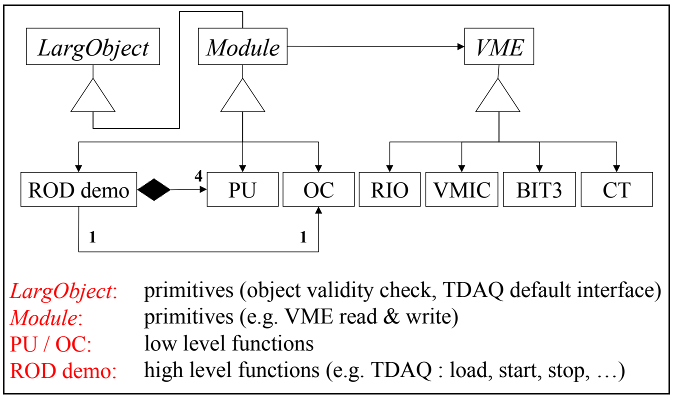

Fig. 5. VME *Module*: Design Pattern. The four SW layers of this architecture are identified in the legend.

2) SPAC and TTCvi controlled modules

We have applied the same technique to develop the software controlled by SPAC or TTCvi. They are also derived from the root *LargObject* virtual class and implement the set of specific functions necessary to control the HFEC electronics.

V. TESTS AND PERSPECTIVES

The DSP embedded software and the LARG online framework are used extensively in several test benches. The final ROD production test bench installed at LAPP, the calibration board test bench installed at LAPP and LAL (Orsay) and the test of the HFEC installed at Brookhaven National Laboratories (BNL) demonstrate the properties of this framework: robust an reliable architecture, compliance and complementarily with TDAQ and easy integration of new features.

Our immediate objective is to use the BNL HFEC test as a kernel for the new planned tests: ROD crate test (fall 2003), coherent noise measurement for the entire barrel calorimeter (fall 2003) and combined EMB & TILE run (spring 2004) .

VI. ACKNOWLEDGMENT

The authors would like to acknowledge the cooperation of the LARG online developers community.

VII. REFERENCES

[1] ATLAS Liquid Argon TDR: http://atlas.web.cern.ch/Atlas/GROUPS/LIQARGEXT/TDR/

[2] The ATLAS LARG ROD System: http://wwwlapp.in2p3.fr/~poggioli/Working_version.doc

[3] ATLAS Level-1 CTP and TTC: http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/LEVEL1/ctpttc/L1CTP.html

[4] SPAC system and Controller design: http://lpnhe-atlas.in2p3.fr/pubdocs/

[5] J. Colas et al., "The LARG calorimeter calibration board", *ATL-LARG-2000-006*.

[6] LARG Tower Builder Board: calculation, simulation, measurements: http://schwind.home.cern.ch/schwind/atlas/calo/docs/note_tb.pdf

[7] LARG ROD board: http://dpnc.unige.ch/LArgROD/

[8] ROD Process Unit http://wwwlapp.in2p3.fr/Electronique/Experiences/ATLAS-ELEC/Rod/index.html