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A 16 channel analog integrated circuit for PMT pulses processing

L. Gallin-Martel, J. Poux, O. Rossetto, M. Yamouni

Abstract—In this paper we present an integrated circuit designed for PMT pulse processing. This circuit was developed for the RICH detector of the AMS experiment. It integrates 16 identical channels and has to deal with space environment constraints (low power consumption, radiation hardness). It processes the 16 analog signals coming from anodes of a multi-anode PMT and the signal coming from a dynode. It integrates a control logic for the multiplexing of the output data. A test mode that can be activated for the calibration of each channel. An offset cancellation system has been designed for the dynode channel. This offset cancellation is important in order to avoid thermal drifts and offset spreads.

Index Terms—Analog processing circuits, integrated circuits, filters, charge measurement, photomultipliers.

I. INTRODUCTION

Photomultiplier tubes are widely used in physics experiments. For example in the RICH detector of the AMS project, more than 1000 multi-anode PMT are used [1]. This represents an amount of 16000 signals to process. Furthermore, the integrated circuit has to operate in space environment, which imposes some constraints (radiation hardness, low power consumption, and very compact front-end electronics) that can be solved only by designing a dedicated integrated circuit for the front-end signal processing. The photomultiplier tubes used in this experiment are composed of 16 anodes. In order to use one integrated circuit per PMT it integrates 16 identical multiplexed channels for charge measurement and an additional channel for the last dynode channel processing used for the tagging. In order to increase the dynamic range, a multi-gain system has been integrated. The circuit also integrates test functions that are used for its calibration.

II. CIRCUIT ARCHITECTURE

Different solutions can be implemented for the analog preprocessing of PMT signals in order to measure the total charge of the pulse. The most common techniques are based on the pulse total charge measurement [2,3]. An other solution based on the time over threshold (TOT) measurement after a pulse stretching has also been proposed for the AMS RICH [4]. The main drawback of this second solution is that a small offset on the voltage comparator input may introduce a large error on the final measurement. For power consumption consideration we used a CMOS

technology. This technology is known to have a large offset due mainly to threshold voltage spread on MOS transistors. This voltage spread is incompatible with a solution based on the TOT measurement. For this reason, we used an architecture based on a spectrometry chain. This method gives a voltage signal proportional to the charge of the input pulse. The circuit integrates 16 identical channels. The analog output of each channel is memorized into the track-and-hold and the 16 outputs are read sequentially via a multiplexer in order to reduce the number of input/output pads. Fig. 1 shows the architecture of the complete circuit.

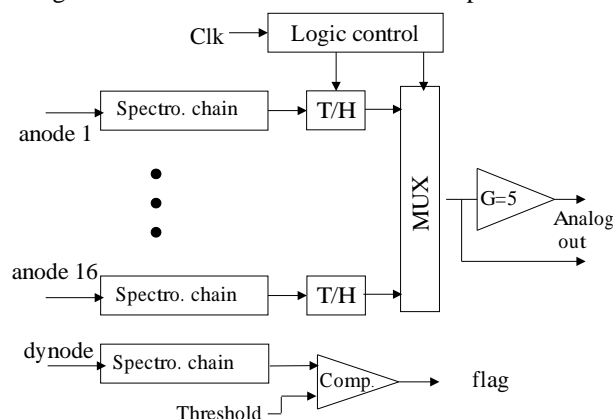


Fig. 1 : Circuit architecture

In order to increase the resolution for small signals, an amplifier with a 5x gain has been added at the output. In this case, the calibration of the system gain (circuit and PMT) can be done with the single photo-electron response. The amplifier with unity gain ensures a large dynamic range, up to 200 photo-electrons with a minimum distortion. A switch selects the gain 1 or gain 5 output. Without this dual gain system, a minimum of 14 bits should be necessary on the output ADC in order to calibrate properly the system's response and to achieve a sufficient dynamic range (6 bits of resolution for the single photo-electron plus 8 bits for the complete dynamic range). Such a ADC is not fast enough to meet the data acquisition system requirements with low power consumption.

A 17th channel, the tagging channel, has been added on the circuit. This channel indicates that one or more channels of the PMT have fired. This output is used in the data acquisition system in order to read only the active circuits, reducing the data acquisition time [5].

In order to minimize the number of input pads, the logic control has only one clock input signal instead of a classical 4 to 16 decoder for the control of the multiplexer.

III. THE ANALOG CHANNEL PRINCIPLE

The spectrometry chain we used is composed of a charge integrator followed by a first order high pass filter with a pole-zero cancellation followed by a 5th order low pass filter. This results in a quasi gaussian shaped pulse [6]. The time constant of the circuit used in the system (200ns) is large enough so that it is easy to sample the signal on its maximum (about 1.9 μ s). The peak amplitude is directly proportional to the total charge. Simulation results show that a time shift of 25ns on the hold pulse edge leads to an error on the peak amplitude of only 0.05%. Fig. 2 shows the principle of the channel measurement. Fig. 3 gives the signal shapes in the different stages of the circuit.

With a 5th order low pass filter, the pulse appears only after a delay of about three time the time constant of the circuit. This delay is used to measure and to store the DC level of the dynode channel.

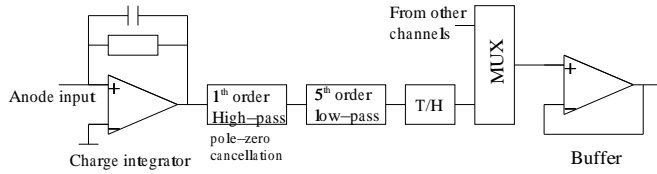


Fig. 2 : One channel architecture

The analog output waveform of the circuit is composed of 32 voltage steps. each step value corresponds to the maximum amplitude of one channel : 16 steps for the gain 1 followed by 16 steps for the gain 5 output. An example of output signal shape coming from the multiplexer output is given in Fig. 3.

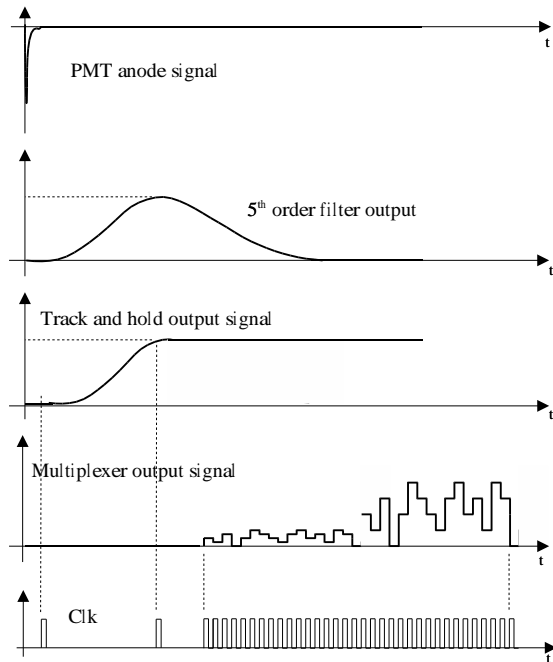


Fig. 3 : Circuit chronograms

The first clock pulse holds the DC value of the tagging channel (see next section). The second clock pulse holds the 16 analog values, and the 32 next pulses change the active multiplexer input. The delay of the second pulse must be adjusted to ensure the sampling of the analog pulses at their maximum.

The 16 to 1 analog multiplexer is in fact composed of four 4 to 1 multiplexers followed by a 4 to 1 multiplexer in order to reduce the load capacitance on each analog channel : each channel is loaded by only 4 switches in this case instead of 16.

In order to reduce the clock feedthrough, dummy transistors are integrated in the switch. In order to improve de dynamic range of the switch, it is composed of a CMOS pair. On this CMOS switch, dummy transistors are added at the input and at the output of the switch in order to minimize the clock feedthrough. The principle of the 16 to 1 multiplexer is given on Fig. 4.

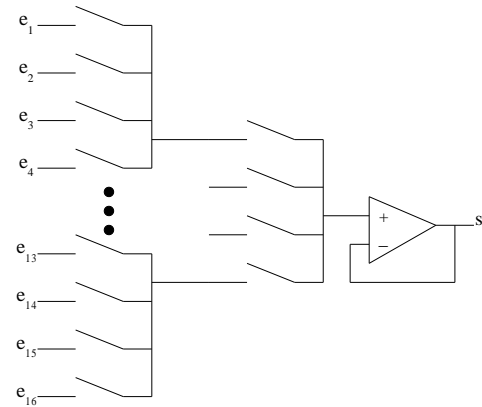


Fig. 4 : The multiplexer architecture

IV. THE TAGGING CHANNEL

The main goal of the tagging channel is to give a logic information on the status of the PMT in order to optimize the data acquisition. The tagging channel processes the signal coming from the last dynode. With this solution, the data acquisition system is able to read only the active PMTs.

On a PMT imager like the cherenkov ring imager of the AMS experiment, it is well know that the image formed on the PMT plane is composed mostly of black pixels that are not carrying any information. It is then interesting to reduce the amount of data transfer and processing by analyzing only active pixels. This information is provided by the tagging channel.

A. Data acquisition optimization

In order to make a data reduction, several solutions can be imagined :

–off chip data reduction : all the circuit outputs are sent to the data acquisition system (a DSP in this case), and the DSP performs the data reduction simply by analyzing and transferring only digital values greater than a threshold. This solution is the most simple for the chip design. But may overload the DSP.

–on chip channel tagging : this solution consists of having a threshold on each PMT channel measurement. This solution has several drawbacks : first, it increases the number of functions to be integrated on the chip and hence its power consumption. Second, it is very difficult to achieve the same threshold for each channel because of the gain spread of the PMT channels, without having additional gain factor one each channel.

–one tagging per PMT : This solution has been implemented on the chip. In order to have a common tagging for the 16 channels of the PMT, an additional channel, the tagging channel, has been added.

B. Auto-zero principle

Because the tagging channel has to give a logical information, it has a higher gain than the others channels. The integrating capacitor is five times smaller than for other channels, and the 5th order filter has a gain 3 times higher than the other channels. This results in a global gain 15 times larger than the other channels, which is necessary in order to toggle the logical output with an input close to 0.1 photo-electron. This higher gain also results in a larger offset voltage spread. The output of this spectrometry chain is compared to an internally generated threshold to give a logic level. The threshold is internally generated by adding the DC level to the external adjustable threshold to take into account the offset of the measurement chain. This DC offset is measured after the PMT pulse occurs and before the output pulse rises. This offset measurement is done on the first clock pulse according to Fig. 3. The channel's offset is then stored into a sample and hold circuit. The leakage of the sample and hold circuit is not a problem in this case, because the offset is measured each time a pulse occurs. This solution is much more simple than having a separate threshold tuning for each circuit. Furthermore, this cancels temperature drift and offset spreads of different stages. The block diagram of this channel is given on Fig. 5.

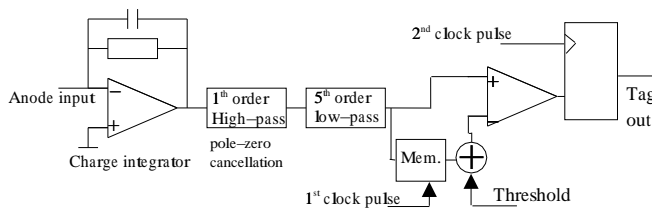


Fig. 5 : The tagging channel principle

V. LOGIC CONTROL

The glue logic controls the 16 to 1 analog multiplexer, the gain5/gain1 switch, the track and hold circuit of each channel and enables or disable the test mode. In order to reduce the number of I/O, the logic control has only three inputs : the clock, a reset and the test mode input. The logic control, is a simple state machine. At each clock edge, the output state changes so that each analog output is accessed. When the test mode is activated, the output of the state machine puts all the track and hold stages in the track mode

so that it is possible to probe the analog output of each channel in order to analyze each pulse shape. This mode can be activated in the calibration session in order to determine exactly the peaking time of the shaper for the hold delay adjustment.

VI. CHARACTERISTICS OF THE CIRCUIT

The circuit has been implemented into two technologies : One CMOS 0,6 μ m technology, and one BiCMOS 0,8 μ m rad hard technology. Particular attention was paid to minimize the noise coupling from the digital part to the analog one. The two parts of the circuit are separated and so are the power supply pads. The results are very similar for the two prototypes. Radiation measurement hardness were performed on the non rad-hard 0.6 CMOS prototype [7]. The circuit is optimized in order to have a power consumption as small as possible. Fig. 6 shows the integral non-linearity of one channel. This response shows that for small signals, the linearity is very good so that it is possible to use the single photo-electron response to calibrate the channel. The measurements of the single photo-electron response are done in conditions simulating the operating environment (with the multi-anodes PMT and pulsed LED light). Table I summarizes the main measured characteristics.

Table I : Circuit's characteristics

feature	measured	required
Power supply	-2 V ; +3 V	-
Power consumption	0.7 mW/channel	< 1 mW/channel
Input range	0-36 pC (250 photoelectr)	0-36 pC
Output range	0-2.8 V	-
Integral Non linearity	+/- 0.5% (gain 1) +/- 0.25% (gain 5)	< +/- 1%
crosstalk	< 10 ⁻³	2.10 ⁻³
I/O number	28 (without power supply pins)	-
Max. Clock freq.	1.5 MHz	1MHz
Noise	< 0,05 photoelectron RMS	0,1 photoelectron RMS

As discussed in the first section, a gain 5 has been implemented in order to calibrate a channel gain simply by analyzing the single photo-electron response. The Fig. 7 shows such a response.

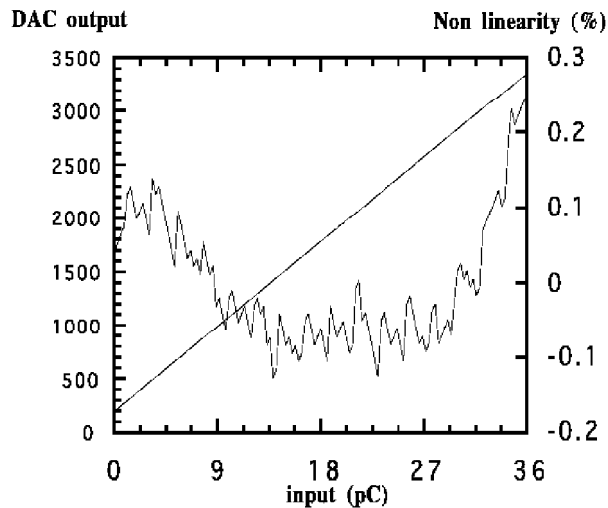


Fig. 6 : linearity and non linearity characteristics

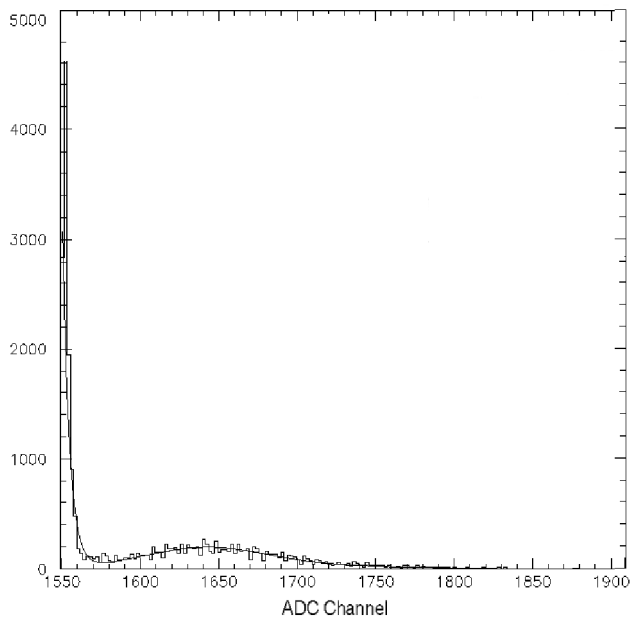


Fig. 7 : Single photo–electron response

The 0.6 μm CMOS technology prototype uses an area of 2.9x2.2 mm². The 0.8 μm BiCMOS technology prototype uses an area of 3.5x3.7 mm². The layout of the 0.6 μm CMOS technology prototype is shown on Fig. 8.

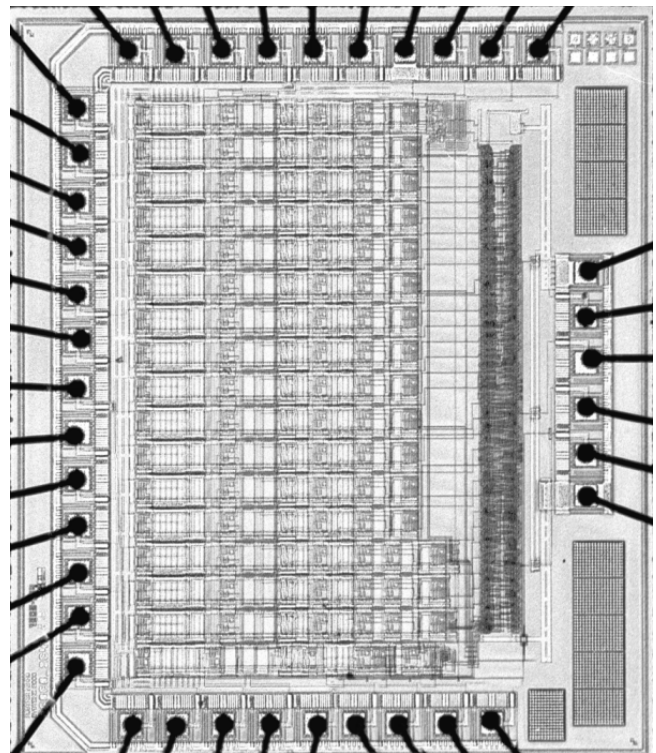


Fig. 8 : photograph of the chip

VII. CONCLUSION

These two prototypes were designed for the RICH detector of the AMS experiment. The test measurement are giving characteristics which satisfy totally the experiment requirements.

This circuit will be used on the prototype of the RICH detector. The linearity is good enough to calibrate the gain from the single photo–electron response, this linearity is better than the PMT one.

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