A low power, and low signal 5-bit 25 Msamples/s pipelined ADC for monolithic active pixels

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H. Ghazlane [2], D. Dallet [3]

***Abstract*– For CMOS monolithic active pixels sensor readout, we developed a 5 bit low power analog to digital converter using a pipelined architecture. A non-resetting sample and hold stage is included to amplify the signal by a factor of 4. Due to the very low level of the incoming signal, this first stage compensates both the amplifier offset effect and the input common mode voltage dispersion. The converter consists of three 1.5 bit sub-ADC and a 2 bit flash. We present the results of a prototype, comprising of eight ADC channels. The maximum sampling rate is 25MS/s. The total DC power consumption is 1.7mW/channel on a 3.3V supply voltage recommended for the process. But at a reduced 2.5V supply, it consumes only 1.3mW. The size for each ADC channel layout is only 43µm*1.43mm. This corresponds to the pitch of two columns of pixels, each one would be 20µm wide. The full analog part of the converter can be quickly switched to a standby idle mode in less than 1µs; thereby reducing the power dissipation to a ratio better than 1/1000. This fast power fall is very important for the ILC vertex detector because it renders the total power dissipation directly proportional to the beam low duty cycle.**

I. Introduction

MONOLITHIC active pixel sensors (MAPS) fabricated in CMOS technology offer several well known advantages for vertex detectors, high precision beam telescopes and imaging devices.

Granularity, flexibility, radiation tolerance, compactness, random access and fast read-out are among their most appealing characteristics. On the other hand, the associated readout electronics design is constrained in several aspects:

- The process used has to be chosen according to its particle detection performances (e.g. epitaxial layer thickness);
- The minimum readable signal may be very small (typically a couple of mV);
- The layout has to be adjusted to the (small) pixel pitch;
- The number of metal layers may be modest (4 or 5 only);
- And, of course, the power budget is a critical issue.

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The design presented here follows the requirements of pixel arrays designed at IPHC-Strasbourg in collaboration with DAPNIA-Saclay, in perspective of the Linear Collider vertex detector [1]. The arrangement of the pixel array with its associated read-out and A/D conversion stages is illustrated by figure 1.

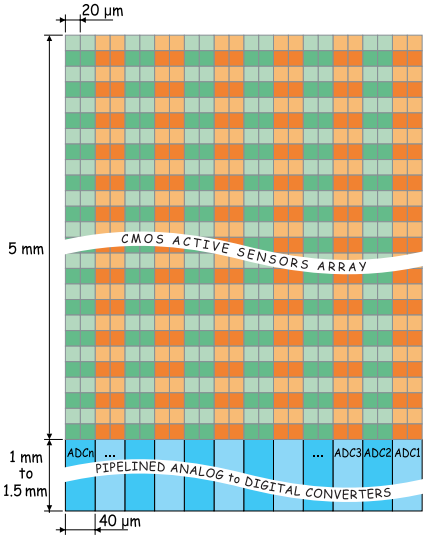

Figure 1: Sketch view of a MAPS array with a data conversion stage.

The IPHC develops fast sensors made of pixel columns read out in parallel, featuring an architecture allowing a frame read-out frequency in excess of 10 kHz. Each pixel hosts a micro-circuit providing a first pedestal subtraction (via correlated double sampling, i.e. CDS), eventually repeated at the end of each column [2]. Each column is presently ended with a discriminator, which will be replaced in future by an ADC.
The latter needs to fit the column width, which amounts to 25µm at present, and should become 20 microns in the next prototypes. The minimal signal delivered by each column is typically in the order of a mV, which translates into a first challenge for the read-out circuit design. Next comes the fast sampling rate ambitioned (10 MS/s). Finally, the power budget should remain as low as about 500 µW/column.

Due to the low value of the Least Significant Bit (LSB ~1mV), the design of the first stages of this converter is critical according to the offset and the signal to noise ratio.

With a sampling rate beyond 10 MHz, pipelined architecture is usually considered as good compromise because it requires less power dissipation and area than a full flash. An overview block diagram is shown in figure 2. [3], [4], [5].

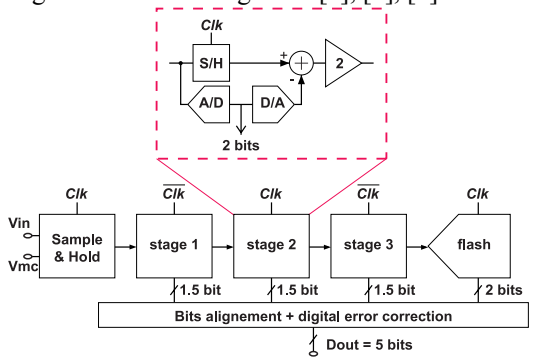

Figure 2: General block diagram of a pipelined converter.

The first stage samples and holds the analog input signal. It is followed by a set of pipelined stages. Each one produces a digital estimate of an incoming held signal, then converts this estimate back to the analog, subtracts the result from the held input; then this residue is amplified before being passed to the next stage. Eventually the last stage is a full flash that determines the least significant bits. The successive digital results from the pipelined stages are appropriately delayed throughout a bit alignment network. Then a digital correction stage helps to recover the errors due to the comparators offset. Therefore, low offset comparators are not necessary and the power consumption is reduced.
This paper describes hereafter each stage of this converter and we present some testing results.

II. The Sample and Hold Amplifier (SHA)

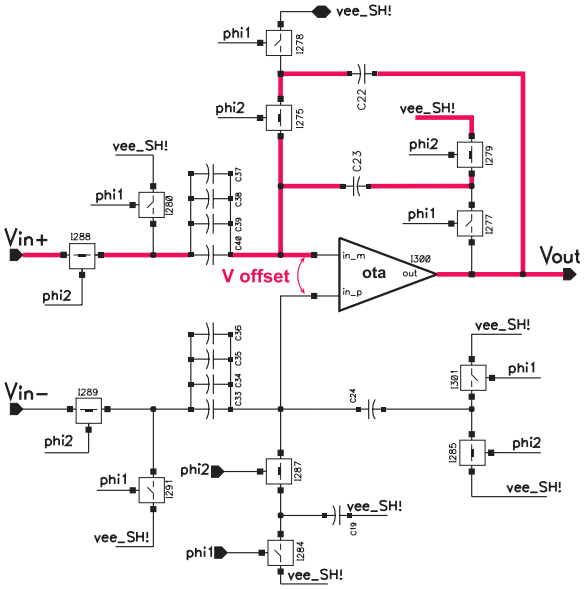

Figure 3: Sample and Hold Amplifier (SHA) scheme.

Charge redistribution non-inverting architecture is used. Figure 3 illustrates the sampling phase (phi2 is ON). "veeSH!" is the name for the virtual ground. The signal is stored onto the set of 4 sampling capacitors (C37...C40). Then during the HOLD (phi1), the charge is transferred to the feedback capacitor C23. This results into amplification by 4 of the differential signal between the reference (dark level) and the intensity level. Each capacitor unit is equal to 100fF.

A. Offset issues

The schematic used is not a full differential because the common mode feedback control that would be necessary is power or area consuming. Due to the low level of the signal, the pseudo differential scheme used is sensitive to the offset coming from different sources.

1) The Amplifier's offset

During the sampling phase (phi2) the amplifier's offset is registered on the feedback capacitor C_{23} and kept at the amplifier's input. Then the sampled signal will be $V_{in} - V_{offset}$. The previous held signal $Vout_{(n-1)}$ was stored on C_{22}. Thereby at the output of the amplifier it is maintained $Vout_{(n-1)} + V_{offset}$ which is not a reset value: this architecture is so called 'non resetting' SHA. During the HOLD phase (phi1), the charges are transferred from the sampling capacitors to the feedback capacitor C_{22} leading to an amplification in the ratio of the capacitors. Figure 4 shows the gain variation according to the input signal. It stays close to the optimal value of 4, when the OTA's offset parameter varies from -10 mV up to 10 mV. One can notice a worse case error of 2.5% for the smallest signal. It comes from the OTA finite open loop gain and also the parasitic capacitors effect. But this error is still acceptable for a 5 bit design.

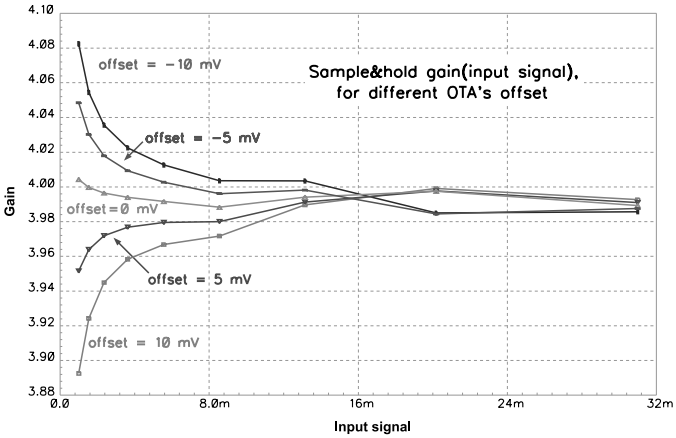

Figure 4: SHA gain according to the input signal, with the OTA's offset as a second parameter.

2) The charge injections offset

When the switches go to the "OFF" position, the charges coming from the transistors channel will create an offset that could be critical here since the capacitors are very small. This offset source is controlled using "non overlapping 4 phase clocks" which is not detailed in the figure 3 schematic for simplification reasons.

3) The pixels common mode voltage fluctuation

In figure 3 one can notice the symmetry between, the reference signal branch on one side going from node V_{in-} to the virtual ground "vee_SH!", and on the other side the intensity signal branch which is from node V_{in+} to the output node V_{out}. This symmetry reduces the fluctuation of the common mode level at the amplifier inputs even when the "dark level" from the pixel varies significantly.

4) The OTA's input parasitic capacitor effect

The finite value of the open loop gain makes this integrator, in the offset point of view, very sensitive to the parasitic capacitors at the OTA's inputs. This offset could easily shift the output signal out of the converter's dynamic range. The random value of some parasitic capacitors, will lead into a dispersion of the signal read by the following ADC. Hence during the layout design, a great care has been taken about the OTA's input nodes.

B. Noise issues

The KT/C noise is a critical parameter in this design due to the constraint of small value used for the capacitors to save surface. The input sampling capacitor is only 400fF which corresponds to a KT/C rms noise of 0.1 mV. Hence we have a safety margin of 1/10 between the rms noise and the minimum incoming signal. That ratio is large enough to maintain a quiet output code. We take care of the additional thermal noise of the OTA to not reduce significantly this robustness to the noise.

C. The OTA architecture

The amplifier designed for the SHA is used also for the converter multiplying stages. It is a telescopic cascode scheme as shown in figure 5. [6]

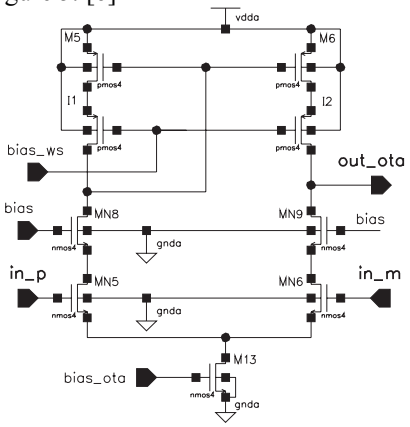

Figure 5: A wide swing telescopic OTA.

The current mirror load is a so called "wide swing cascode" [3]. It improves the dynamic range better than a basic cascode and makes robust the design for future low voltage version.

The Bode diagram simulations results on a 1pF load are shown in figure 6.

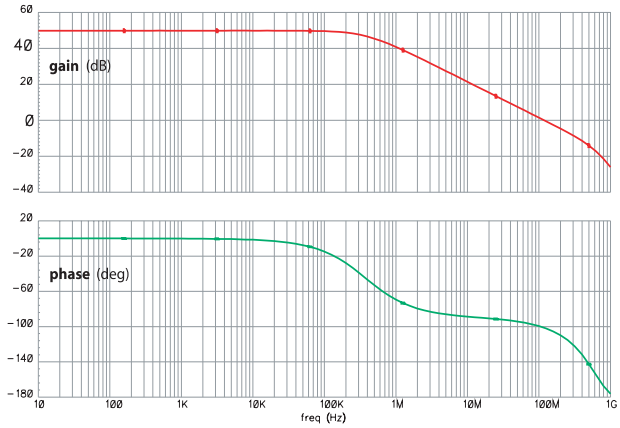

Figure 6: Bode diagram for the OTA on a 1pF load.

III. THE PIPELINED ADC

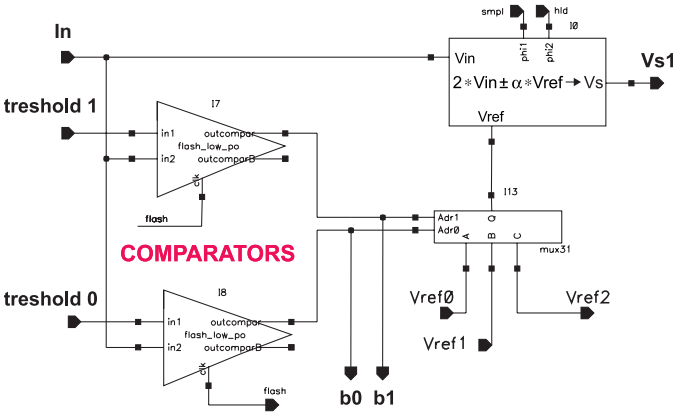

Figure 7: Bloc diagram of a 1.5bit sub-converter stage.

Fig. 7 illustrates the implementation of a 1.5 bit pipeline stage. The A/D block consists of two non critical comparators. The D/A conversion, subtraction, amplification, and S/H functions are performed by a switched capacitor circuit with a resolution of 1.5 bit per stage and an interstage gain of 2. Hence the transfer function of this stage is Vs=2*Vin-αVref where α = 0; or 0.5; or 1, depending on the output code (b0, b1). The transfer characteristic of a 1.5 bit stage is shown in figure 8 by the continuous line. The dashed lines show the possible variation of this characteristic depending on the comparators offset spread. The so called "1.5 bit" emphasizes that only 3 combinations out of the four are acceptable for the output codes. The (1, 1) code is avoided, thereby the interstage amplifier should not saturate and leaves room for the digital error correction.

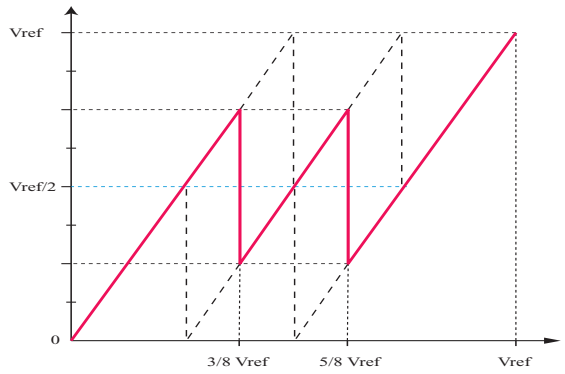

Figure 8: 1.5 bits residue transfer curve

This 1.5 bit configuration is particularly suitable to minimize the converter's total power dissipation because the amplifiers operate at a low closed-loop gain leading to a best settling time for minimum power consumption. Also this low gain per stage allows a maximum acceptable value for the comparators' offset, thereby once again low power latch architecture will be sufficient.

The maximum offset of these comparators is limited to Vref/4, where Vref = 4mV * 2^5 = 128mV is the full dynamic range. A simplified schematic of the comparator is given in figure 9. It is constituted by a low gain and low offset differential preamplifier followed by a latched folded cascode comparator [7].

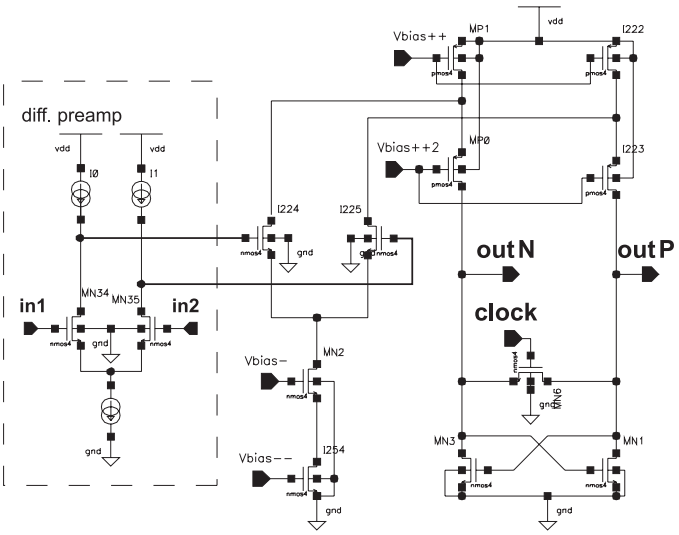

Figure 9: The comparator scheme.

A precise amplification by 2 is performed by two equal capacitors as shown in figure 10. The incoming signal is sampled during phase "phi1". It is amplified by charge redistribution during phase "phi2". During this amplification phase, the bottom plate of the sampling capacitor (C1) is connected to a reference voltage $Vref_i$ which will be subtracted from the amplified signal. The residue resulting from this operation is transmitted to the next pipe line stage. The value for $Vref_i$ is respectively 0 or 0.5*Vref or Vref depending on the comparators outputs (see figure 7). Vref is the dynamic range of the converter, with reference to the virtual ground.

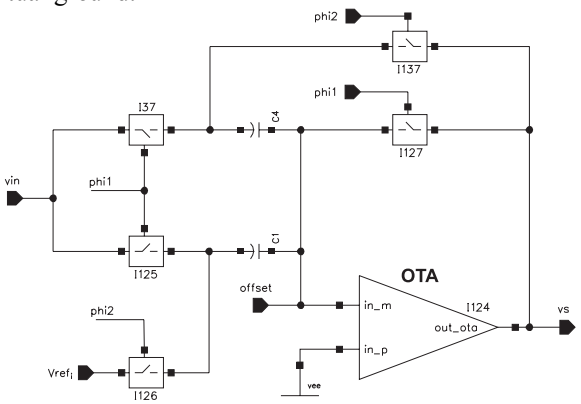

Figure 10: The capacitive precise multiplier scheme.

A prototype has been designed in a CMOS 0.35µ process from Austria Micro System. It includes 8 channel of this ADC. The layout is shown in figure 11. The dimensions of one full channel including the sample & hold stage is 43µm*1.43mm. One may notice also that the area occupied by the digital error correction stage is quite 1/5 of the full channel.

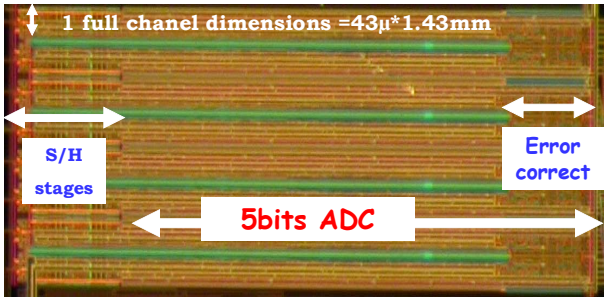

Figure 11: Layout of a prototype with 8 channel ADC.

IV. TESTING RESULTS

The circuit has been tested successfully up to 25Mhz. This sampling rate and the power dissipation are summarized in the table 1 for two different power supply values (3.3V and 2.5V). The sample & hold consumption is given specifically to help in comparison with other ADC designs.

	Sample & Hold	5 bits ADC	Full channel
Sampling rate	25 Mhz	25 Mhz	25 Mhz
Dimensions	43 µ * 250 µ	43 µ * 1250 µ	43 µ * 1500 µ
Power@3.3V	0.413 mW	1.287 mW	1.7 mW
Power@2.5V	0.313 mW	0.975 mW	1.288 mW

Table 1: Power consumption and sampling rate testing results.

The DNL and INL were measured for a 1 MHz sinus input signal, and the results given in figure 12 [8].

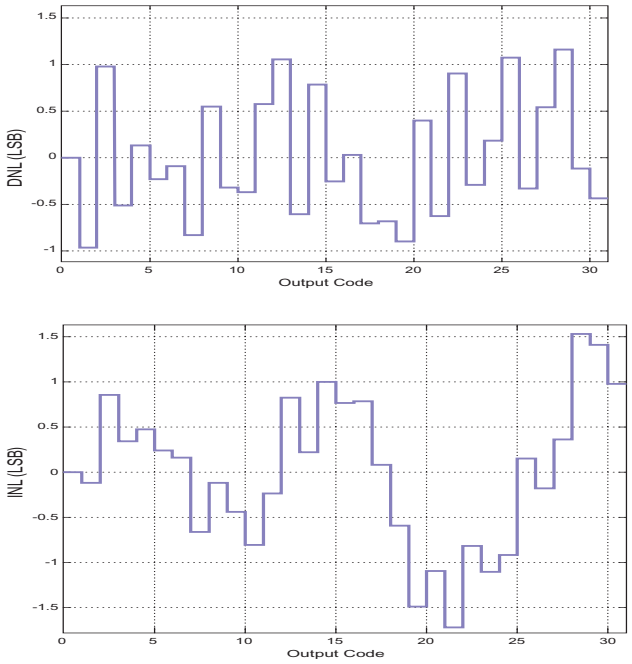

Figure 12: Non linearity results.

For the next ILC experiment, the beam duty cycle will be very low (~1%). Therefore a very useful idea to reduce the total power dissipation is to switch on the analog part of the circuit only when it is used, rendering the total power dissipation directly proportional to the beam low duty cycle. This circuit includes such a very fast and very efficient "power ON" capability. The testing result is given in figure 13.

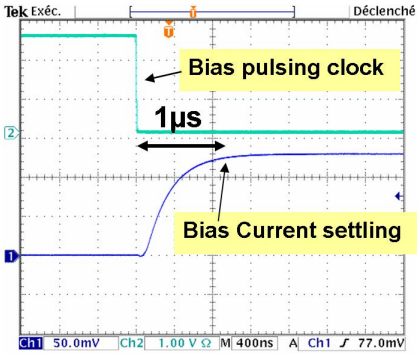

Figure 13: Bias fast pulsing results.

From the falling edge of a pulsing clock, the bias current is settled after only 1µS in the worst case. In the standby idle mode (pulsing clock at high level), the full analog part of the converter is switched OFF and the analog power dissipation is reduced to a ratio better than 1/1000.

V. CONCLUSION

The design of a 5 bit pipelined ADC has been reported, featuring the low level signal required for monolithic active pixel sensors. It is one of the possible candidates in perspective of the future International Linear Collider vertex detector. It includes a sample and hold stage, and the converter had 1.5 bit/stage with a non differential architecture. The layout deals with the pitch of the pixels array. The size of each channel layout is 43µm*1.43mm. We are still working to reduce the length of this converter's layout in our next version. A very efficient fast power pulsing is integrated with this circuit and that help to make the power dissipation directly proportional to the beam duty cycle.

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