Large Silicon Tracking Systems for ILC: Role, Design and Main issues

A. Savoy-Navarro

2005 International Linear Collider Workshop – Stanford, U.S.A.

Large Silicon Tracking Systems for ILC: Role, Design and Main issues

Aurore Savoy-Navarro
LPNHE-Universités de Paris 6 et 7/IN2P3-CNRS, Paris, France

The roles, the designs, the main issues and the current status of the R&D on large Silicon Tracking Systems for the ILC are discussed in this paper. The R&D work presented here is performed within the SiLC (Silicon tracking for the Linear Collider) R&D Collaboration.

1. TRACKING IN THE TWO DETECTOR CONCEPTS

The ILC detector concepts differ mainly by their tracking strategy; the aim here is to show that the Silicon trackers play an essential role whether or not there is a gaseous central tracker, and that the R&D issues with regards to the Silicon devices are common. This is the motivation of the R&D activities conducted within the SiLC collaboration [1].

In the LDC and GLD concepts, the tracking is essentially achieved by the TPC and the microvertex. Instead, in the SiD concept, the tracking is all based on Silicon technology, and this Silicon-tracking system acts as a ''sagitter'' linking the microvertex to the Si-W calorimeter. The question in this case is: do we need more from this tracker? People are getting more and more convinced that the Silicon tracking system in the SiD design needs to be optimized in terms of number of layers, strip orientation and of the requested performances. Likewise, in the LDC and GLD concepts, the idea of introducing layers of Silicon strips in the internal and external parts of the central and forward regions is recognized as a relevant one. It leads to the concept of the Silicon Envelope [2] that surrounds the TPC, with the four components listed before. The crucial reasons for doing so are: to ensure the robustness of the overall tracking system, to have a full coverage and to improve the tracking performances.

2. COMPONENTS OF THE SI-TRACKING SYSTEM: ROLE AND CURRENT DESIGN

Two main regions must be considered, namely: the central barrel and the forward regions

2.1. Si-tracking components in the central barrel

If there is a TPC as a central tracker, two designs are proposed for the innermost layers. One is the present LDC design that includes only two double-sided layers, linking the microvertex, with an expected spatial resolution of the order of 2 to 3 μm, to the TPC, with a spatial resolution of the order at best of 50 to 80 μm. This design resembles the inner Silicon tracking (ISL) in CDF. These intermediate Silicon layers should have 50 μm readout pitches, 200 μm thicknesses and should provide a spatial resolution of the order of 7 μm. They improve the momentum resolution by about 30%, give the possibility to detect secondary vertices of long lived particles, and allow the tracking to cover down to 25° with respect to the beam axis. Detailed simulation studies tend to prove that occupancy rates could be well sustained by up to 30 cm long strips without any problem. It would drastically reduce the number of electronic channels on detector to a total of 200 or 300 thousands channels. In the case of the first layer, sitting after the microvertex at

about 16cm in radius, it would permit to locate the electronics at its both ends. A similar design could be applied to the two first layers in the SiD central tracking system.

The GLD concept has a somewhat different design for this component. Namely the intermediate tracker is made of 5 double sided Silicon layers and thus this component acts more like a real tracker than like a simple 'linker' device. Indeed this design reminds of the central Silicon tracker (SCT) in the ATLAS experiment.

However, a few external Silicon layers were proposed to be added in the current LDC design in order to better link the central tracker with the calorimeter [2]. In order to optimize these detector performances, the best design was proven to be the one made of 3 layers: two single sided layers with a double-sided one in between. The ensemble of devices comprising the microvertex, the internal Silicon layers, and those additional external layers provides an independent track finding, thus redundancy and liability (safety) and also alignment, calibration and distortions handling.

There are two alternative basic module designs for the central outer Silicon layers. SiD explored first very long strips and now favors tiles [3]. The current LDC design is based on 60 cm long strips maximum that could also be used for the SiD outer layers. The advantage of this medium size strip solution is the reduction of electronic channels and thus of the power dissipation. Besides, modules made of those medium size strips are not difficult to assemble (especially with 8 inches sensors) and they are well suited to the low occupancy rates at these large radii.

2.2. Si-tracking components in the forward region

The forward region is a key-region for the Physics at the ILC. It is therefore mandatory to have a highly performing tracking system at large angle. The overlap between the central and the forward parts of the tracking system must be studied with great care in order to avoid dead tracking regions or a dramatic increase of material budget in these zones.

The inner forward Silicon tracking component is very similar in each detector concept. Its angular coverage with respect to the beam axis extends roughly from 25° down to a few degrees. The TPC does not help in this region, and thus the tracking only relies on Silicon layers, including the microvertex. But the TPC end caps increase the material budget in a region which is already rather touchy and this is a weak point of the LDC or GLD designs in this region.

The SiD design foresees 4 disks nearby the microvertex, at these small angles. It is rather similar to the LDC design where there are 7 disks: the 3 first disks are made of pixels of 50 µm by 300µm (as ATLAS microvertex device), and the four following ones are made of projective strips.

The current studies for this component concentrate on the cooling system and on the possibility to use other pixel technologies in particular in the first 3 or 4 layers near the microvertex, CMOS or DEPFET sensors could be used. In addition the cooling studies in this zone should dedicate a particular attention to minimize the material budget.

If there is a TPC, the forward outer component can be designed in the two following ways; one possibility is by squeezing this component between the TPC end cap and the forward calorimeter, as in the current LDC baseline design. The counterpart is that the tracker acts as a simple linker and not a real tracker in a region where tracking is barely needed. Thus the second possibility is to decrease the length of the TPC by about 40 cm on each side and to extend the tracking device by the same amount. It thus provides a sufficient level-arm to achieve a real tracking. Detailed simulations are needed to optimize those crucial dimensions. The design of these layers as presented at this

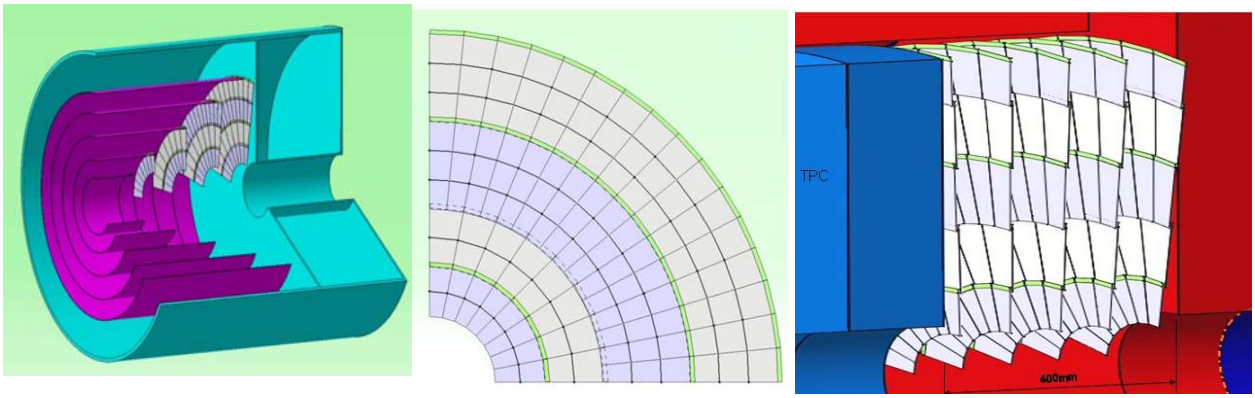

Figure 1: Projective design of the end cap Silicon layers (middle view), and their integration in the SiD concept (left) or in the LDC or GLD concepts (right)

Workshop is based on a projective geometry, shown in Figure 1 here above. This is the type of geometry used in the forward disks for the ATLAS or CMS experiments at the LHC. But in the case of the ILC, the radius length to be covered by those disks is much larger, typically of the order of 1m to 1.30 m length, whereas it is much shorter in the LHC case (only about 30 cm). Therefore ten different sizes of trapezoidal sensors are needed to achieve the detector design shown in Figure 1; this could be a bit inconvenient for both the sensor fabrication and the detector assembly. An XUV alternative geometry is under study. It is based on a single sensor type and it is therefore attractive for this reason. The CAD designs of both geometries are underway and will be carefully compared with detailed simulations.

Both designs can be applied to the SiD case for the external forward layers as shown in Figure 1 (left side). The performances in the forward region are a key point when comparing the two detector concepts.

3. MAIN ISSUES

There are a number of common issues for both detector concepts, namely with or without a TPC, among which:

The detector modules and the sensors, including the R&D on sensors and their characterization

The cooling, i.e.: the thermo mechanical studies to design the needed cooling system if any needed.

The front-end and readout electronics associated to these detectors

The material budget issues and the ways to overcome it.

The integration issues

The detailed simulations

3.1. The sensors and detector elementary modules

The detector module can be made of a single sensor (tile) (see Tim Nelson's talk [3]). or a few sensors bonded to each other in order to make a module with longer strips. In any case the main issue is to have larger wafers, of 8 inches at least, in order to reduce the number of sensors to be bonded together, typically to 2 to 3, or else, in order to have a size suitable for a detector architecture based on tiles. Furthermore one would like to have thinner wafers and/or to apply thinning technique as well, in order to reduce the material budget with, at the same time, a small pitch for good spatial resolution.

Various types of sensors and modules might be considered depending on the location of the Silicon tracking components and of the required performances. Different shapes such as for instance trapezoidal sensors for the forward detectors built for LHC experiments or R-Phi sensors in the case of the VELO detector of LHCb are already available on the market. Also under consideration, there is the possibility to use only one type of sensor, a "universal tile", for constructing the entire Silicon tracking system; these two alternative solutions are presently under study.

An important issue is to characterize the sensor properties in order to be able to check the new types of sensors and also to ensure later on the follow up of the production as provided by the Industrial firm when building the Silicon detectors. Most of the Labs are now equipped with test benches that permits detailed studies of sensor and detector prototype performances by exciting the Silicon substrate with a laser diode in the infra red to scan the detailed structure properties of the sensor, and a radioactive source to measure in particular the Signal/Noise ratio.

3.2. Thermo-mechanical studies

In order to tackle the primordial quest for low material budget, thermo mechanical studies are undergoing on prototypes of the various components of the Silicon tracking system. The present achieved results demonstrate that air convection is sufficient to ensure the proper cooling in the outer parts of the central or the forward components. The study of the internal central and forward components is now starting and it needs information about the environmental conditions in those regions which are of course trickier from several points of view.

3.3. Front-end and Readout Electronics

The front end and readout electronics is an essential item and lot of progress was achieved this last year (see LCWS04 Proceedings). Let us first remind what are the main goals to be achieved: low noise preamplifier, a shaping time from 0.5 to 5 µs, very low power dissipation, highly shared ADC, digitization and sparsification on detector, power cycling, compact and transparent device. For many of these reasons the choice was made by the LPNHE-Paris team to go to deep sub micron (DSM), 0.18 µ CMOS UMC technology for the first prototype. The layout was ready and sent to foundry by end of November 2004 (see Figure 2, left side). The chips (Figure 2, right side) were delivered by end of February 2005. The preliminary test results are very promising (see J.F. Genat's presentation [4]).

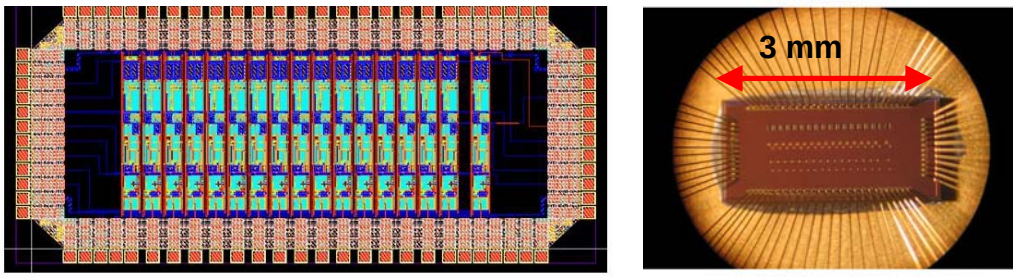

Figure 2: LPNHE front end layout: 16 + 1 channels (left side), and chip delivered by the foundry (right side)

3.4. Material Budget

The material budget or the "slimness" is a main focus in this R&D. There are various ways to overcome this problem and they are under study on both the mechanical and the electronics sides. This implies the optimization of the support structure, the choice of the materials, the detector architecture (integration included), the use as much as possible of passive cooling, and the electronics on detector made in DSM technology, the cabling and the connection issues.

To tackle these problems we are taking advantage of the technological advances in these high tech related issues and also we benefit from all the R&D work performed for Tevatron II, for the LHC and now in the SiLC framework.

3.5. The other common issues

To go ahead there are now three major issues:

The setting up of a test beam with a realistic detector prototype by the end of 2006.

The design, layout and production of the next front-end readout chip that should also be used to equip the detector prototype in the test beam (about 10,000 readout channels).

The detailed simulation studies GEANT4 based, to compare detector designs and detector concepts from the point of view of their tracking and physics performances and in the full detector acceptance.

All these issues are undergoing now within the R&D collaboration.

To conclude this brief and thus incomplete review, let us stress that Silicon tracking systems are essential whether or not there is a central gaseous tracker. The LDC and GLD designs need Silicon tracking for at least two crucial reasons: robustness and overall angular coverage. This will greatly improve their overall tracking system. In the SiD case, there is a need for a highly performing all Silicon tracking system and not only a simple "track linker". Therefore, both detector concepts need highly performing Silicon trackers with similar conceptual designs. All the related R&D aspects that we briefly mentioned in this paper are addressed within the SiLC collaboration.

Acknowledgments

The author wish to thank all the collaborators from SiLC, i.e.: University of Michigan, UCSC and SCIPP-UCSC, IMB-CNM/CSIC, DPNC University of Geneva, University of Helsinki, IEKP Karlsruhe University, Moscow State University, Obninsk State University, Charles University in Prague, IFCA University of Cantabria, IHEP Austria Academy of Science in Vienna, Consortium of Korean Universities, Tokyo University and HAMAMATSU Co., and J. Brau, M. Breidenbach, W. Cooper, M. Demarteau, J. Jaros, T. Nelson and H. Weerts for fruitful discussions. And special thanks to the LPNHE team.

References

[1] T. Blass et al, "SiLC: Silicon tracking for the Linear Collider, Status report", PRC R&D 03-02 updated 03-02 (05), DESY-Hamburg, May 2005, and references therein. And see also: http://www.desy.de/prc/html/documentation.htm

[2] J.E. Augustin et al., "A Silicon Envelope for the TPC", LC Internal Note, LC-DET-2003-013, October 2003. See also: http://www-flc.desy.de/lcnotes

[3] T. Nelson, “Silicon Tracker Design for the ILC”, LCWS’05, SLAC, March 2005.

[4] J.F. Genat, “Front-End Electronics for Large Silicon Trackers”, LCWS’05, SLAC, March 2005.