A very-front-end ADC for the electromagnetic calorimeter of the International Linear Collider

G. Bohner, R. Bonnefoy, R. Cornat, Pascal Gay, J. Lecoq, S. Manen, L. Royer

A very-front-end ADC for the electromagnetic calorimeter of the International Linear Collider

Gérard Bohner, Roméo Bonnefoy, Rémi Cornat, Pascal Gay, Jacques Lecoq,
Samuel Manen, Laurent Royer

***Abstract*— A 10-bits pipeline Analog-to-Digital Converter (ADC) is introduced in this paper and the measurements carried out on prototypes produced in a 0.35 μm CMOS technology are presented. This ADC is a building block of the very-front-end electronics dedicated to the electromagnetic calorimeter of the International Linear Collider (ILC). Based on a 1.5-bit resolution per stage architecture, it reaches the 10-bits precision at a sampling rate of 4 MSamples/s with a consumption of 35 mW. Integral and Differential Non-Linearity obtained are respectively within ± 1 LSB and ± 0.6 LSB, and the measured noise is 0.47 LSB at 68% C.L. The performance obtained confirms that the pipeline architecture ADC is suitable for the Ecal readout requirements.**

***Index Terms*— ADC, pipeline, CMOS integrated circuit, comparator, differential, amplifier, ILC, CALICE, calorimeter, very-front-end electronics.**

I. Introduction

THE Electromagnetic Calorimeter (ECAL) of the International Linear Collider (ILC) requires a performant very-front-end readout electronics which implies an ambitious R&D inside the CALICE collaboration [1]. This integrated electronics has to process 10^8 channels which deliver a 15-bits dynamic range signal with a precision of 8 bits. Moreover, the minimal cooling available for the embedded readout electronics imposed an ultra-low power limited to 25 μW per channel. This issue will be reached thanks to the timing of ILC which allows the implementation of a power pulsing with a duty ratio of 1% .

A key component of the very-front-end electronics is the Analog-to-Digital Converter (ADC) which has to reach a precision of 10 bits. In order to save the die surface of the chip and to limit the power consumption, one ADC will be shared by several channels. To fullfill this request, an ADC operating at a sampling rate of the order of one MSamples/s has been designed.

This paper presents the design and the performance of a 35-mW 4-MSamples/s 10-bits ADC. After a description of the 1.5-bit per stage architecture, the gain-2 amplifier and comparator are detailed. Measurement results of the engineering samples fabricated in a 0.35 μm CMOS technology are then reported.

II. 1.5-bit/stage pipeline ADC architecture

Among the various efficient ADC architectures developed and improved last tens years, the pipeline architecture is adapted to reach high resolution, speed and dynamic range with relative low power consumption and low component count. Typically, resolutions in the range of 10-14 bits at sampling frequency up to 100 MSamples/s are achieved in CMOS technologies with power lower than 100 mW [2]–[4].

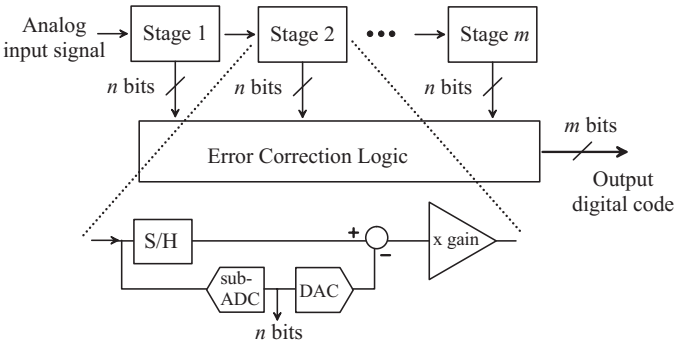

Fig. 1. Conventional *m*-bits pipeline ADC architecture with *n* bits delivered per stage.

The block diagram of a conventional *m*-bits pipeline ADC [5] with *n* output bits per stage is given in Fig. 1. Each stage consists of a sample-and-hold (S/H), a low-resolution *n*-bits flash sub-ADC, a substractor and a residue amplifier. This stage converts the input voltage into the corresponding *n*-bits code and provides the amplified residual voltage to the next stage. The complete *m*-bits system consists in piling up *m* stages and in adding an Error Correction Logic block which delivers the final digital code.

The simplest architecture is designed with a resolution of 1 bit per stage. In such basic ADC, each sub-ADC is composed of one comparator, with the reference signal V_{REF} fixed at the middle of the analog input dynamic ADC range, and the gain of the residue amplifier is 2. The algorithm for the i^{th} stage is as follows: if $(V_{In})_i > V_{REF}$ then $b_i = 1$ and $(V_{In})_{i+1} = 2(V_{In})_i - V_{REF}$, else $b_i = 0$ and $(V_{In})_{i+1} = 2(V_{In})_i$, where $(V_{In})_i$ is the input voltage of the i^{th} stage and b_i the output bit of this stage.

The accuracy of this type of ADC is limited by three main [6]–[8] parameters :

- the interstage gain 2 accuracy limited by the gain-bandwidth product of the amplifier and the mismatch of its feedback components;
- the offset voltage of the comparators caused by the mismatch of components of its input stage;
- the thermal noise which varies between samples. The noise contribution of the sampling in each stage, represented by the kT/C expression, is generally predominant

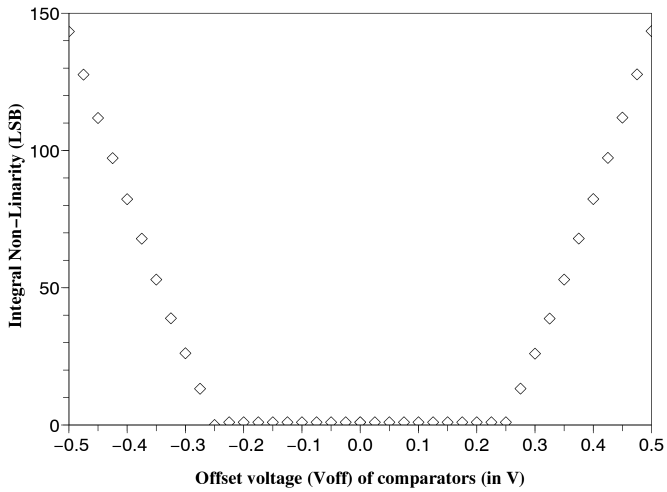

Fig. 2. 1.5-bit/stage ADC: variation of INL as a function of offset voltage Voff on comprarators.

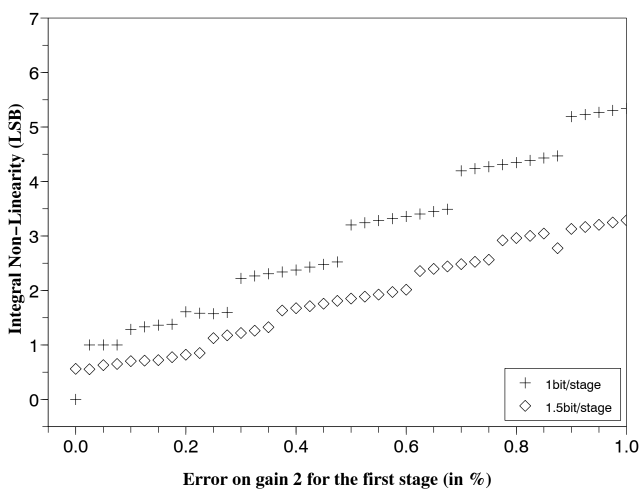

Fig. 3. Comparative variation of INL versus error on gain 2 of the first stage amplifier, for 1-bit/stage (cross) and 1.5-bit/stage (diamond) ADC architectures.

but this noise contribution of a latter stage is effectively attenuated by the gain of the previous stage.

An architecture with a resolution of 1.5 bits per stage is a solution to attenuate the contributions of the gain error and offset voltage to the non-linearity of the ADC. The Integral Non-Linearity (INL) obtained with algorithmic simulations is displayed on Fig. 2 and Fig 3. The Integral Non-Linearity refers to the deviation, in LSB, of each individual output code from the ideal transfert-function value. Fig 2 shows that, for an input dynamic range of 2V, the INL of the ADC is not affected by the offset voltage V_{off} of the comparators up to $\pm 250\,\mathrm{mV}$. Moreover, as reported in Fig 3, the precision is less sensitive to the gain 2 accuracy with the 1.5-bit/stage architecture compare to a basic 1-bit/stage one.

This 1.5-bit/stage pipeline ADC architecture [9] involves two comparators per stage, with separate threshold voltages V_{Th}^{Low} and V_{Th}^{High}, and two reference voltages V_{Ref}^{Low} and V_{Ref}^{High}. A 2-bits word $[b_2 b_1]_i$ is delivered by each stage *i*. The corresponding algorithm is given by:

- if $(V_{In})_i < V_{Th}^{Low}$ then $[b_2 b_1]_i = [00]$ and $(V_{In})_{i+1} = 2(V_{In})_{i+1}$
- if $V_{Th}^{Low} < (V_{In})_i < V_{Th}^{High}$ then $[b_2 b_1]_i = [01]$ and $(V_{In})_{i+1} = 2((V_{In})_i - V_{Ref}^{Low})$
- if $(V_{In})_i > V_{Th}^{High}$ then $[b_2 b_1]_i = [10]$ and $(V_{In})_{i+1} = 2((V_{In})_i - V_{Ref}^{High})$

III. Schematic of One Stage

The global schematic of one ADC stage with resolution of 2 bits is given on Fig. 4. In order to reject the common mode noise, a fully differential structure has been adopted. In the very-front-end electronics of the electromagnetic calorimeter of ILC, the differential mode is particularly relevant considering the presence in the chip of a digital electronics which could induced common mode noise into the analogue part. Since the captor delivers a common mode signal, a common-mode to differential-mode conversion is required before the digitalisation stage. This interface should be inserted as soon as possible during the analogue processing of the signal in order to take advantage of the improvement signal-to-noise induced by the differential mode.

As represented on Fig. 4, the value of the reference signal added to the $(V_{In})_i$ input signal is selected by comparators outputs through switches. Then the circuit operates on two clock phases: during the sampling phase, the input signal and the reference signal are summed through capacitors 2C, while during the hold phase, the summed signal is amplified by factor 2.

A. *The gain-2 amplifier*

The gain-2 amplifier is built with a differential amplifier and a capacitive feedbacked loop. A better matching is obtained with capacitors and they have been preferred to resistors [10]. This matching is particularly important because it affects the precision of the gain 2, and therefore, the linearity of the ADC. Thus, feedback capacitors must be large enough to minimize both the thermal noise kT/C and the components mismatch proportional to $1/\sqrt{C}$. In contrast, both the small die surface and the dynamical performance achieved with low supply current have to be carry out. Then capacitors values of 300 fF and 600 fF are used. To match these components with the precision required of 0.1%, the capacitors array has been drawn using a common-centroid layout composed of six poly-poly capacitor unit cells of 300 fF each. Dummy switches have been introduced in order to counterbalanced the parasitic capacitors introduced by the reset switches.

B. *The operational amplifier*

As represented in Fig. 5, the operational amplifier is based on a fully differential architecture with rail-to-rail inputs and outputs [11]–[15]. It includes a resistive Common Mode FeedBack circuit (CMFB) to control the common mode output voltage.

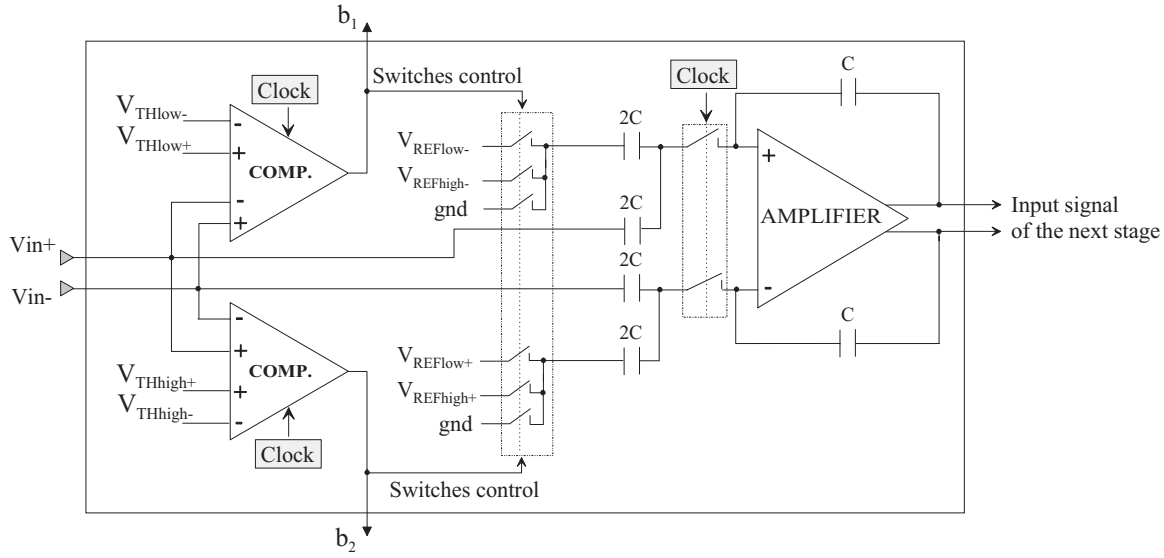

Fig. 4. Simplified schematic of one ADC stage: 2 comparators give the output bits of the stage and determine the reference signals substracted to the input signal; the amplifier amplifies by a factor 2 the redidual voltage and delivers it to the next stage.

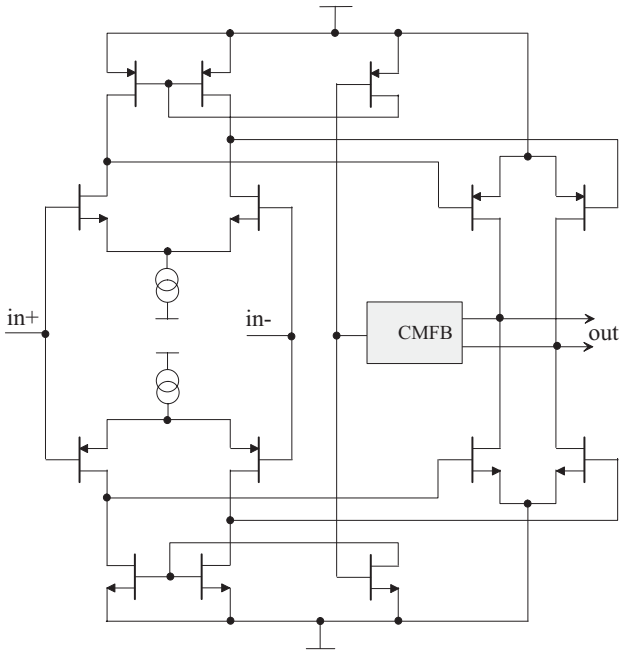

Fig. 5. Simplified schematic of the differential operational amplifier: the input and output stages are differentail and rail-to-rail, with a required Common Mode FeedBack block to fix the output common mode voltage.

TABLE I
OPEN LOOP AMPLIFIER CHARACTERISTICS.

Power supply	5.0 V
Consumption	1.9 mW
Gain-Bandwidth	50 MHz
Differential phase margin	66 $\pm$ 3 degrees @ 68% C.L.
Common Mode phase margin	66 $\pm$ 5 degrees @ 68% C.L.

The main characteristics of the open loop amplifier are reported in the table I.

This table shows that despite a large gain-bandwidth product of 50 MHz, the consumption is limited to 1.9 mW with a 5V power supply.

The design of the differential amplifier must guarantee a stable behaviour of the gain-2 feedback amplifier over process parameters fluctuations. Both differential output signal and common mode output signal must be stable with a total load capacitance evaluated to 1 pF. On that purpose, a pole-zero compensation network is connected at the differential output and its parameters adjusted. Then, stability simulations give a phase margin better than 66 degrees for both differential and common mode signals. Statistical simulations with process parameters fluctuations give standard deviation of 3 degrees and 5 degrees respectively for differential and common mode phase margins.

C. The comparator

As represented on Fig. 6, the comparator consists on a latched comparator [16] followed by a dynamic memory. This architecture is fully differential with two differential inputs: one for the differential signal $(V_{In})_i$ from the previous stage and one for the differential reference signal. However, for simplicity, only one differential input is represented in Fig. 6. The very high impedance of the load represented by the latch gives the very high sensitivity of this comparator. The high gain is reached when the switch of the latch is open, leading the latch output to switch into a logical state corresponding to the sign of the differential input voltage namely $(V_{In})_i - V_{Ref}$. The intrinsic sensitivity of this comparator is so high that the sensitivity is finally dominated by the input comparator noise.

The characteristics of the designed comparator are summarized on the table II.

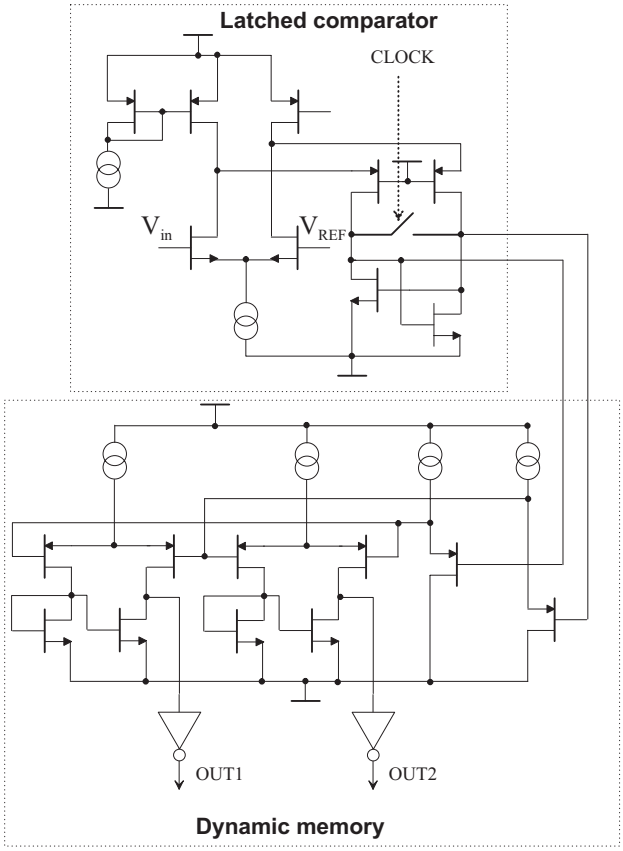

Fig. 6. Simplified schematic of the comparator, separate into parts: the latched comparator triggered by a clock signal and a dynamic memory with two complementary digital outputs.

TABLE II

COMPARATOR CHARACTERISTICS.

Power supply	5.0 V
Clock frequency	4 MHz
Consumption	815 μW @ 4 MHz
Sensitivity	$<$ 300 nV @ 68% C.L.
Input noise	$<$ 280 μV @ 95% C.L.
Offset	20 $\pm$ 9 mV @ 68% C.L.

IV. MEASUREMENT RESULTS

A 10-bits ADC prototype has been fabricated using the Austriamicrosystems 0.35 μm 2-poly 4-metal CMOS process. The total area of the ADC is 1.35 mm^2 and the chip is bounded into a JLCC 44 pins package. The circuit is measured with a 5.0 V supply and a differential input swing of 2.0 V_{pp}, at a frequency clock of 4 MHz.

Main performance is reported on table III. A dynamic input range of 2.0 V is measured with zero and gain errors respectively of 0.5 % and 0.8 % of the full scale. The standard deviation of the noise is lower than 0.5 LSB at 68% C.L.

The static linearity curves of the 1.5-bit/stage ADC are given in Fig. 7 and Fig. 8.
The Differential Non-Linearity (DNL) is displayed in Fig. 7. This error is defined as the difference between an actual step width and the ideal value of one LSB. The DNL measured is

TABLE III

SUMMARIZED PERFORMANCE OF THE PIPELINE ADC.

Architecture	1.5-bit/stage
Technology	0.35μm 2-P 4-M CMOS
Area	1.5 mm x 0.9 mm
Supply Voltage	0-5 V
Resolution	10 bits
Full scale	2 V differential
Sample rate	4 MS/s
Consumption @ 4 MHz	35 mW
INL	+0.85/-0.70 LSB
DNL	+0.56/-0.46 LSB
Noise	0.47 LSB @ 68% C.L.
Gain Error	0.8% of full scale
Zero Error	0.5% of full scale

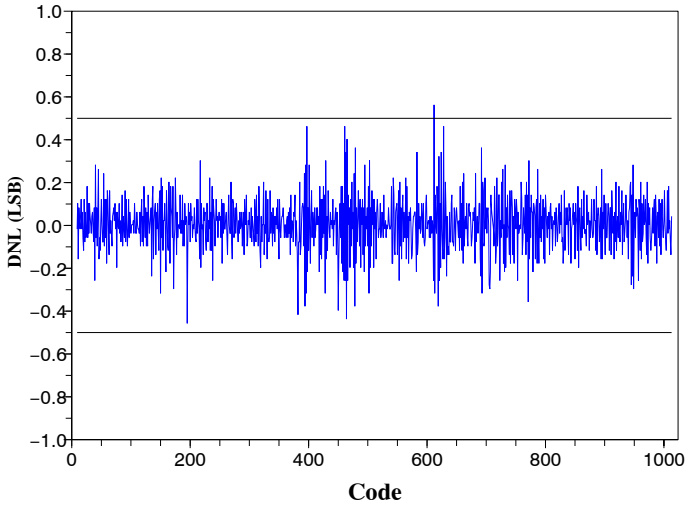

Fig. 7. Differential nonlinearity measurement

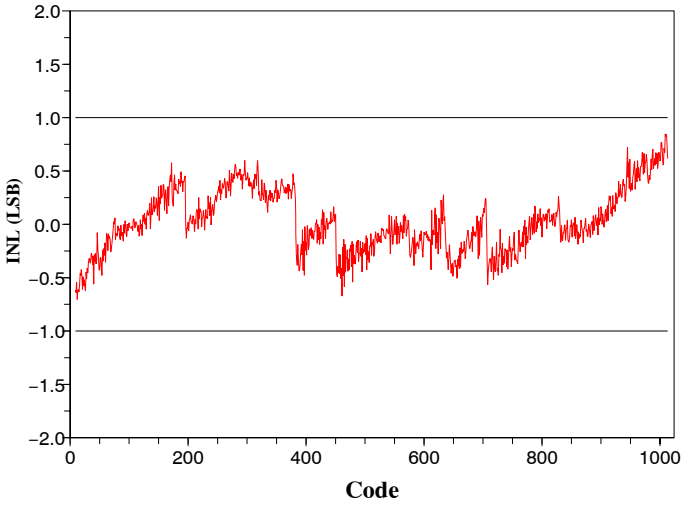

Fig. 8. Integral nonlinearity measurement

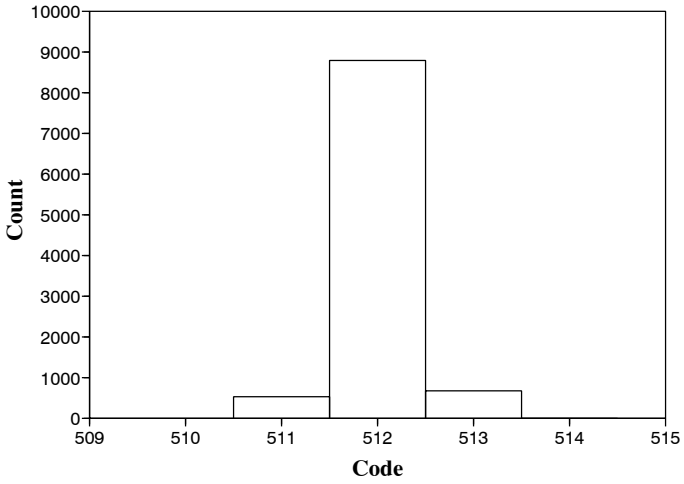

Fig. 9. ADC code occurence histogram at the code centre

within a ± 0.6 LSB range.

The Integral Non-Linearity curve plotted in Fig. 8 never exceeds +0.85/-0.70 LSB over the 2V dynamic range.

The code occurence histogram at the code value of 512 is given in Fig. 9. All the codes delivered are included into 512 ± 1 LSB, with about 90% of them at the center value.

At a sampling rate of 4 Msamples/s the dissipation of the chip is 35 mW. With a time of 250 ns to convert one analogue signal and considering the number of events stored per channel to be less than 5, the power consumption integrated during the ILC duty cycle of 200 ms is evaluated to $0.22\,\mu W$/channel. Assuming that the ON-setting time and the pipeline latency of the convertion are neglected when the ADC is shared by tens of channels, the integrated power dissipation of the ADC is then limited to $1\,\%$ of the total power available for the very front-end electronics of the ECAL.

V. Conclusion

A 10-bit 4-MSamples/s 35-mW CMOS ADC based on a pipeline 1.5-bit/stage architecture has been designed and tested. Its performance confirms that this architecture fullfill the ADC requirements of the ECAL at ILC. Nevertheless, such results can not be obtained without the efficient comparator and amplifier presented in this paper. These building blocks have been optimized to fulfill the offset, sensitivity, speed and stability requirements with low power consumption. Their schematics are as simple as possible in order to improve integration and reliability. Bearing in mind that the comsumption is a key point, the next step will consist on a portage in 3V supply.

References

[1] R. Brinkmann et al., "Tesla Technical Design Report, part II," March 2001.

[2] L.Sumanen, M.Waltari and K.A.I.Halonen, "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter," *IEEE journal of Solid State Circuits*, vol. 36, no. 7, pp. 883–889, July 2001.

[3] K.Iizuka, H.Matsui, M.Ueda and M.Daito, "A 14-bit Digitally Self-Calibrated Pipelined ADC With Adaptative Bias Optimization for Arbitrary Speeds Up to 40 MS/s," *IEEE journal of Solid State Circuits*, vol. 41, no. 4, pp. 883–889, April 2006.

[4] D.Kurose, T.Ito, T.Ueno, T.Yamaji and T.Itakura, "55-mW 200-MSPS 10-bit Pipeline ADCs for Wireless Receivers," *IEEE journal of Solid State Circuits*, vol. 41, no. 7, pp. 1589–1594, July 2006.

[5] R.Van de Plassche, *Integrated analog to digital and digital to analog converters*. Kluwer Academic, 1994.

[6] T. Cho, "Low power, low voltage analog to digital conversion techniques using pipelined architectures," Ph.D dissertation, University of California, Berkeley, CA, 1995.

[7] D.W. Cline, "Noise, Speed and Power trade-offs in pipelined analog to digital Converters," Ph.D dissertation, University of California, Berkeley, CA, November 1995.

[8] H. Lee, A.N. Karanicolas and K.L. Bacrania, "A 15-bit 1-Ms/s digitally self-calibrated pipeline ADC," *IEEE journal of Solid State Circuits*, vol. 28, no. 12, pp. 1207–1215, December 1993.

[9] A.M. Abo and P.R. Gray, "A 1.5V, 10-bit, 14.3-Ms/s CMOS pipeline analog to digital converter," *IEEE journal of Solid State Circuits*, vol. 34, no. 5,pp. 599–606, May 1999.

[10] A. Hastings, "The art of analog layout," Prentice Hall, 2001.

[11] A. Gharbiya, "Operational Amplifiers rail to rail input stages using complementary differential pairs," Technical report, Simon Fraser University, November 2002.

[12] M.F. Li, "A compact power efficient 3V CMOS rail to rail input/output operational amplifier for VLSI cell libraries," *IEEE Solid states circuits*, vol. 29, no. 12, pp. 1505–15014, December 1994.

[13] M.F. Li. "A low voltage CMOS OTA with rail to rail differential input range," *IEEE transactions on circuits and systems*, vol. 47, no. 1, pp. 1–9, January 2000.

[14] M. Wang, "Constant gm rail to rail CMOS op-amp input stage with overlapped transition regions," *IEEE solid states circuits*, vol. 34, no. 2, pp. 148–157, February 1999.

[15] A. Kaiser, "'Introduction to CMOS analog integrated circuit," April 1999.

[16] P.A. Crolla, " A fast latching current comparator for 12-bit A/D applications," *IEEE journal of Solid State Circuits*, vol. 17, no. 6, pp. 1088–1094, December 1982.