A custom 12-bit cyclic ADC for the electromagnetic calorimeter of the International Linear Collider

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Abstract—A custom 12-bit Analog-to-Digital Converter (ADC) has been designed. It is dedicated to the very-front-end electronics of the electromagnetic calorimeter (Ecal) of the International Linear Collider (ILC). A cyclic architecture, with a resolution of 2 bits per cycle has been chosen. Its compactness allows the use of one ADC per channel which simplifies the layout of the final 64-channel very-front-end chip and preserve the signal integrity. In order to optimize the ratio between the sampling rate and the power consumption, an enhanced design is proposed. It involves the use of a single amplifier shared between two parallel capacitor arrays. The power consumption is then limited to 4 mW, and with the use of a power pulsing with the duty ratio of ILC, an integrated power consumption of 0.12 W is expected. The time conversion of 7 $\mu$s obtained with a clock frequency of 1 MHz is shorter compared to the 500 $\mu$s foreseen for A/D conversion. The building blocks which are the operational amplifier and the comparator have been previously validated in a 10-bit pipeline ADC, but they have been optimized to fulfill the 12-bit resolution and speed performance required. A prototype chip has been layouted using the 0.35 $\mu$m CMOS technology of Austriamicrosystems. Measurements show that the Differential Non-Linearity and Integral Non-Linearity are respectively within ±1.2 LSB range and a ±1 LSB range, with a noise limited to 0.9 LSB @ 68 % CL.

Index Terms—ADC, comparator, amplifier, ILC, CALICE, calorimeter, very-front-end electronics.

I. INTRODUCTION

A Custom Analog-to-Digital Converter (ADC) is presented in this paper. It is involved in the ambitious R&D on the very-front-end electronics of the electromagnetic calorimeter (Ecal) of the International Linear Collider (ILC). This calorimeter requires an efficient very-front-end readout electronics to process the 10$^8$ channels of the detector. A measurement of particle energy with a dynamic range of 15 bits and a precision of 8 bits is mandatory. As represented in Fig. 2, those requirements are solved using a wide dynamic range charge amplifier followed by a dual gain shaper and a 12-bit precision ADC. Moreover, the minimal cooling available for the embedded readout electronics imposes an ultra-low power limited to 25 $\mu$W per channel. This objective will be reached thanks to the timing of ILC (Fig. 1), which allows the implementation of a power pulsing with a duty ratio of 1%.

This front end chip is embedded in detector. Concerning radiations, a rad hard technology is not required, so the prototype has been developed with the 0.35 $\mu$m CMOS Austriamicrosystems technology.

II. CHOICE OF THE CONVERTER ARCHITECTURE

A. Requirements for the Ecal

Recalling requirements for the Ecal, the resolution needed for the ADC is 12 bits, with a very compact structure. Concerning the time of conversion, 500 $\mu$s are available to convert all the data at the maximum five data events stored in the analog memories. It means each data has to be converted within a maximum time of 100 $\mu$s. Moreover, the maximum integrated consumption for the ADC has been fixed to 10% of the total power budget of the very front end electronics that means 2.5 $\mu$W.

The cyclic architecture is well adapted to the requirements of the very front end converter of the electromagnetic calorimeter.
Its compactness allows the use of one ADC per channel in order to simplify the layout of the final multi-channel chip. Moreover, the length of the sensitive analog wires can be limited in order to preserve analog signal integrity. The calibration is simplified when each channel is made of a complete analog to digital processing chain. The cyclic ADC is also well adapted to answer to the low power intermediate speed conversion required.

**B. The Cyclic Architecture**

The global architecture is shown in Fig. 3. It consists of a single stage with the output fed back to the input. The resolution of the subranging ADC is 2 bits in order to be insensitive to the offset voltage of the comparators. At each conversion phase, one effective bit and 0.5-bit redundancy are delivered. The two bits are acquired by a flash DAC which delivers the reference voltage needed for the next conversion phase. This architecture presents an optimum trade-off between integration, resolution, consumption and speed.

**III. DESIGN OF THE CYCLIC ADC**

**A. Gain 2 amplifier**

The main issue of the design of the cyclic ADC is the accuracy of the gain 2 amplification which gives the resolution of the ADC. As this gain is made with a ratio of capacitors, a resolution of 12 bits, the matching must be better than \( \frac{1}{\beta} \). Concerning the amplifier itself, its open loop gain and bandwidth must also guarantee the 12-bit accuracy. [3]

**B. Amplifier characteristics**

1) The open loop gain of the amplifier: Assuming \( \beta = 0.5 \), the feedback factor, and \( N = 12 \) bits, the ADC resolution, the closed loop gain of the amplifier \( A_{CL} \) can be write

\[
A_{CL} = \frac{A_{OL}}{1 + A_{OL}/\beta} = \frac{1}{\beta} - \Delta A
\]

where, \( A_{OL} \), is the open loop gain of the amplifier, \( \Delta A = \frac{1}{\beta} \times \frac{1}{\tau} \) is the maximum tolerable error gain. To obtain the 12 bits resolution needed, the minimal open loop gain of the amplifier, \( A_{OL} \), must be,

\[
A_{OL} = \frac{1}{\beta} \left( 2^{(N+1)} - 1 \right) \approx \frac{2^{(N+1)}}{\beta}
\]

2) The bandwidth amplifier: Assuming the clock frequency used for the ADC is \( f_{clk} = 1 \) MHz, the open loop gain of the amplifier can be expressed as is,

\[
A_{OL} (f) = \frac{A_{OL} (0)}{1 + j \frac{f}{f_{3dB}}}
\]

Considering that \( 1 \gg \frac{1}{10^{6} \times A_{OL} (0)} \), the closed loop gain of the amplifier can be defined as,

\[
A_{CL} (f) = \frac{\frac{1}{\beta}}{1 + j \frac{f}{f_{3dB}}}
\]

With, \( f_{3dB} = f_{3dB} \times A_{OL} (0) \)

In temporal domain, the output of the amplifier must be obtained with a 12 bits accuracy to obtain the required resolution for the ADC.

\[
V_{out} = V_{outfinal} \left( 1 - \frac{1}{2^{N+1}} \right) = V_{outfinal} \left( 1 - e^{-\tau} \right)
\]

With, \( \tau = \frac{1}{2\pi\beta} \)

Considering that the time required to obtain 12 bits resolution must be inferior to the clock frequency, \( t < \frac{1}{f_{clk}} \), the conditions for the bandwidth amplifier are given by,

\[
f_{3dB} \geq \frac{f_{clk} \times ln \left( \frac{2^{N+1}}{2} \right)}{2\pi\beta}
\]

\[
f_{3dB} \geq 2.86 MHz and f_{3dB} \geq 174 Hz
\]

3) Summary of the technical characteristics for the operational amplifier: The characteristics of the amplifier, [4], are presented with a 2.4 pF capacitive charge. Its gain-bandwidth product has been fixed to 50 MHz with a power consumption limited to 3 mW.

<table>
<thead>
<tr>
<th>Power supply</th>
<th>3.5 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Consumption</td>
<td>3 mW</td>
</tr>
<tr>
<td>Differential Gain</td>
<td>19.6 k</td>
</tr>
<tr>
<td>Differential Bandwidth -3dB</td>
<td>2.5 kHz</td>
</tr>
<tr>
<td>GBW</td>
<td>49 MHz</td>
</tr>
<tr>
<td>( f_{p} )</td>
<td>102 MHz</td>
</tr>
<tr>
<td>Common Mode Gain</td>
<td>36.0 k</td>
</tr>
<tr>
<td>Common Mode Bandwidth -3dB</td>
<td>520 Hz</td>
</tr>
<tr>
<td>Differential phase margin</td>
<td>73 degrees @ 68% C.L.</td>
</tr>
<tr>
<td>Common Mode phase margin</td>
<td>74 degrees @ 68% C.L.</td>
</tr>
</tbody>
</table>

**C. Capacitor array**

The minimal size for capacitance to have a 12 bits resolution is defined by this formula.

\[
U_{noise} = \frac{U_{max}}{2} = \frac{U_{max}}{2^{(N+1)}} = \sqrt{\frac{kT}{C}}
\]

- \( U_{max} \) maximum output signal, 2V;
- \( N \) : ADC resolution, 12 bits;

\[
C = 834 fF
\]
the configuration is swapped as represented in the bottom part of Fig. 4. Comparators perform the flash digital conversion and deliver two bits to the corresponding DAC which fixes the value of the voltage reference subtracted during the next clock phase. This structure requires twice comparators and DAC compared to the basic one, it means four comparators and two DAC. The total time to obtain the 12-bit data is reduced to (6+1) clock periods.

V. GAIN ACCURACY, THE KEY POINT

The cyclic ADC works in two main cycles, one is the sampling phase (phase 1) and the other one is the amplification phase (phase 2). During the phase 1, \( Q_{1C_2} = C_3 V_{in} \), \( Q_{1C_3} = C_4 V_{in} \). During the phase 2, there is a charge conservation and we obtain, \( Q_{2C_2} + Q_{2C_4} = Q_{1C_3} + Q_{1C_4} \), \( C_3 V_a + C_4 V_{ref} = C_3 V_{in} + C_4 V_{in} \). If \( C_3 = C_4 \), we obtain,

\[
V_a = (2 \times V_{in} - V_{ref})
\]

This approach doesn’t take into account three parameters
• The open loop gain amplifier is not infinity;
• The input capacitance, \( C_{in} \) of the amplifier is not zero;
• A time constant due to the amplifier, 12 bits resolution

needs \( t = 8.3\tau \), with \( \tau \) the time constant of the amplifier.

Considering the three parameters, the formula is, [2],

\[
V_a = (2 \times V_{in} - V_{ref}) \times \left( 1 - e^{t/\tau} \right) \times \frac{1}{1 + \frac{2}{A_0} + \frac{C_{in}}{A_0 C}}
\]

• \( A_0 \) : Open loop gain amplifier;
• \( C \) : Feedback capacitance.

VI. POWER PULSING

A power pulsing has been implemented reducing the integrated consumption per conversion to 0.12 \( \mu \)W. The power pulsing is implemented in the master current sources with four complementary switches, like presented in the Fig. 5. The ADC is power on 1\% of the time.

VII. MEASUREMENTS

A first prototype circuit of a 12-bit cyclic ADC has been designed using the 0.35 \( \mu \)m CMOS technology of Austriamicrosystems, and the ten chips bounded tested. Measurements of the cyclic ADC have been carried out thanks to a dedicated test bench illustrated on Fig. 6. A 16-bit resolution DAC generates the analog signal \( V_{IN} \) to the input of the ADC under
test. This DAC is controlled by a PC through an USB link and a FPGA circuit. The DC input signal is processed by the ADC under test and the resulting data $D_{ADC}$ of the analog-to-digital conversion is acquired by the PC.

Only static measurements are performed with this test bench.

Fig. 6. Architecture of the test bench used to measure static performance of the ADC.

Evaluation of dynamic performance for ADC dedicated to the very front-end electronics of the Si-W detector is not relevant because signals to be converted are static voltage stored in the analog memory.

Noise and linearity performance has been measured and the efficiency of the power pulsing system evaluated.

A. Linearity

Linearity measurements have been performed applying a ramp of DC voltages from 0 to 2.0 V to the input of the ADC under test. Then both Integral (INL) and Differential (DNL) Non-Linearity can be determined. The INL refers to the deviation, in LSB, of each individual output code to the corresponding value on the ideal transfer function. The DNL is defined as the difference between an actual step width and the ideal value of one LSB.

The curve plotted on Fig. 7 shows that the differential non-linearity is within ±1 LSB.

The INL curve plotted on Fig. 8 exhibits that the error is limited to ±1.2 LSB over the 2.0 V dynamic range.

B. Noise

The measurement of the noise of the conversion is given by the fluctuation of the code delivered by the ADC with a steady input voltage.

The distribution of the codes obtained at the middle of the dynamic range with the nominal clock frequency of 1 MHz is given by Fig. 9. It is obtained with 1000 successive conversions of a DC input voltage signal of 1.0 V. The standard deviation of the data is limited to 0.88 LSB.

Measurements of the noise have been also performed with different values of input voltage over the 2.0 V dynamic range, with the nominal clock frequency of 1 MHz and with twice the nominal frequency. Results are reported on Fig. 10. With the nominal clock frequency, the noise is lower than 0.9 LSB all over the 2.0 V dynamic range. When the clock frequency is increased to 2 MHz, the noise increases as the input voltage does. We can observe on the plot that the noise rises by step when the input voltage overcomes the value of the threshold voltages. The additional noise is then induced by the reference voltages. Decoupling outside the chip is not sufficient and the implementation of decoupling capacitors inside the chip is relevant to improve noise performance at higher clock frequency.
C. Power pulsing

A power pulsing system has been implemented in the chip. This function has been tested down to a duty cycle of 3% with a clock frequency of 1 MHz. The total time to perform one analog to digital conversion is increased from 7 to 8 µs when the power pulsing is functioning. As shown by the linearity curve on Fig. 11, the linearity is not deteriorated by the use of the power pulsing.

The decrease of the consumption versus the duty cycle is reported in Fig. 12.

VIII. SUMMARY OF THE PERFORMANCE OF THE ADC

<table>
<thead>
<tr>
<th>Architecture</th>
<th>1.5-bit/stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.35 µm 2-P 4-M CMOS</td>
</tr>
<tr>
<td>Area</td>
<td>0.7 \times 0.25 \text{mm}^2</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>3.5 V</td>
</tr>
<tr>
<td>Resolution</td>
<td>12 bits</td>
</tr>
<tr>
<td>Full scale</td>
<td>2 V differential</td>
</tr>
<tr>
<td>Conversion rate</td>
<td>143 kS/s</td>
</tr>
<tr>
<td>Consumption</td>
<td>3.94 mW</td>
</tr>
<tr>
<td>INL</td>
<td>1.2 LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>1 LSB</td>
</tr>
<tr>
<td>Noise</td>
<td>0.88 LSB @ 68% C.L.</td>
</tr>
</tbody>
</table>

REFERENCES