A custom 12-bit cyclic ADC for the electromagnetic calorimeter of the International Linear Collider

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***Abstract*—A custom 12-bit Analog-to-Digital Converter (ADC) has been designed. It is dedicated to the very-front-end electronics of the electromagnetic calorimeter (Ecal) of the International Linear Collider (ILC). A cyclic architecture, with a resolution of 2 bits per cycle has been chosen. Its compactness allows the use of one ADC per channel which simplifies the layout of the final 64-channel very-front-end chip and preserve the signal integrity. In order to optimize the ratio between the sampling rate and the power consumption, an enhanced design is proposed. It involves the use of a single amplifier shared between two parallel capacitor arrays. The power consumption is then limited to 4 mW, and with the use of a power pulsing with the duty ratio of ILC, an integrated power consumption of 0.12 μW is expected. The time conversion of 7 μs obtained with a clock frequency of 1 MHz is shorter compare to the 500 μs foreseen for A/D conversion. The building blocks which are the operational amplifier and the comparator have been previously validated in a 10-bit pipeline ADC, but they have been optimized to fulfil the 12-bit resolution and speed performance required. A prototype chip has been layouted using the 0.35 μm CMOS technology of Austriamicrosystems. Measurements show that the Differential Non-Linearity and Integral Non-Linearity are respectively within a $\pm$1.2 LSB range and a $\pm$1 LSB range, with a noise limited to 0.9 LSB @ 68 % CL.**

***Index Terms*—ADC, comparator, amplifier, ILC, CALICE, calorimeter, very-front-end electronics.**

I. Introduction

A Custom Analog-to-Digital Converter (ADC) is presented in this paper. It is involved in the ambitious R&D on the very-front-end electronics of the electromagnetic calorimeter (Ecal) of the International Linear Collider (ILC). This calorimeter requires an efficient very-front-end readout electronics to process the 10^8 channels of the detector. A measurement of particle energy with a dynamic range of 15 bits and a precision of 8 bits is mandatory. As represented in Fig. 2, those requirements are solved using a wide dynamic range charge amplifier followed by a dual gain shaper and a 12-bit precision ADC. Moreover, the minimal cooling available for the embedded readout electronics imposes an ultra-low power limited to 25 μW per channel. This objective will be reached thanks to the timing of ILC (Fig. 1), which allows the implementation of a power pulsing with a duty ratio of 1 %.

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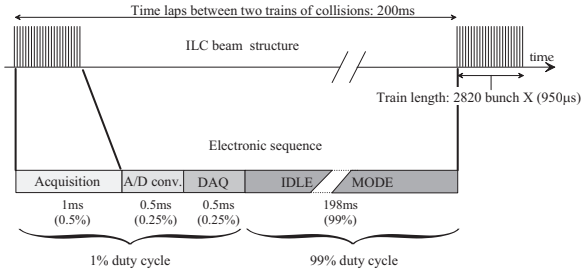

Fig. 1. ILC beam structure.

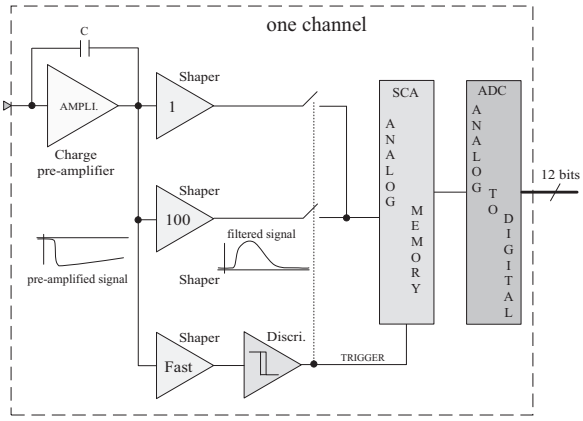

Fig. 2. One VFE channel block diagram: a charge pre-amplifier is followed by three shapers, two shapers for the filtering and one fast shaper for the auto-trigger; the analog data is stored in an analog memory (SCA) before being processed by the ADC .

This front end chip is embedded in detector. Concerning radiations, a rad hard technology is not required, so the prototype has been developped with the $0.35\,\mu m$ CMOS Austriamicrosystems technology.

II. Choice of the converter architecture

A. Requirements for the Ecal

Recalling requirements for the Ecal, the resolution needed for the ADC is 12 bits, with a very compact structure. Concerning the time of conversion, $500\,\mu$s are available to convert all the datathe maximum five data events stored in the analog memories. It means each dat has to be converted within a maximum time of $100\,\mu$s. Moreover, the maximum integrated consumption for the ADC has been fixed to $10\,\%$ of the total power budget of the very front end electronics that means $2.5\,\mu$W.

The cyclic architecture is well adapted to the requirements of the very front end converter of the electromagnetic calorimeter.

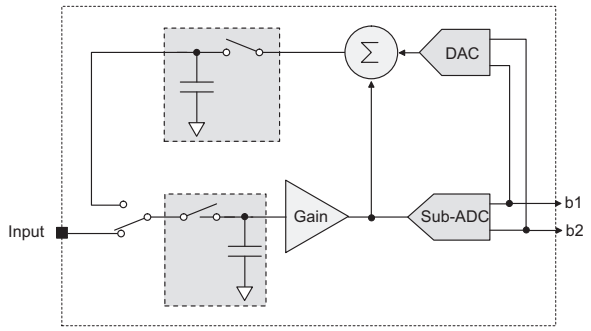

Fig. 3. Global Cyclic ADC architecture

Its compactness allows the use of one ADC per channel in order to simplify the layout of the final multi-channel chip. Moreover, the length of the sensitive analog wires can be limited in order to preserve analog signal integrity. The calibration is simplified when each channel is made of a complete analog to digital processing chain. The cyclic ADC is also well adapted to answer to the low power intermediate speed conversion required.

B. The Cyclic Architecture

The global architecture is shown in Fig. 3. It consists of a single stage with the output fed back to the input. The resolution of the subranging ADC is 2 bits in order to be insensitive to the offset voltage of the comparators. At each conversion phase, one effective bit and 0.5-bit redundancy are delivered. The two bits are acquired by a flash DAC which delivers the reference voltage needed for the next conversion phase. This architecture presents an optimum trade-off between integration, resolution, consumption and speed.

III. Design of the cyclic ADC

A. Gain 2 amplifier

The main issue of the design of the cyclic ADC is the accuracy of the gain 2 amplification which gives the resolution of the ADC. As this gain is made with a artio of capacitors, the matching aspect of these capacitors is very critical. For a resolution of 12 bits, the matching must be better than $\frac{1}{4000}$. Concerning the amplifier itself, its open loop gain and bandwidth must also guarantee the 12-bit accuracy. [3]

B. Amplifier characteristics

1) The open loop gain of the amplifier: Assuming $\beta = 0.5$, the feedback factor, and $\mathrm{N} = 12\,\mathrm{bits}$, the ADC resolution, the closed loop gain of the amplifier $\mathrm{A_{CL}}$can be write

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta} = \frac{1}{\beta} - \Delta A$$

where, $\mathrm{A_{ol}}$, is the open loop gain of the amplifier,
$\Delta \mathrm{A} = \frac{1}{\beta} \times \frac{1}{2^{\mathrm{N}+1}}$ is the maximum tolerable error gain.
To obtain the 12 bits resolution needed, the minimal open loop gain of the amplifier, $\mathrm{A_{OL}}$, must be,

$$A_{OL} = \frac{1}{\beta}\left(2^{(N+1)} - 1\right) \approx \frac{2^{(N+1)}}{\beta}$$

$$\boxed{A_{OL} = 16484}$$

2) The bandwith amplifier: Assuming the clock frequency used for the ADC is $\mathrm{F_{clk}} = 1\,\mathrm{MHz}$, the open loop gain of the amplifier can be expressed as is,

$$A_{OL}(f) = \frac{A_{OL}(0)}{1 + j\frac{f}{f_{3dB}}}$$

Considering that $1 >> \frac{1}{(\beta \times \mathrm{A_{OL}}(0))}\}$, the closed loop gain of the amplifier can be defined as,

$$A_{CL}(f) = \frac{\frac{1}{\beta}}{1 + j\frac{f}{f_\mu \beta}}$$

With, $\mathrm{f}_\mu = \mathrm{f_{3dB}} \times \mathrm{A_{OL}}(0)$
In temporal domain, the output of the amplifier must be obtained with a 12 bits accuracy to obtain the required resolution for the ADC.

$$V_{out} = V_{outfinal}\left(1 - \frac{1}{2^{N+1}}\right) = V_{outfinal}\left(1 - e^{-\frac{t}{\tau}}\right)$$

With, $\tau = \frac{1}{2\pi \mathrm{f}_\mu \beta}$
Considering that the time required to obtain 12 bits resolution must be inferior to the clock frequency, $\mathrm{t} < \frac{1}{\mathrm{f_{clk}}}$, the conditions for the bandwith amplifier are given by,

$$f\mu \geq \frac{f_{clk} \times ln\left(2^{N+1}\right)}{2\pi\beta}$$

$$\boxed{f_\mu \geq 2.86\,MHz\,and\,f_{3_{dB}} \geq 174\,Hz}$$

3) Summary of the technical characteristics for the operational amplifier: The characteristics of the amplifier, [4], are presented with a 2.4 pF capacitive charge. Its gain-bandwidth product has been fixed to 50 MHz with a power consumption limited to 3 mW.

TABLE I
Open loop amplifier characteristics.

Power supply	3.5 V
Consumption	3 mW
Differential Gain	19.6 k
Differential Bandwith -3 dB	2.5 kHz
GBW	49 MHz
F_μ	102 MHz
Common Mode Gain	36.0 k
Common Mode Bandwith -3 dB	520 Hz
Differential phase margin	73 degrees @ 68% C.L.
Common Mode phase margin	74 degrees @ 68% C.L.

C. Capacitor array

The minimal size for capacitance to have a 12 bits resolution is defined by this formula.

$$U_{noise} = \frac{\frac{U_{LSB}}{2}}{\sqrt{12}} = \frac{\frac{U_{max}}{2^{(N+1)}}}{\sqrt{12}} = \sqrt{\frac{kT}{C}}$$

- U_{max} maximum output signal, 2 V;
- N : ADC resolution, 12 bits;

$$\boxed{C = 834\,fF}$$

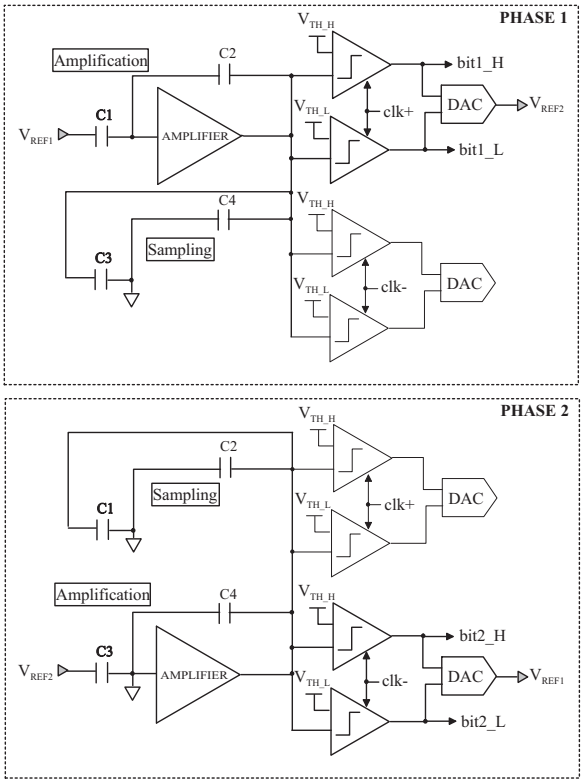

Fig. 4. Simplified schematic of the cyclic ADC where the configuration of the two opposite clock phases are represented. A single amplifier is shared between two capacitor arrays which are used alternatively for amplification and for sampling. Four comparators and two DAC are also needed.

D. The comparator

The architecture of the comparator is the same as the one previously designed for a 10-bit pipeline ADC [4]. The main characteristics are reported in table II.

TABLE II
COMPARATOR CHARACTERISTICS.

Power supply	3 V
Clock frequency	1 MHz
Consumption	204 μW @ 1 MHz
Max. Sensitivity	3 mV @ 3 σ
Max. Offset	10 mV @ 3 σ

IV. CHARACTERISTICS OF THE ADC

Considering Ecal requirements, a cyclic ADC has been designed. It presents a 12-bit resolution with a clock frequency of 1 MHz and a conversion rate of 143 kS/s. The power consumption is limited to 4 mW with a power supply of 3.5 V. The simplified schematic view of the cyclic ADC is given in Fig. 4. In order to reject the common mode noise, a fully differential structure has been adopted, but for simplicity the schematic has been drawn with single ended signals.

Fig. 4 shows that, in order to optimize power consumption, a single operational amplifier is shared between two identical capacitors arrays. During the clock phase (PHASE 1), capacitors C1 and C2 are fed back to the amplifier, when capacitors C3 and C4 are used for sampling the amplified-by-two signal. During the opposite clock phase (PHASE 2), the configuration is swapped as represented in the bottom part of Fig. 4. Comparators perform the flash digital conversion and deliver two bits to the corresponding DAC which fixes the value of the voltage reference subtracted during the next clock phase. This structure requires twice comparators and DAC compared to the basic one, it means four comparators and two DAC. The total time to obtain the 12-bit data is reduced to (6+1) clock periods.

V. GAIN 2 ACCURACY, THE KEY POINT

The cyclic ADC works in two main cycles, one is the sampling phase (phase 1) and the other one is the amplification phase (phase 2). During the phase 1, $\mathrm{Q_{1C_3}} = \mathrm{C_3 V_{in}}$, $\mathrm{Q_{1C_4}} = \mathrm{C_4 V_{in}}$. During the phase 2, there is a charge conservation and we obtain, $\mathrm{Q_{2C_3}} + \mathrm{Q_{2C_4}} = \mathrm{Q_{1C_3}} + \mathrm{Q_{1C_4}}$, $\mathrm{C_3 V_s} + \mathrm{C_4 V_{ref}} = \mathrm{C_3 V_i n} + \mathrm{C_4 V_i n}$. If $\mathrm{C_3} = \mathrm{C_4}$, we obtain,

$$\mathrm{V_s} = (2 \times \mathrm{V_{in}} - \mathrm{V_{ref}})$$

This approach doesn't take into account three parameters

- The open loop gain amplifier is not infinity;
- The input capacitance, $\mathrm{C_{in}}$ of the amplifier is not zero;
- A time constant due to the amplifier, 12 bits resolution needs $\mathrm{t} = 8.3\tau$, with τ the time constant of the amplifier.

Considering the three parameters, the formula is, [2],

$$V_s = (2 \times V_{in} - V_{ref}) \times \left(1 - e^{t/\tau}\right) \times \frac{1}{\left(1 + \frac{2}{A_0} + \frac{C_{in}}{A_0 C}\right)}$$

- $\mathrm{A_0}$: Open loop gain amplifier;
- C : Feedback capacitance.

VI. POWER PULSING

A power pulsing has been implemented reducing the integrated consumption per conversion to $0.12\,\mu\mathrm{W}$. The power pulsing is implemented in the master current sources with four complementary switches, like presented in the Fig. 5. The ADC is power on $1\,\%$ of the time.

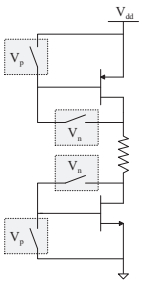

Fig. 5. Power pulsing schematic.

VII. MEASUREMENTS

A first prototype circuit of a 12-bit cyclic ADC has been designed using the $0.35\,\mu\mathrm{m}$ CMOS technology of Austriamicrosystems, and the ten chips bounded tested. Measurements of the cyclic ADC have been carried out thanks to a dedicated test bench illustrated on Fig. 6. A 16-bit resolution DAC generates the analog signal $\mathrm{V_{IN}}$ to the input of the ADC under

test. This DAC is controlled by a PC through an USB link and a FPGA circuit. The DC input signal is processed by the ADC under test and the resulting data D_{ADC} of the analog-to-digital conversion is acquired by the PC.

Only static measurements are performed with this test bench.

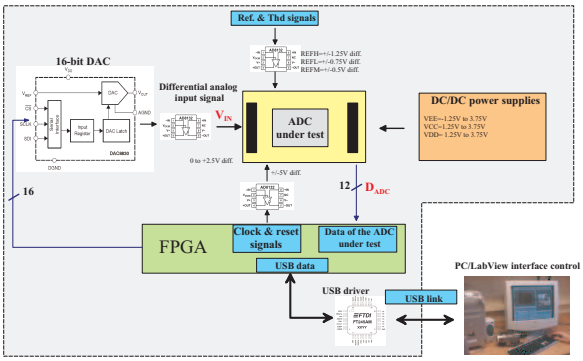

Fig. 6. Architecture of the test bench used to measure static performance of the ADC.

Evaluation of dynamic performance for ADC dedicated to the very front-end electronics of the Si-W detector is not relevant because signals to be converted are static voltage stored in the analog memory.

Noise and linearity performance has been measured and the efficiency of the power pulsing system evaluated.

A. *Linearity*

Linearity measurements have been performed applying a ramp of DC voltages from 0 to 2.0 V to the input of the ADC under test. Then both Integral (INL) and Differential (DNL) Non-Linearity can be determinated. The INL refers to the deviation, in LSB, of each individual output code to the corresponding value on the ideal transfer function. The DNL is defined as the difference between an actual step width and the ideal value of one LSB.

The curve plotted on Fig. 7 shows that the differential non-linearity is within ± 1 LSB.

The INL curve plotted on Fig. 8 exhibits that the error is limited to ± 1.2 LSB over the 2.0 V dynamic range.

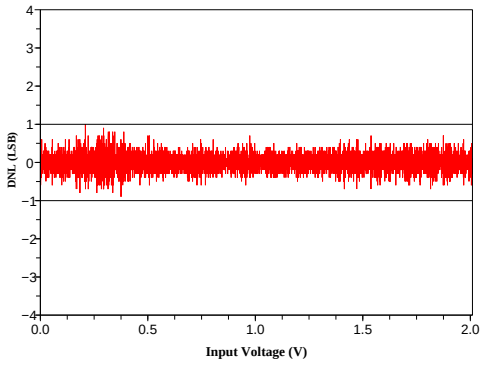

Fig. 7. Differential Non-Linearity.

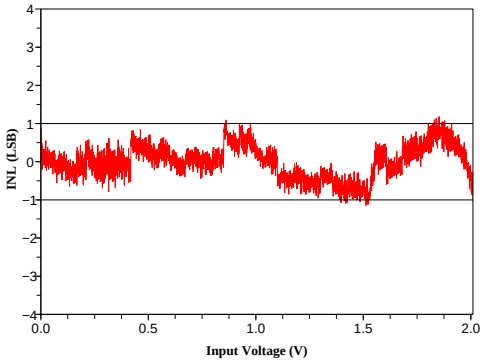

Fig. 8. Integral Non-Linearity.

B. *Noise*

The measurement of the noise of the conversion is given by the fluctuation of the code delivered by the ADC with a steady input voltage.

The distribution of the codes obtained at the middle of the dynamic range with the nominal clock frequency of 1 MHz is given by Fig. 9. It is obtained with 1 000 successive conversions of a DC input voltage signal of 1.0 V. The standard deviation of the data is limited to 0.88 LSB.

Measurements of the noise have been also performed with different values of input voltage over the 2.0 V dynamic range, with the nominal clock frequency of 1 MHz and with twice the nominal frequency. Results are reported on Fig. 10. With the nominal clock frequency, the noise is lower than 0.9 LSB all over the 2.0 V dynamic range. When the clock frequency is increased to 2 MHz, the noise increases as the input voltage does. We can observe on the plot that the noise rises by step when the input voltage overcomes the value of the threshold voltages. The additional noise is then induced by the reference voltages. Decoupling outside the chip is not sufficient and the implementation of decoupling capacitors inside the chip is relevant to improve noise performance at higher clock frequency.

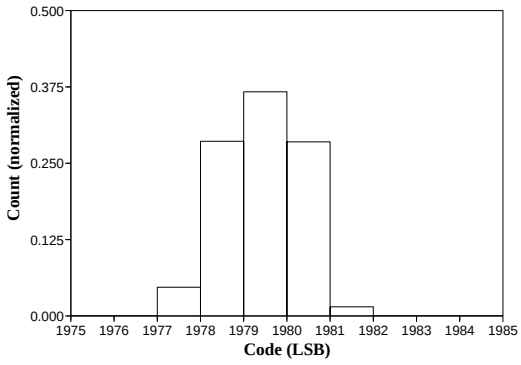

Fig. 9. Distribution of the code delivered by the ADC at the middle of the dynamic range.

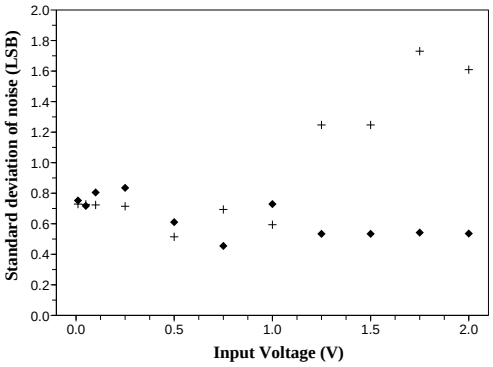

Fig. 10. Standard deviation of ADC measurement for different input voltages, with a clock frequency of 1 MHz (diamond) and 2 MHz (cross).

C. Power pulsing

A power pulsing system has been implemented in the chip. This function has been tested down to a duty cycle of 3 % with a clock frequency of 1 MHz. The total time to perform one analog to digital conversion is increased from 7 to 8 μs when the power pulsing is functionning. As shown by the linearity curve on Fig. 11, the linearity is not deteriorated by the use of the power pulsing.

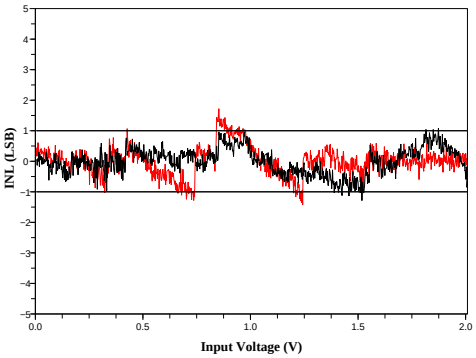

Fig. 11. Integral Non-Linearity with (black) and without (red) power pulsing.

The decrease of the consumption versus the duty cycle is reported in Fig.12.

VIII. Summary of the performance of the ADC

TABLE III
SUMMARIZED PERFORMANCE OF THE CYCLIC ADC.

Architecture	1.5-bit/stage
Technology	0.35 μm 2-P 4-M CMOS
Area	$0.7 \times 0.25\,\mathrm{mm}^2$
Supply Voltage	3.5 V
Resolution	12 bits
Full scale	2 V differential
Conversion rate	143 kS/s
Consumption	3.94 mW
INL	1.2 LSB
DNL	1 LSB
Noise	0.88 LSB @ 68% C.L.

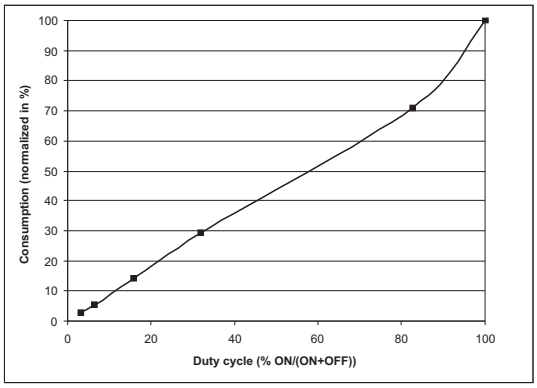

Fig. 12. Measured power consumption (normalized to 100 % when power pulsing is not used) versus the value of duty cycle.

IX. Conclusion

A cyclic ADC has been designed using the 0.35 μm CMOS technology of Austriamicrosystems. It presents a resolution of 12 bits with a clock frequency of 1 MHz and the conversion rate is 143 kS/s. The power consumption is limited to 4 mW with a power supply of 3.5 V. A power pulsing has been implemented reducing the integrated consumption per conversion to 0.12 μW in the ILC timing condition. The performance of the ADC has been measured. The INL is within a $\pm$ 1.2 LSB range, when the DNL is within a $\pm$ 1 LSB range. This compact 12-bit low power ADC fulfil the requirements of the very front end for the electromagnetic calorimeter of the International Linear Collider.

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