Phase and amplitude measurement for the SPIRAL2 accelerator
C. Jamet, W. Le Coz, C. Doutressoulles, T. André, E. Swartvagher

To cite this version:

HAL Id: in2p3-00397563
http://hal.in2p3.fr/in2p3-00397563
Submitted on 22 Jun 2009
PHASE AND AMPLITUDE MEASUREMENT FOR THE SPIRAL2 ACCELERATOR

C. Jamet, W. Le Coz, C. Doutressoulles, T. Andre, E. Swartvagher, GANIL, Caen, France

Abstract
The SPIRAL2 project is composed of an accelerator and a radioactive beam section. Radioactive ions beams (RIBs) will be accelerated by the current cyclotron CIME and sent at GANIL experimental areas. The accelerator, with a RFQ and a superconducting Linac, will accelerate 5 mA deuterons up to 40 MeV and 1 mA heavy ions up to 14.5 MeV/u. A new electronic device has been evaluated at GANIL to measure phase and amplitude of pick-up signals. The principle consists of directly digitizing pulses by under-sampling. Phase and amplitude of different harmonics are then calculated with a FPGA by an I/Q method. Tests and first results of a prototype are shown and presented as well as future evolutions.

SPIRAL2 ACCELERATOR

The accelerator is divided in 3 main parts, an injector, a superconducting linac and a high energy line. The injector part is composed of a deuteron/proton line, an ion line (LEBT), a RFQ and a MEBT line. Two kinds of superconductivity cavity are used for the Linac ($\beta=0.07$, $\beta=0.12$).

Table 1: Beam Intensity and Power

<table>
<thead>
<tr>
<th>Intensity</th>
<th>Energy</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEBT1 (ions)</td>
<td>1 mA</td>
<td>20 keV/A</td>
</tr>
<tr>
<td>LEBT2 (deut.)</td>
<td>5 mA</td>
<td>40 keV</td>
</tr>
<tr>
<td>MEBT</td>
<td>5 mA</td>
<td>750 keV/A</td>
</tr>
<tr>
<td>HEBT</td>
<td>5 mA</td>
<td>20 MeV/A</td>
</tr>
</tbody>
</table>

Beam energy measurement

During the RFQ and the MEBT commissioning, an Injector Test Bench (BTI) will be used to qualify beam characteristics. Beam energy will be measured at the exit of the RFQ by the “time of flight” method. Another beam energy measurement by TOF is foreseen in the HEBT at the exit of the superconducting LINAC.

Table 2: Phase Measurement Accuracy

<table>
<thead>
<tr>
<th>Energy</th>
<th>Distance</th>
<th>Phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBT</td>
<td>$10^{-3}$</td>
<td>1500 +/-0.2</td>
</tr>
<tr>
<td>HEBT</td>
<td>$5.10^{-3}$</td>
<td>5000 +/-2</td>
</tr>
</tbody>
</table>

INTJECTOR TEST BENCH PICK-UP

3 pick-ups will be used to measure beam energy. The third pick-up allows determining the bunch number between two first pick-ups.

PICK-UP SIGNAL SIMULATIONS

Signal amplitudes
- 1mA ions Q/A =1/3: $V_{h1} = 50$ mV
- 5mA deuterons: $V_{h1} = 230$ mV
Ratio h1/h2 = 13
Figure 4: HEBT Pick-up Signal Simulation.

Signal amplitudes
- 1mA Ions Q/A= 1/3: Vh1= 27mV  Vh2= 44mV
- 5mA Deuterons : Vh1= 136mV Vh2= 220mV
Ratio h1/h2 = 0,62

PHASE MEASUREMENT METHOD

Three pick-up signals and the accelerator frequency signal will be connected directly to the FPGA phasemeter.

Under-sampling

Every signal is digitized at a sampling frequency lightly different from the signal frequency.

\[ S(t) \]

\[ \Delta t = Tsamp - Tsig \]

\[ Nb = \frac{Tsig}{\Delta t} \]

\[ Fsamp = \frac{Fsig}{Nb + 1} \]

Nb: number of samplings to reconstruct a signal period

Under-sampling uses ADCs at a lower frequency than a classical digitalisation frequency. The sample period is higher and allows digital signal processing directly by FPGA. The ADC accuracy increases and improves the dynamic measurement. The reference is also undersampled and used in the FPGA digital signal processing.

I/Q Method

Digital signals are processed by an I/Q method in a FPGA. A synchronisation input is foreseen for pulsed beam, which indicates the beam presence. Under-sampling and digital process simplify the analogic chain and remove mixers used classically with an I/Q method.

FPGA BOARD PROTOTYPE

The FPGA board prototype is composed of analog to digital converters AD6645 Analog Devices (14 bits), a FPGA Virtex2 Xilinx, a double digital to analog converter AD9765, a parallel and a serial interface.
TEST BENCH DESCRIPTION

Tests and measurements are realized at a GANIL frequency (7MHz). The goal is to compare the measures in laboratory and on the accelerator.

**CW Sinusoidal Signal**

Synthesizer R&S and splitters generate references and signals. FPGA Phase and module values are compared with the lock-in amplifier measures (SR 844 Stanford Research). The reference frequency is calculated to have 256 values per period in the FPGA process. Programmable Delay lines change the signal phase from 0° to 360°. Tests consist of measuring phase and module variations between FPGA and SR844 with shifting the signal phase. A variable attenuator decreases module signal from 0dB to 60 dB and allows comparing results with different signal levels.

RESULTS

Results are the same with a duty cycle (1ms/100ms), measurement time increases proportionally to the ratio.

**CW Pulse Signal**

A pulse generator (Avtech AVM-1-C) is installed in front of the attenuator. The pulse width is about 10 ns.

**CONCLUSIONS AND EVOLUTIONS**

Under-sampling and numerical processing by I/Q method gives good results in laboratory. On a great dynamics (60dB), FPGA phasemeter is able to measure sinusoidal signal phase precisely (+/-0.1°). With pulse signals, improvements must be done to filter the reference signal and optimize the accuracy.

Pick-up signal digitalization gives also the possibility to calculate module and phase of different harmonics. This electronics can also give the opportunity to follow beam intensity on line.

The next step consists in using FPGA phasemeter on the GANIL accelerator, measuring the time of flight with two pick-ups, calculating the beam energy and comparing this value with the spectrometer measure.

A new prototype is also in development to improve analog input adaptation, sampling frequency distribution, integration with the FPGA.

REFERENCES

[4] T. Junquera & al, The high intensity superconducting Linac for the SPIRAL2 project at Ganil, LINAC06, Knoxville,