Front-end multi-channel PMT-associated readout chip for hodoscope application
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Abstract

For developing a prompt gamma imaging system, we have designed a 16-channel readout chip in a BiCMOS process to be associated with multi-anode photomultipliers (MaPMTs). Each channel has one current input and two separated outputs. The input has very low impedance to minimize electrical crosstalk and effects of capacitances. The two outputs serve to, respectively, detect signal event and quantify signal charge. The channel architecture is a current-mode one, employing a current conveyor to drive both a buffered current comparator and a charge-sensitive amplifier (CSA). The current conveyor is built with super-common-base (SCB) transistor structures to obtain input impedance in the order of a few ohms. Circuit design with the use of bipolar transistor components also improves frequency and noise performances. The chip has been tested and the evaluated characteristics meet the system requirements.

Keywords: prompt gamma imaging system, super-common-base(SCB), current conveyor, charge-sensitive amplifier (CSA),

1. INTRODUCTION

References

2. CIRCUIT DESCRIPTION

This process allows the use of RF and large-transconductance bipolar components, which is useful for the design of wideband, low-impedance and low-noise circuits with improved performances[3].

2.1. Current Conveyor

The current conveyor has a low-impedance input and two high-impedance current outputs, with a 4-bit current gain control to compensate effects of optic fiber ageing and the MaPMT’s gain dispersion. Figure 2(a) shows the structure of the current conveyor. It employs two Super Common-Base (SCB) transistors [4-5] (see Figure 2(b)) to drive complementary switched current mirrors having variable-gain output branches. The current input signal is applied to one SCB, and a referenced current is applied to the other to cancel bias offset contribution to the output signals.
Figure 1: Prompt gamma imaging using a beam hodoscope

Figure 2: (a) Low-impedance, variable-gain current conveyor

Figure 2: (b) Super-common-base SCB transistor structure

The SCB transistor shown in Figure 2(b) is basically a common-base topology \( Q_1 \) with a negative feedback loop \( Q_2 \). The input impedance of the current conveyor, mainly determined by that of the SCB, is expressed as:

\[
Z_{in} = \frac{1}{(1 + \frac{A_0}{\omega_A}) \cdot g_m \cdot Q_1 + s C_A} \tag{1}
\]

where \( A_0 \) is the voltage gain of \( Q_2 \) at low frequencies; \( C_A \) is the sum of parasitic capacitances at the input node A (including the detector output capacitance \( C_D \)). \( \omega_A \) and \( \omega_B \) are poles related respectively to nodes A and B. At moderate frequencies, the input impedance is given by

\[
Z_{in} \approx \frac{1}{A_0 \cdot g_m \cdot Q_1} \tag{2}
\]

The current gain of the current conveyor is given by[6]:

\[
\frac{I_{out}}{I_{in}} = \frac{g_{m,MP_2-MP_5}}{g_{m,MP_1}} \times \left( 1 + \frac{C_1}{\delta_{m,Q_1}} \right) \left( 1 + \frac{C_2}{\delta_{m,MP_2}} \right)
\]

with \( C_1 = C_{bc,Q_1} \) and \( C_2 = \Sigma C_{node,G} \)

The current comparator following the current conveyor detects current signal events. It compares the current conveyor’s corresponding output signal (typically lasting a few nanoseconds) with a referenced threshold current and produces a pulsed output voltage response.

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Figure 3 shows the current comparator mainly consisting of a signal current mirror and a 2-stage output buffer. The signal current mirror employs bipolar transistor components to reduce its input impedance and to improve the speed performance of the circuit. This current mirror performs current-to-voltage conversion at its output:
The time constants at nodes C and D are respectively $\tau_C = C_C/S_m.Q_1$ and $\tau_D = C_D/S_m.Q_2$ with $C_C = C_{ce, Q_1} + C_{be, Q_1} + C_{inverter}$. As $C_C \gg C_D$ and $S_m.Q_1 < S_m.Q_2$, the speed performance of the current comparator is determined by $\tau_C$. It can be optimized by careful layout and proper sizing of transistor components to reduce different capacitance contributions to $C_C$. The 2-stage buffer converts $\Delta V_D$ to a logic-level pulse.

### 2.3. CSA (Charge Sensitive Amplifier)

The CSA consists of a buffered amplifier and a $R_f C_f$ feedback network (Figure 4(a)). For a fast input current pulse during $t_{\text{pulse}}$ ($\sim 20\text{ns}$), the CSA output produces a voltage swing given by:

$$\Delta V_{out,\text{CSA}} = \frac{1}{C_f} \int_{0}^{t_{\text{pulse}}} I_{in}(t)dt$$

After the input current pulse, $V_{out,\text{CSA}}$, returns exponentially to its steady level with a time constant determined by $R_f/C_f$. This time constant is chosen according to the maximum counting rate.

The buffered amplifier has an input part shown in Figure 4(b), which is a folded-cascode structure with $R_A$ and $C_A$ for feed-forward compensation [7-8]. The second cascode transistor $Q_{1\text{st}}$ is a bipolar component for better gain, speed and/or phase margin achievements. The input transistor $MP_1$ has a large $W/L$ ratio to minimize its noise contribution.

### 3. RESULTS AND DISCUSSION

Figure 5 shows the fabricated readout chip. The chip area including pads is $6.16\text{mm}^2$. Each channel occupies a surface area of $680\mu m \times 120\mu m$. The chip has been tested using a board shown in Figure 6(a).

The test board includes a structure shown in Figure 6(b), to generate an input current signal for the testing:

$$I_{in}(t) = \frac{C_f}{dV_{gen}(t)}$$

The magnitude of $I_{in}(t)$ can thus be evaluated from the waveform of $V_{gen}$. By measuring directly the magnitude of $V_{in}$, the input impedance of the current conveyor can be determined by $Z_{in} = \frac{\Delta V_{in}}{I_{in}}$. We have obtained $Z_{in} = 12\Omega$.

Figure 7 shows signal waveforms of a channel. The circuit operation is verified by observing the output signal of the current comparator $V_{out,\text{comp}}$ and that of the CSA $V_{out,\text{CSA}}$. The pulsed output of the current comparator indicates the signal event, and the output signal of the CSA gives a magnitude $\Delta V_{out,\text{CSA}}$, from which an input signal charge can be evaluated.

For signal-event detection, the detection threshold for the current comparator is set by $I_{ref}$, which can be adjusted from 100\mu A to 400\mu A.

For signal charge quantification, the conversion gain at the output of the CSA is $98\text{mV/pC}$. The evaluated noise in ENC (Equivalent input RMS Noise Charge) is $91\text{fC}$. The maximum measurable charge before saturation (limited by the current conveyor) is 10 pC. The dynamic range is 36 dB. The crosstalk between adjacent channels is 1.7% (i.e. 35 dB).
Table 1: Summary of characteristics of the designed readout ASIC

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Post-Layout results</th>
<th>Test results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption /channel(under 3.3V) @ current gain from 0.25 to 2</td>
<td>15 to 22mW</td>
<td>16 to 23mW</td>
</tr>
<tr>
<td>Input dynamic range</td>
<td>50μA(525 fC) @ gain 2</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>2.4mA(25.2 pC) @ gain 2</td>
<td>—</td>
</tr>
<tr>
<td>Input impedance @ working frequencies</td>
<td>4Ω</td>
<td>12Ω</td>
</tr>
<tr>
<td>Current Conveyor Bandwidth</td>
<td>200MHz</td>
<td>—</td>
</tr>
<tr>
<td>Current comparator Bandwidth</td>
<td>667MHz</td>
<td>—</td>
</tr>
<tr>
<td>CSA Peaking time</td>
<td>30ns</td>
<td>28ns</td>
</tr>
<tr>
<td>1-full-channel ENC</td>
<td>42ºC</td>
<td>19ºC</td>
</tr>
<tr>
<td>Xtalk</td>
<td>—</td>
<td>1.7%</td>
</tr>
<tr>
<td>Chip Size (including pads)</td>
<td>6.61 mm²</td>
<td>6.61 mm²</td>
</tr>
</tbody>
</table>

Table 1 summarizes the measured characteristics of the readout chip in comparison with post-layout simulation results.

5. Acknowledgment

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We would also like to thank Mr. E. Bechetoille and Mr Y. Zoccarato for their technical help in layout optimization and ASIC design.

References


4. Conclusion

We have designed a 16-channel readout chip in a BiCMOS process to be associated with MaPMTs or MCPs for developing a prompt gamma imaging system. Each channel is a current-mode architecture consisting of three main building blocks: a channelizer, a buffered current comparator and a CSA. Testing of the chip has shown improved characteristics compared to a reported chip with similar functions. The channel input has very low impedance (∼ 12Ω) to minimize crosstalk.