MULTI-FLEX PROTOTYPE FOR THE LAYER 2 ATLAS ALPINE STAVES LAYOUT

S. Vilalte

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Sébastien Vilalte for the LAPP ATLAS pixel group.

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Laboratoire d'Annecy le Vieux de Physique des Particules
B.P. 110 74941 ANNECY-LE-VIEUX CEDEX France.
Phone : 33 4 50 09 16 00
Fax : 33 4 50 25 94 95
e-mail : vilalte@lapp.in2p3.fr

Abstract:

LAPP is involved in the phaseII upgrade for the ATLAS pixels tracker [1].
The LAPP's group is currently designing a pixels detector layout called Alpine Staves.
This layout should allow to save matter in the detector. The silicon detectors should also cover a very high angle in the forward region. The pixel modules data transmission is an issue because of the very high number of channels and because of the high data rates.
A first study in 2014 allowed to estimate the feasibility of data transmission and powering of the pixel modules along the staves thanks to multicore flexes.
Discussions with manufactures have showed that the multicore solution is too complex in term of feasibility and cost.
A simpler solution is a multiple flex made of several double-sided cores.
This study presents the methods and principles for a transmission flex based on the Alpine layout but results can be applied to a general stave-based layout.

A prototype has been produced in 2015 and test results show the capabilities of a flex designed with real detector specifications.

1- <u>Specifications, constraints and choices.</u>

LAPP is proposing the Alpine layout for the future tracker pixel detector as a lighter and cheaper architecture. The idea of mountain modules seems to trend to a consensus around an inclined layout in the ATLAS collaboration.

One of the next challenges is to be able to recover the data from modules running at high rates. The amount of matter should also be reduced as possible.

A first prototype of a full stave is currently developed in order to prove the feasibility of the concept concerning all the different mechanics and electronics topics.

The final layout and the associated final possible lengths for "inclined staves" are not chosen yet. The architecture and the number of layers are currently discussed, so we based our study on the alpine layout layer 2.

This Layer 2 is the most representative layer as a demonstrator because of its length, of the issues on mechanics or thermal aspects and it is also representative because of high data rates and services.

Only the stave flex is discussed in this document but its design directly depends on the detector module (sensor and front-end).

1-1 <u>From the multi-core to the multi-flex solution.</u>

The previous multicore study [2] is based on a single six layers multi-cores flex.

We chose the multi-cores architecture because of the impedance matching reliability. Discussions with manufactures showed that standard processes are often not able to deal with our special specifications:

- <u>Length of the flex</u>: the maximum length of available presses is generally 90cm for sheets solutions, including technical room for process. For higher lengths, a continuous roll technic has to be used. This technic doesn't allow accurate etching as sheet pressing.
  We also met problems on multi-cores pressing for platted holes: platted holes have to be drawn oblong for position precision issues. It is a limiting factor for the connectors areas because the oblong holes should be ~2mm long and so increase too much the occupancy in the wings.
- <u>Platted holes thru the layers</u>: platted holes can be performed on a single core but getting signals through several cores needs the use of flex rigid implementation which is a local combined version of a PCB and flex. The multi-cores solution should require the use of flex rigid for the end-of-stave board connections. We estimated to 6 the number of needed connectors (78 pins each) for the layer2. It should be impossible to align, mate and unmate six micro-connectors at the same time.
- <u>Platted holes and metallization</u>: one of the most constraining specification is the loss due to radiation length and so the amount of matter. We used the thinner existing copper laminate which is basically 5µm thick. Platted holes (vias) implementation needs the platting of holes with a minimum extra-metallization of 10µm all over the copper layer.

This metallization is not possible on a selected and restricted area for continuity and current densities issues on copper tracks. The multi-core solution requires copper metallization and final copper thickness should be at least 15μm.

- Impedance matching: the serial powering tracks were foreseen to be used as reference planes for impedance matching but we can't avoid impedance mismatches due to non-continuities in these planes.

Another solution is to produce three independent double sided core flexes instead of one: the multi-flex solution. This design has several advantages:

- Power supplies: we foresaw the multi-cores design with power supplies and signals distributed to modules thanks two independent wings. The goal was to avoid platted holes. We also decided to supply the front-ends in parallel by group of two in order to have a single power supply type (1.2A) and in order to limit the voltage capability of the power supply.
Comparing to a single front-end current powering (0.6A), the drawback is a four times higher power consumption over the tracks (P~I²).
The serial powering track width is calculated to produce an acceptable thermal power dissipation. Typically, we based our calculations on standard PCB and flexes rules and we try to keep the global efficiency above 80% (see 2-4). For the multi-cores solution, we foresaw about 8mm power supplies tracks. For the multi-flex solution, we decided to reduce the current to 0.6A and so to serialize all the front-ends (see 1-2), whatever the type of module. We also take advantage of this serial solution for the flex module routing. The resulting affordable power track width is 1.6mm. It allows us to implement a large current return track, used as a reference plane. All the signals tracks can be routed with continuity over this reference plane and so we better control the impedance.
- Wings: in multicore solution, implementing two types of wings (powers and signals) increase the difficulty of production because of alignment issues. In the multi-flex solution, we fix this issue implementing only a single wing.
- Versatility: multi-cores flex is made in one part. Power supplies layers require the shorting of all the module in order to use the stave properly. We'll see the multi-flexes solution is more versatile for tests. The three flexes are totally independent and this solution is better for mounting and reworking.
- Connections: as we are able to route all the signals on the same side of the core, the goal is to implement all the connectors on this unique side at both ends, and so avoid platted holes. The connections that remain to go through the core are the power supplies. It represents only three contacts per module wing and we decided to perform these contacts using hand-soldered wires.

1-2 Specifications and choices.

- **Specifications from front-ends:**

Although not finalized, current specifications are based on physics, detector and technology. For each front-end (RD53A), we have to deal currently with:

- **Input**: **1** input data link.
  Timing and controls. Clock is locally recovered over data.
  160Mbps, DC balanced, SLVS, LPGBT compatible.
  3-bits coding enables the sharing of a single link for the module (up to 4 FE).

- **Output**: user selectable differential ports, fast serial or slow parallel.
  Fast serial: **1** CML (common mode logic) pair up to 5Gbps.
  Programmable output rate down to 1/16 (320Mbps).
  Drivers and receivers should be compatible with commercial devices and include pre-emphasis and equalization filters.
  Parallel: 4 SLVS pairs up to 2.56Gbps each.
  Programmable output rate down to 1/8 (320Mbps).
  Number of parallel outputs also programmable from 1 to 2 and 4.
  At 1.28Gbps, links should be compatible with LPGBT.

Electrical links (copper) could be up to 6m long because of opto-box location.
All links are AC coupled, DC balanced, in order to power the modules in series.

Remark: the previous numbers of inputs/outputs are the current and latest ones. The prototype has been designed with the previous assessment including two independent input lines for controls and clock. Opto-box location will be discussed in the future. The flex solution is foreseen to be implemented from the modules to the end-of-stave boards (EOS). Links from the EOS to opto-boxes have to be discussed.

- **Specifications from slow-control and powering:**

In order to limit the number of power lines and their thermal contribution, we decided to implement serial powering for modules. The front-ends are foreseen to work in this configuration thanks to special regulators.
Several architectures are possible: supplying all front-ends in parallel on modules limits the number of serialized regulators and so limits the total voltage drop but increases the total current on the line.
On the contrary, serializing the front-end chips on the modules allows to reduce the serial current but increases the total voltage drop. In order to limit the power supply lines width, we assumed that we should be able to serialize all the front-ends.
Basing our development on the last FEI4 chip, we assumed that the front-end supply current is ~0.6A and the drop voltage ~1.7V, so a ~1W power consumption per FE.
These numbers will surely evolve for next FE.
The limitation is the total voltage drop due to serialized chips. As we use several flexes, we will see in chapter 2 a possible distribution.

The modules would include a chip able to short the current in case of front-end failure and so, to insure the serial power continuity. This chip should also perform slow-control features as temperature measurement. It should be controlled by a I²C AC coupled link.

- **Specifications from layout architecture:**

Optical boxes (opto-boxes) locations are currently discussed. Because of radiation environment and difficult access for rework, opto-boxes should be located outside from the tracker. That implies 6m long copper links. In another hand, this length has to ensure the data transmission at very high speed, up to 5Gbps.
One important specification is to limit the amount of matter in the detector.
This specification is not clear in very front-end areas.
We decided to base this first stave flex design on the use of end-of-stave boards. It allows us to optimize the design in the detector area in term of matter amount. In this perspective, several scenari are possible: the end-of-stave board could include the optical transceivers, or just be a passive or active intermediate device between flexes and copper links.

- **Dimensions specifications:**

The length is limited by the manufactures capabilities. The maximum length we found is 120cm from CERN's technical support department. In the industry, the maximum is closer to 80cm.
The stave flex has been designed for the alpine layout layer2. The mechanical design constrains the modules locations and the flex width because of the mandatory individual extraction for rework. The maximum possible flex width corresponds to the minimum stave width: 24mm.
The longest flex is 120cm long.

- **Amont of matter: radiation length.**

In order to reduce the particules loss in matter, we used the thinner double sided copper-polyimide laminate available: UPICEL, *5µm copper - 50µm polyimide - 5µm copper*.
We used *12µm glue – 12µm polyimide coverlays*.
The is not currently a specification concerning losses in the matter but we started the design with a maximum radiation length loss of **X/X0=0.3%**, integrated on a **20mm** wide flex.

Cross-section stack-up:
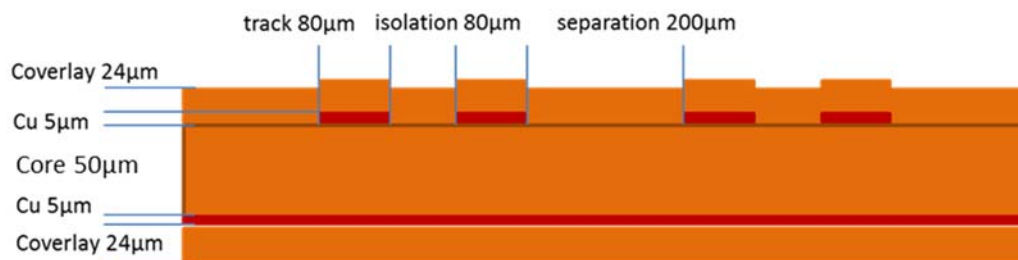
In order to achieve 100Ω differential lines impedance, we implemented lines on one side and a reference plane on the other side. We reduced the track's etching width to its minimum, according with impedance matching: 80µm tracks, 80µm isolation, 200µm separation between pairs.

We are aware that CERN's capabilities are not compatible with a large detector production. For this first prototype we decided to work anyway with CERN's specialists because of their skills and because the goal is to characterize a long flex before finding a solution for the length otself.

1-3 Geometry for the Alpine layout

Taking into account the previous specifications, we designed a set of flexes dedicated to the Alpine layout layer2.
Alpine layers include 3 different types of modules:

- Plain modules M4: 2X2 FE modules.
- Transition area modules M1: 2 FE, one plain, one mountain. These modules are treated like a M2 module because we implemented the same connection.
- Mountain M2 modules: 2 FE modules.

- **Geometry:**

The flexes are distributed on the back side of the stave (plate side, in opposition to modules side). We decided to connect modules and flex using Kyocera micro connectors. In order to ensure the individual extraction of the staves, connections are done on the back side. Modules wings will be designed to bring the signals to this location:
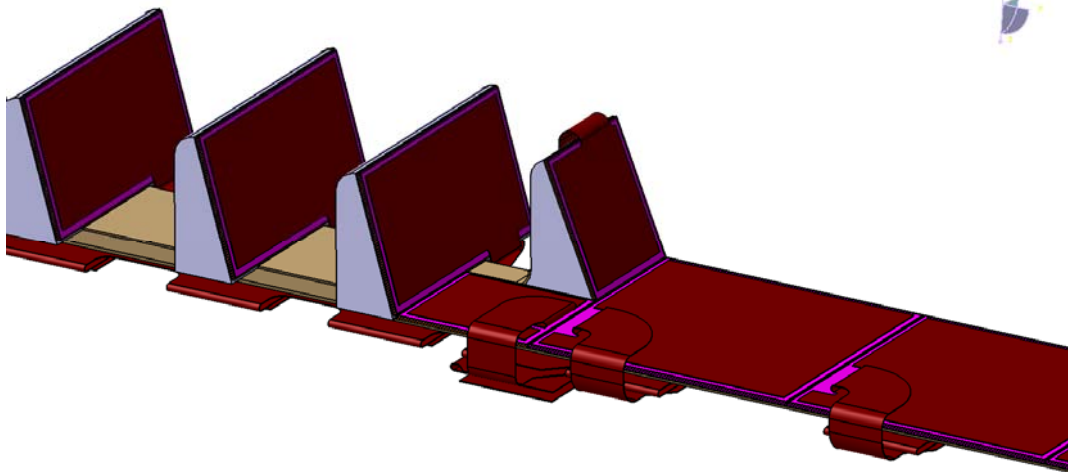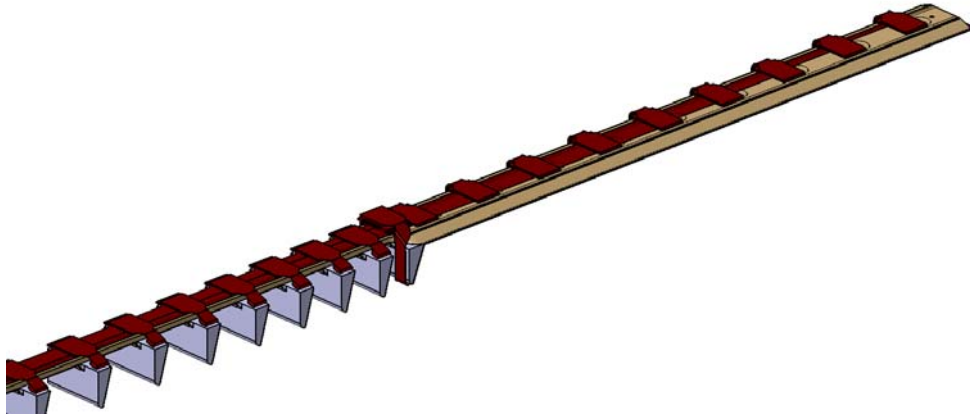
For staves extraction issues, flexes widths have to be limited to the back side flat part, 24mm maximum.

As the goal is to minimize the number of flexes and the amount of matter, we can't implement connectors on the straight main part of the flexes. As it is also impossible to implement platted holes in CERN without extra metallization, transmission lines have to be drawn from point to point on connectors with no crossing. So connectors have to be implemented on the same side of the core.

The solution is to implement connectors on wings that will be folded.

For routing reasons, all wings have to be implemented on the same edge of the flex.

The chosen Kyocera 5801 series connectors are designed for large temperature range (-40°C to 85°C), for high speed data transmission and for their size (**0.8mm mated**).

Schematic cross-section of the stave + flex, M4: in red, the flex circuits.
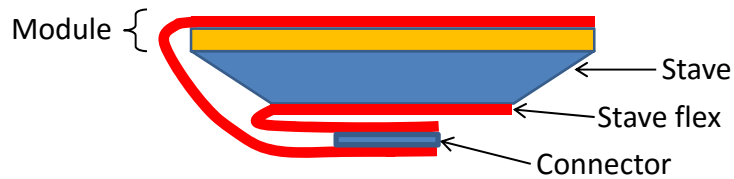
This architecture allows to test different loading and mating technics.
We could first mate the connectors and then fold & glue the ensemble on the stave flex or first fold the stave wings, glue them on the stave flex and finally mate the modules connectors.

- **Tracks distribution on sides:**

The stack-up and etching have to be respected for the transmission lines impedance matching. The differential lines are referenced to the modules power supplies current return path.
As we don't implement platted holes we decided to implement transmission lines and connectors on the same side: modules links, I²C links and high voltage lines.

On the other side, we implemented the serial powering lines:
using usual PCB rules, we estimated to **1.6mm** the width of the track for a **0.6A** serial current. Minimizing the current allows to reduce this width and so to save space for the reference plane. Serializing the front-ends supplies (0.6A) on a module will also help for the module flex routing. The lower common denominator for the current and for the different modules is **1.2A**.

As the I²C and high voltage lines doesn't need reference plane, we implemented them above the serialized current track.

So finally, the connector side of the flex includes all data links, high voltage and I²C links while the other side includes the serialized current line and the reference plane (return current path).

Example of a stave flex wing routing.

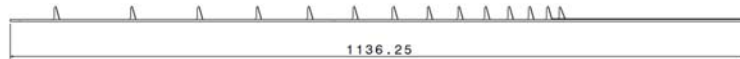In green, the top copper layer of the flex:
Data lines, HV and I²C.
In yellow, the bottom copper layer:
Serial powering lines and reference plane.
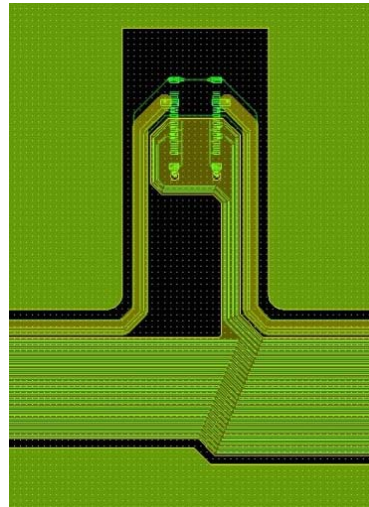
2- Design of the prototype.

The flex design is based on the alpine layer 2 stave.

Layer 2: 7 M4 plain modules + 1 transition module (2xM1 modules) + 13 M2 mountain modules.
stave length **1136.25**mm;

2-1 Modules in layer2.

As discussed in 2-1, we based the flex design on FEI4 chips.
For each module we only implement a common single clock line and a common single control line for FEs. We implemented a data line for each FE.
So we implemented the following lines for the different modules:

- **M4**: 1 line for clock, 1 line for controls, 4 lines for data.
  So, 6 differential pairs + 3 tracks for I²C + 1 track for HV + power supplies.

- Transition module & M2: 1 line for clock, 1 line for controls, 2 lines for data.
  So, 4 differential pairs + 3 tracks for I²C + 1 track for HV + power supplies.

HV track width is **200μm** and isolation from other lines is **600μm**.
I²C data lines width is **100μm**, **200μm** for its power line and isolation is **200μm**.

2-2 Flex distribution.

The goal is to concentrate the maximum modules transmission lines on flexes and so to reduce the number of flexes in the set.
We base our design on a 24mm maximum width for the main part of the stave flex. So, each flex includes the maximum number of modules it can contain. Lines of a module can't be implemented on different flexes. In order to limit the amount of matter in the detector, the flexes widths are reduced to the minimum. For each flex, we implement a single serial powering line and a single high voltage line.

Respecting the process rules (cf. 1-2), we grouped the modules as follows:

Flex 1: all 7 M4 can be implemented on a single flex, width: **22.7mm**.
    Serial powering: 7X4=**28** serialized FE, power supplies **0.6A - 28x1.7~ 48V**.

Flex 2: 7 M2 can be implemented on a single flex, width: **16.5mm**.
    Serial powering: 7X2=**14** serialized FE, power supplies **0.6A - 14x1.7~ 24V**.

Flex 3: 7 M2 can be implemented on a single flex, width: **16.5mm**.
    Serial powering: 7X2=**14** serialized FE, power supplies **0.6A - 14x1.7~ 24V**.

Remark 1: we implemented 3 flexes thanks to the maximum 24mm available width and so, for M4 modules we should have to implement a **0.6A-48V** current power supply. If the number of modules is too high, we could implement two different power lines. Next alpine staves design should reduce the available width to about 15mm. So the number of flexes should increase and the number of serialized module should decrease and so the total drop voltage. In this case the amount of matter should not change, only its distribution on flexes. We could also reduce the drop voltage by increasing the current to 1.2A.

Remark 2: in order to insure the continuity of the serial powering in the case of a failure (short-cut or open circuit), a DCS chip is currently designed to mimic the FEs. A limitation of the proposed flex architecture could be the maximum possible number of serialized FE, and so the maximum possible number of serialized DCS chips. In this case, we should implement several power lines and/or increase the serial current.


Prototype of the set of flexes.

2-3 Geometry, production and radiation length.

- **Stack-up.**

For process reasons and for a better impedance matching, we implemented all connectors and sensitive data transmission lines on one side of the flexes.
Nevertheless, we are not able to implement the connectors in the main (central) part of the flex because of transmission lines density.
The solution is to implement wings. It allows to shift the connectors from the main part and to turn connectors over by folding. In the Alpine design, the end-of-stave connectors face the stave.
So we can stack the flexes as follows: (sketch)
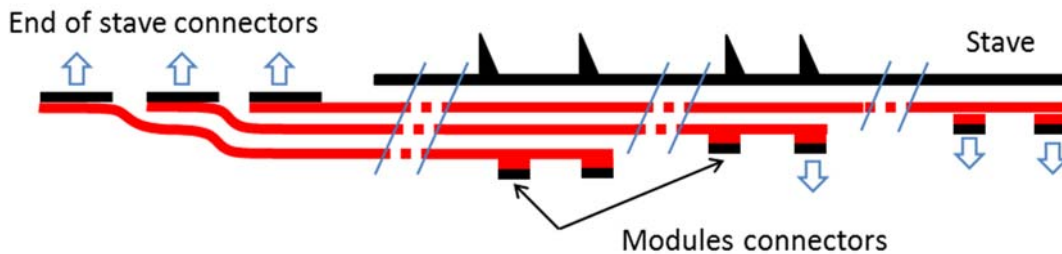
- **Radiation length.**

Concerning the amount of matter in the detector we can see there are three different areas corresponding to the three stacked flexes.
In the modules areas, the matter amount varies along the flexes because of the distribution of the modules and so the number of lines.

X0 polyimide= 28.6cm.
X0 copper= 1.44cm.

The total polyimide thickness is constant all over a flex and is **98µm**.

- **Flex 1: M4 modules.**

    Narrower part (first module, z=0): width **5.7mm**.
On TOP face: 6 differential lines 80µm, 2 lines 100µm, 2lines 200µm wide.
On BOTTOM face: 1 ground plane 2.8mm, 1 powering line 1.8mm wide.

Polyimide: X/X0=98E-6/28.6E-2=342E-6
    20mm equivalent X/X0=342E-6x(5.7/20)=**98E-6.**
Total equivalent copper thickness over the flex:
    (((6x80E-6)+(2x1E-6)+(2x2E-6)+2.8E-3+1.8E-3)/5.7E-3)x5E-6=5E-6m
    X/X0=5E-6/1.44E-2=347E-6
    20mm equivalent X/X0=347E-6x(5.7/20)=**99E-6.**

Total 20mm equivalent X/X0=**197E-6≈0.02%**

      <u>wide part</u> (stave): width **21.5**mm.
On TOP face: 42 differential lines 80µm, 2 lines 100µm, 2lines 200µm wide.
On BOTTOM face: 1 ground plane 18.7mm, 1 powering line 1.8mm wide.

Polyimide: X/X0=98E-6/28.6E-2=342E-6
      20mm equivalent X/X0=342E-6x(21.5/20)=**368E-6.**
Total equivalent copper thickness over the flex:
      (((42x80E-6)+(2x1E-6)+(2x2E-6)+18.7E-3+1.8E-3)/21.5E-3)x5E-6=5.7E-6m
      X/X0=5.7E-6/1.44E-2=396E-6
      20mm equivalent X/X0=396E-6x(21.5/20)=**426E-6.**

Total 20mm equivalent X/X0=**794E-6≈0.08%**

- **Flex 2 & 3: M2 modules.**

      <u>Narrower part</u> (first module, z=0): width **4.8**mm.
On TOP face: 4 differential lines 80µm, 2 lines 100µm, 2lines 200µm wide.
On BOTTOM face: 1 ground plane 2mm, 1 powering line 1.8mm wide.

Polyimide: X/X0=98E-6/28.6E-2=342E-6
      20mm equivalent X/X0=342E-6x(4.8/20)=**82E-6.**
Total equivalent copper thickness over the flex:
      (((4x80E-6)+(2x1E-6)+(2x2E-6)+2E-3+1.8E-3)/4.8E-3)x5E-6=4.9E-6m
      X/X0=4.9E-6/1.44E-2=341E-6
      20mm equivalent X/X0=341E-6x(4.8/20)=**82E-6.**

Total 20mm equivalent X/X0=**164E-6≈0.016%**

      <u>wide part</u> (stave): width 15.4mm.
On TOP face: 28 differential lines 80µm, 2 lines 100µm, 2lines 200µm wide.
On BOTTOM face: 1 ground plane 12.5mm, 1 powering line 1.8mm wide.

Polyimide: X/X0=98E-6/28.6E-2=342E-6
      20mm equivalent X/X0=342E-6x(15.4/20)=**263E-6.**
Total equivalent copper thickness over the flex:
      (((28x80E-6)+(2x1E-6)+(2x2E-6)+12.5E-3+1.8E-3)/15.4E-3)x5E-6=5.6E-6m
      X/X0=5.6E-6/1.44E-2=390E-6
      20mm equivalent X/X0=390E-6x(15.4/20)=**300E-6.**

Total 20mm equivalent X/X0=**563E-6≈0.056%**

So the matter amount impacts the X/X0 over the stave as follows:

Remark:
Due to the distribution and to the thicknesses of laminates, the contributions of copper and polyimide are equivalent. Companies with a 5µm copper laminate process are rare. As 9µm copper thickness is a standard, we can assume that the use of a 9µm copper thickness will increase X/X0 by a factor **1.4**. Even with such a factor, we still respect the specifications (<0.3%).

The matter amount due to the wings is not included in the previous calculations. We can calculate their contribution for M2 and M4 modules, 20mm wide equivalent: Whatever the module type, the wing surface is **30x15mm=450mm².**

- **M4:**
The total copper surface is ≈250mm², so an equivalent copper thickness of (250/450)x5E-6=2.8E-6m.
20mm equivalent polyimide X/X0: (30/20)x342E-6=**588E-6**
20mm equivalent copper X/X0: (30/20)x(2.8E-6/1.44E-2)=**292E-6**
Total M4 20mm equivalent X/X0=**880E-6≈0.09%.**

- **M2:**
The total copper surface is ≈230mm², so an equivalent copper thickness of (230/450)x5E-6=2.56E-6m.
20mm equivalent polyimide X/X0: (30/20)x342E-6=**588E-6**
20mm equivalent copper X/X0: (30/20)x(2.56E-6/1.44E-2)=**266E-6**
Total M4 20mm equivalent X/X0=**854E-6≈0.085%.**

So, locally X/X0 can increase by **~0.09%** for M2 and M4 modules. The maximum X/X0 will be for the three flexes pilled-up plus a module **≈0.29%**, which matches with the maximum 0.3% specification.

In order to compare with others transmission solutions (twinax, twisted pairs…), we can estimate the contribution of a single transmission pair on the flex, taking into account copper, polyimide and isolations:
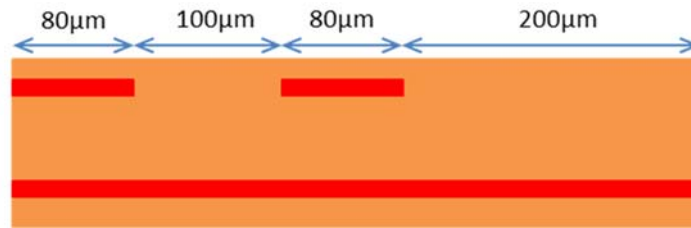
Taking into account the needed 200µm isolation between two transmission pairs, this element is 460µm wide.

Polyimide: $X/X_0 = 98E\text{-}6/28.6E\text{-}2 = \textbf{342E-6.}$
Total equivalent copper thickness over the 460µm element:
  $(((2x80E\text{-}6)+460E\text{-}6)/460E\text{-}6)x5E\text{-}6 = 6.7E\text{-}6\,m$
  $X/X_0 = 6.7E\text{-}6/1.44E\text{-}2 = \textbf{465E-6.}$

  Total $X/X_0 = \textbf{807E-6}$ for a **460µm** wide element.

This number has to be multiplied by **(W/460E-6)**, with W the reference width of comparison.

2-4 <u>Mechanical and thermal aspects.</u>

- **Mechanical attachment:** the produced set of flexes has not been designed in order to be attached on the stave. Solutions should come from a discussion with mechanical designers.
An important point to take care about is the differential length between flexes and staves due to different CTEs (Coefficient of thermal expansion).
The detector will be assembled at ≈+20°C and cooled at ≈-40°C, so a full ≈60°C temperature range.
    Carbon: α_c=-7.6E-7 (1/K).
    Flex: α_f≈20E-6 (1/K).
We can calculate the staves (ΔS) and flexes (ΔF) lengths variations over a maximum -60°C temperature range:
    Stave length=1136mm, **ΔS=52μm**, **ΔF=-1.36mm.**

We can see that the major part of the variation comes from the flexes.
We will have to design the flexes longer in order to compensate their contraction.
Mechanical attachment will take it into account.
Flex modules wings will be also de designed in order to allow the differential sliding in order to prevent any effort on the connectors.

- **Power consumption on serial powering:**

    Serial powering allows to reduce the number of powering lines from one for each module to one for all the serialized modules and so allows to reduce the matter amount. On modules, specific regulators should provide a local stable power supply voltage for FEs and adapt the input drop voltage in order to be supplied with a constant current.
    Basing the design on FEI4 chips and on first FE65 specifications, we assumed that we can use two different current values: **0.6A** and **1.2A**.
    Power consumption on the powering lines is due to their resistance.
    The return path for supply current is used as a reference plane for transmission lines. It is wide and so its resistance is negligible in front of the serialized input current track. The flexes will not be in continuous contact with the staves, the heat produced by the lines should be mostly drained by connectors and so by the modules.
    Copper resistivity depends on temperature: ρ[-40°C]=13E-6 Ω.mm and ρ[20°C]=17E-6 Ω.mm.
    The difference is slight and we are not able to foresee the final steady copper temperature. We took ρ=15E-6 Ω.mm as an average value for calculations.
    It corresponds to a temperature of -5°C, a (impossible) worst case.

With L the length, W the width and T the thickness, we can calculate the resistance as follows:

$$Rlin = \frac{L \times \rho}{T \times W}$$

Implementing **1.8mm** wide current lines, we can calculate the resistance and the power consumption for the three flexes:

- **Flex 1: 7 M4 modules.**
Total length of the power line, including wings: **1419mm**.
The total resistance is

$$Rlin = \frac{1419 \times 15.10^{-6}}{0.005 \times 1.8} = \mathbf{2.37\Omega}$$

It corresponds to a total power consumption of:
I=0.6A, Pflex=0.6²x2.37=**0.85W.**
I=1.2A, Pflex=1.2²x2.37=**3.41W.**

The flex 1 supplies 7x4=**28** front-ends. Assuming a FE power consumption about **1W** (minimum), the total FE power consumption should be about **Pfe=28W**.
We can estimate the serial power efficiency E for the two possible currents:
I=0.6A, E=(1-(0.85/28))x100≈**97%**.
I=1.2A, E=(1-(3.41/28))x100≈**88%**.

- **Flex 2: 7 M2 modules.**
Total length of the power line, including wings: **1188mm**.
The total resistance is

$$Rlin = \frac{1188 \times 15.10^{-6}}{0.005 \times 1.8} = \mathbf{2\Omega}$$

It corresponds to a total power consumption of:
I=0.6A, Pflex=0.6²x2=**0.72W.**
I=1.2A, Pflex=1.2²x2=**2.88W.**

The flex 2 supplies 7x2=**14** front-ends. Assuming a FE power consumption about **1W** (minimum), the total FE power consumption should be about **Pfe=14W**.
We can estimate the serial power efficiency E for the two possible currents:
I=0.6A, E=(1-(0.72/14))x100≈**95%**.
I=1.2A, E=(1-(2.88/14))x100≈**79.5%**.

- **Flex 3: 7 M2 modules.**

Total length of the power line, including wings: **954mm**.
The total resistance is

$$Rlin = \frac{954 \times 15.10^{-6}}{0.005 \times 1.8} = \mathbf{1.6\Omega}$$

It corresponds to a total power consumption of:
I=0.6A, Pflex=0.6²x1.6=**0.58W.**
I=1.2A, Pflex=1.2²x1.6=**2.3W.**

The flex 1 supplies 7x2=**14** front-ends. Assuming a FE power consumption about
1W (minimum), the total FE power consumption should be about Pfe=14W.
We can estimate the serial power efficiency E for the two possible currents:
I=0.6A, E=(1-(0.58/14))x100≈**96%**.
I=1.2A, E=(1-(2.3/14))x100≈**84%**.

The total flex power consumption and efficiency over the stave can be
calculated:
I=0.6A, Pflex=**2.15W**, Pfe=**56W**, E=(1-(2.15/56))x100=**96%**.
I=1.2A, Pflex=**8.6W**, Pfe=**56W**, E=(1-(8.6/56))x100=**85%**.

Conclusion:

Matter amount estimation show the benefit of the serial powering scheme in
front of a parallel powering. It also allows the use of the return current path as a
reference plane. Efficiency calculations show the advantage of a current as low as
possible. With a **0.6A** serial current, the total efficiency is **96%**. With a **1.2A**
current, the efficiency decreases to **85%** which is not a bad result but in this case,
thermal effects of the flexes should be taken into account in the cooling.

3- <u>Tests results: data rates.</u>

The goal is to estimate the maximum transmission data rates according to the detector specifications. Depending on the layers from 0 to 4, the expected rates are from **320Mbps** to **5Gbps** per FE. The clock and control should be transmitted at **160Mbps**.
Two different transmission standards are discussed:

- **SLVS**: differential current generator technology, similar to LVDS.
  Rates from **160Mbps** to **1.2Gbps**.
- **CML**: differential transmission thanks to two 50Ω generators.
  Rate up to **5Gbps**.

We estimated the maximum length of the flex for maximum foreseen LVDS and CML rates. We produced the *Signal Integrity* board which allows to inject data on the wings connectors and so to emulate the modules. At the other side of the flex, data are recovered from the end-of-stave board connectors. This board is plugged on a PCIe very high speed board. On it, a FPGA is programmed for a pseudo random bit injection and Bit Error Rate counting (BER). The transmissions have been tested both in streaming and packet configurations. We used 8b10b coding.
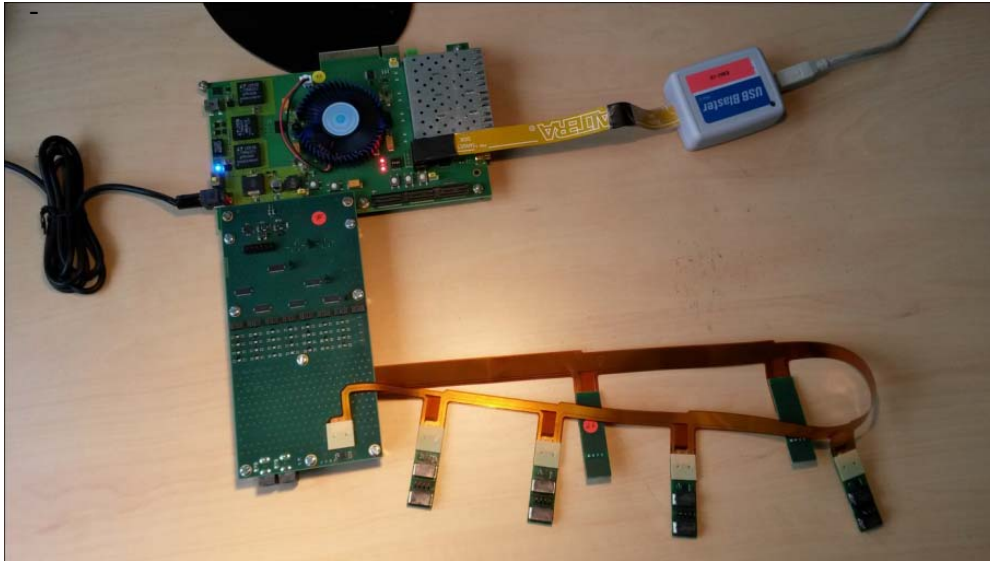We implemented CML drivers on the signal integrity board in order to avoid the effects of cascaded connectors.
We tested the transmissions on the modules wings until **BER>1E-12.**
We tested the crosstalk on adjacent lines from a module.
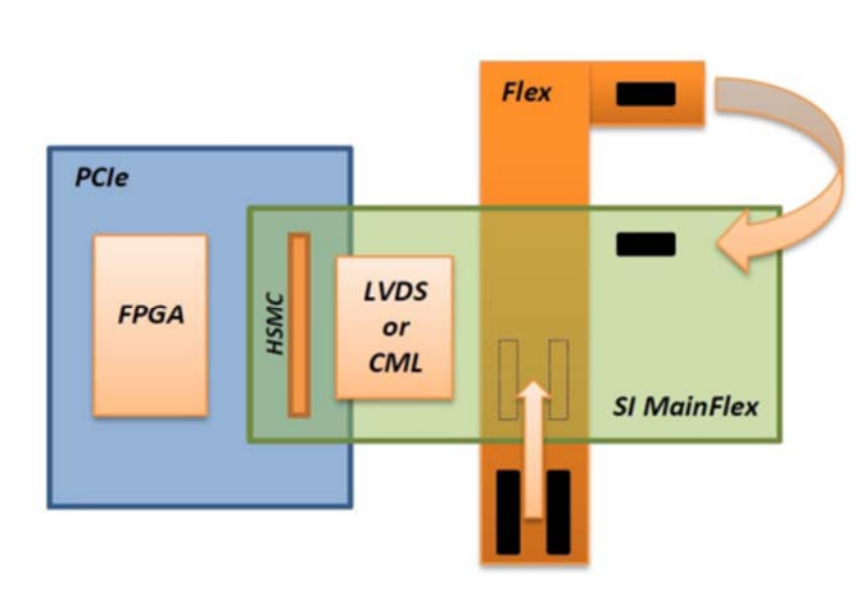
This configuration allows to test data rates over the flex, including the connectors.

The *Signal Integrity* board, the PCIe board and a flex.

Tests results:

The numbering of the wing begins at z=0. i.e, wing#1 corresponds to the longer lines on the flex.

- LVDS, data streaming:
  Pattern : PRBS-31
  Data rate : **1.2Gbps**
  Coding : 8b10b
  NumberCount : 1E+12 Bits
  BER : 0 for wings up to **0.76m** (wing#7). No crosstalk over 4 adjacent pairs.

- LVDS, packets:
  Pattern : PRBS-31
  Data rate : **1.2Gbps**
  Coding : 8b10b
  NumberCount : 1E+12 Bits
  BER : 0 for wings up to **0.95m** (wing#3). No crosstalk over 4 adjacent pairs.

For LVDS transmissions we noticed that we have a "discrete effect" on the wing number transmission due to the high susceptibility of LVDS to attenuation.
I.e. for wing#3, BER=0 while errors are too many for wing#2.

- <u>CML, data streaming</u>:
  Shaping : Pre-Emphasis& Linear Equalization
  Pattern : PRBS-31
  Coding : 8b10b
  NumberCount : 1E+12 Bits
  Data rate : **4.6Gbps** Max, BER=0 for all the wings (120cm).
  No crosstalk over 4 adjacent pairs.

- <u>CML, data streaming</u>:
  Shaping : Pre-Emphasis& Linear Equalization
  Pattern : PRBS-31
  Coding : 8b10b
  NumberCount : 1E+12 Bits
  Data rate : **5Gbps** Max, no crosstalk over 4 adjacent pairs.
         Channel#1 => BER : 5E-11 for wing#1 (120cm).
         Channel#2 => BER : 3E-11 for wing#1 (120cm).
         Channel#3 => BER : 0 for wing#1 (120cm).
         Channel#4 => BER : 0 for wing#1 (120cm).

<u>Conclusion:</u>
LVDS tests have shown good results with packets configuration up to **95cm** with no crosstalk between lines.
CML tests have shown that current specifications of **5Gbps** data rates are possible but the use of pre-emphasis and equalization filters is mandatory.
These tests have been performed using a single synchronous system for the injection and reception (PCIe board). In the detector, the system will be formed by two independent electronics: the floating serial powered front-end and the read-out system. This configuration has to be tested in the future.

4- <u>Conclusions and perspectives.</u>

This first prototype proved that flexes are a good solution for the modules data transmissions and powering from the end of stave boards. Tests results showed that data rates can match with the current FE specifications of maximum 5Gbps. The prototype has been designed specifically for the alpine layout layer 2 stave but the principle can be adapted to any of the proposed layouts in the collaboration. Results on the use of shaping (pre-emphasis & equalization) are a useful input for the FE designers.
Solutions for a complete transmission are currently discussed in the collaboration. Boards at the end of staves (End Of Stave boards) should not be able to perform the optical conversion to optical fibers because of radiations. A solution could be to transfer data over micro-twinax cables from EOS bards to opto-box (optical conversion boards) placed in a safer location. Estimated length of added cables is about 6m. Next developments will allow to test the flex+twinax chain, using or not buffers that can be implemented on the EOS board.
These results will be useful for the collaboration.

The set of flexes has been produced at CERN. It allowed us to learn a lot on processes but CERN has not the capability for a production of a large number of them, typically for a detector. Next prototype has to be produced by a specialized company.
Industrial flex length is limited to 90cm because of automated processes with laminate sheets. Roll processes can achieve longer flexes but with less precision, particularly on etching.
A solution is to fold flexes as snakes in order to produce flexes longer than 90cm. Standard available laminate is 9μm copper thick. In front of 5μm, it should represent an increase of **25%** of the X/X0. Industrial manufacturers are also able to implement selective metallization of holes that should allow vias without extra matter for metallization.

References:

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