LHCb level-0 muon trigger

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Abstract. The LHCb experiment will study CP violation and rare phenomena using the b-hadrons copiously produced by the LHC, at CERN. A powerful trigger system is required to select efficiently b-hadron decays of interest, while reducing the 40 MHz input rate to a level acceptable for tape storage systems. This document gives an overview of one part of the LHCb trigger system: the level-0 muon trigger.

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1 Introduction

LHCb is an experiment dedicated to the study of CP violation and rare decays in b-hadron sector. It is in preparation at CERN. The Large Hadron Collider (LHC) will provide the LHCb detector with proton-proton interactions at a luminosity around 2×10^{32} cm^{-2}s^{-1} and a center of mass energy of 14 TeV. The challenge for the LHCb trigger system is to select efficiently b-hadron decays of interest while reducing the 40 MHz input event rate by 6 orders of magnitude. For this purpose, the two main characteristics of the b-hadrons are exploited: presence of high transverse momentum particles in the decay products and displaced decay vertex. The trigger system is subdivided into three main levels:

- The level-0 trigger searches for hadrons, electrons, muons, photons and π^0, with high transverse energy using calorimeters and muon detector information. Multiple interactions are rejected by a dedicated device, located upstream of the vertex detector. The level-0 trigger reduces the input rate from 40 to 1 MHz in 4 μs.
- The level-1 trigger refines the b selection by looking for a displaced secondary vertex, using the vertex detector information. It reduces the rate from 1 MHz to 40 kHz well within the maximum allowed latency of 1.7 ms.
- The final selection of specific b-hadron decay channels uses the full detector information. It is done on a computer farm and the selected events are written to a tape storage at a rate of 200 Hz.

The LHCb experiment is described in detail in [1–7]. This document gives an overview of the muon trigger. We explain the algorithm used to search for muon tracks. We present the general architecture of the muon trigger, some details of the hardware implementation and some prototype results.

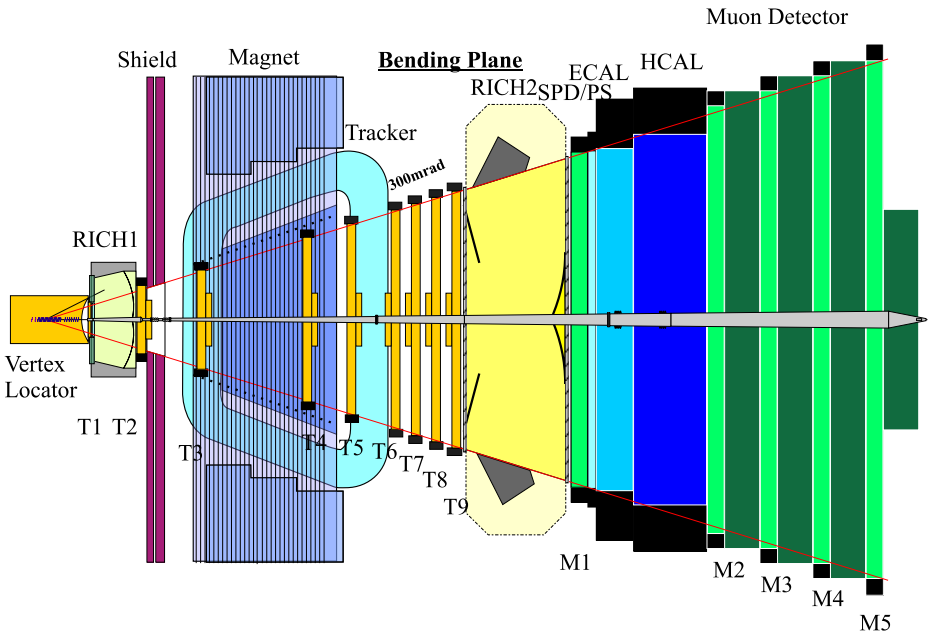

Fig. 1. The LHCb experiment. The five muon stations (M1 to M5) are indicated

2 Algorithm of the muon trigger

The level-0 muon trigger uses the property of muons resulting from b-hadrons decay to have high transverse momentum, P_T, compared to muons coming from kaons and pions decaying in flight. The high P_T muons are interesting to select channels like $B_d^0 \to J/\psi K_s^0$, $B_s^0 \to J/\psi\phi$, $B_s^0 \to \mu^+\mu^-$ or $B \to K^{*0}\mu^+\mu^-$. They also provide a tag of initial b flavour, when the other b-hadron in the event decays semileptonicaly.

The LHCb muon detector consists of five stations as shown in Figure 1. The muon trigger searches straight track segments in these five stations. The search starts by looking for a seed in station M3. A road is then opened in the other stations and a candidate is selected if at least one hit is found in each station within a certain Field of Interest (FOI). The pads found in station M2 and M3 are used to extrapolate to station M1. The transverse momentum is then computed using the impact points and the slope in station M1 and M2 and the P_T-kick induced by the magnetic field.

3 General architecture

The segmentation of the muon system is shown in Figure 2. It is very regular and projective with respect to the interaction point. This regularity is important for the trigger implementation, as explained below. Each station is divided into

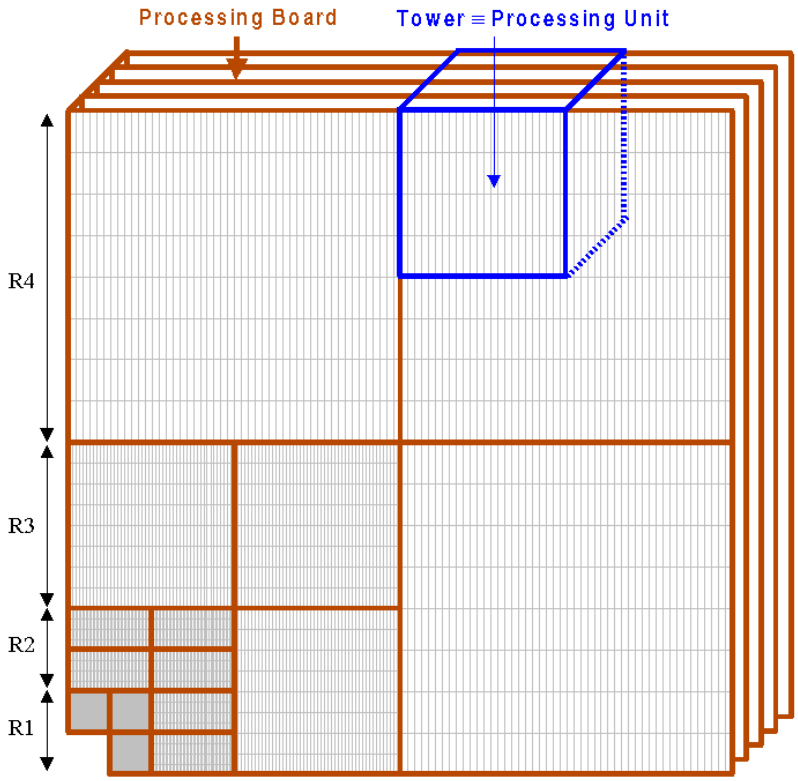

Fig. 2. Segmentation of a quarter of the muon system in a plane perpendicular to the beam axis. The full system is projective with respect to the interaction point. Areas served by processing units and processing boards are indicated.Each chamber has four regions with different pad granularity, indicated by R1 to R4

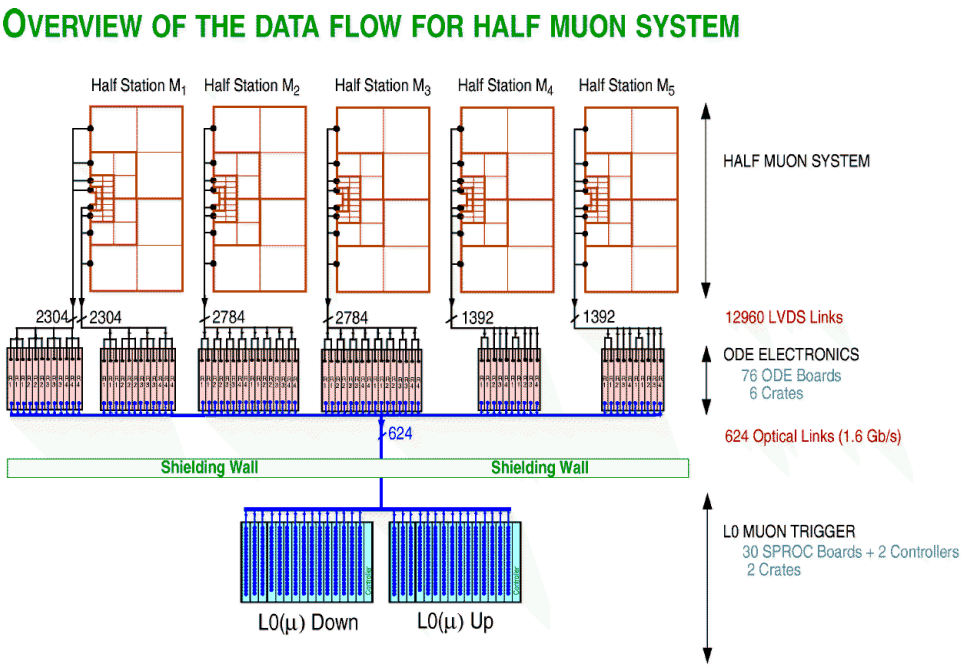

Fig. 3. Data flow for half a muon system. The flow of data from the muon detector to the frond end electronics (ODE) and to the trigger is indicated

four regions. In each region, the pad granularity increases by a factor two with respect to the adjacent inner region. The muon system is divided in 192 towers which point towards the interaction point. All data from a tower are collected by one entity called Processing Unit (PU). Each quarter of the muon system is connected to an independant processor containing 15 processing boards housed in one crate. One processing board contains four PUs.

An overview of the data flow, for half a muon system is shown in Figure 3. The five muon stations are connected to the Front End electronics via LVDS links. Physical muon detector cells are combined in 26000 logical channels. They represent pads or strips depending on the station and region. Logical channels data are sent to the trigger every 25 ns, via 1248 high speed optical links. This allows to place the trigger crates behind the shielding wall, so that they are insensitive to radiation and especially to Single Event Upsets (SEU). The trigger architecture is massively parallel, synchronous with the LHC bunch crossings and pipelined.

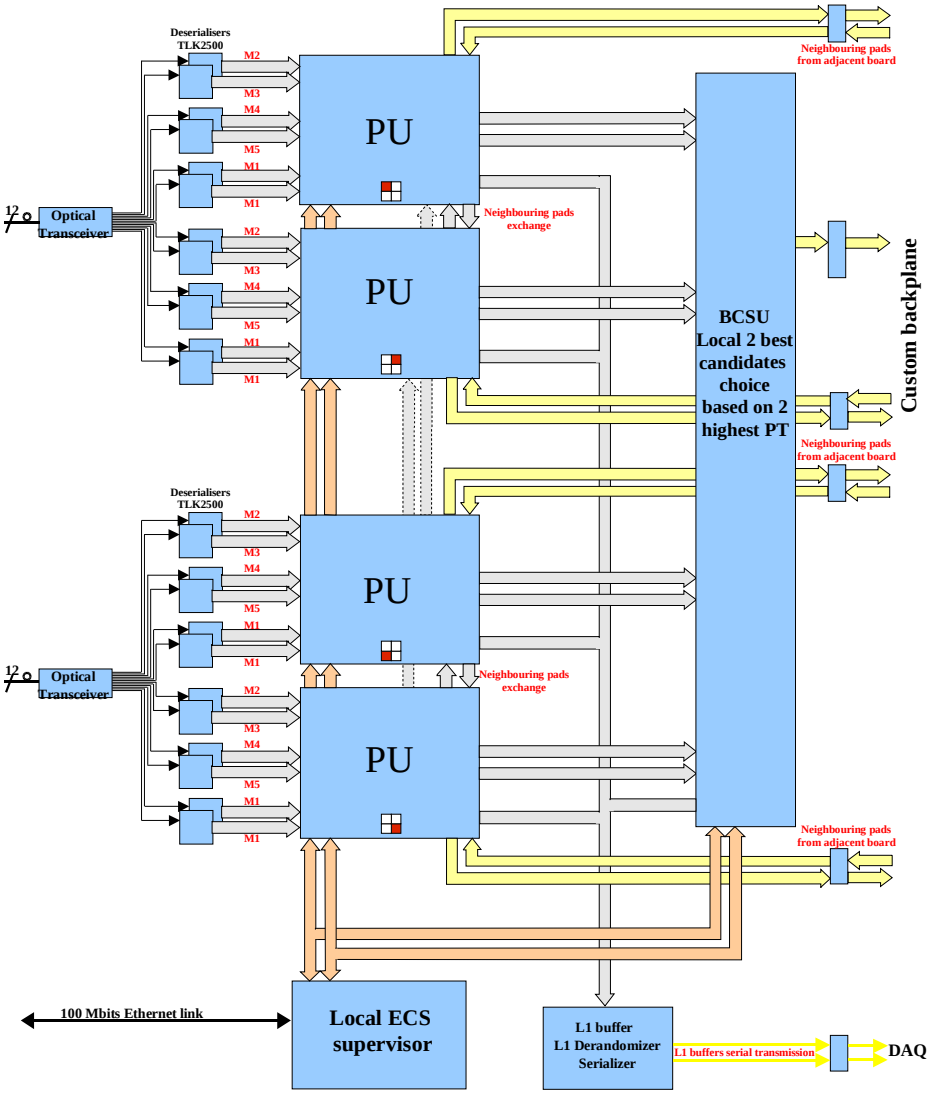

Fig. 4. Scheme of the processing board

4 Details of the hardware implementation

One of the advantages of this architecture is that we use a unique processing board, represented in Figure 4. The data from the five muon stations arrive through 24 optical links to the board. They are deserialized and transmitted to the four PUs. Each PU finds muon candidates and sends them to a second entity called Best Candidate Selection Unit (BCSU). It is in charge of selecting the 2 candidates with the highest P_T. A dedicated part of the board is used for monitoring, debugging and to send data to the DAQ[1]. It allows to keep in memory a copy of inputs and results for each component of the board. In debugging mode, the principle is to inject test patterns on the optical link buffers, run the processing board, read results and compare them with the simulation. In running mode, it is possible to set parameters like the size of the FOI and the LUT content within PU. The local ECS[2] supervisor allows to read error counters, perform local resets and events capture.

The architecture of a PU is shown in Figure 5. A PU receives 6 optical links from the five muon stations: one link for station Mi (i=2,...,5) and two for station M1. After synchronisation with the LHC bunch crossings, the muon identification starts. The pad finding in M1 and the selection are performed. The P_T is computed using Look-Up Tables (LUT). All this work can be done using only logical operations. A PU exchanges data with its neighbours on the same board, but also with PU on other boards, via a custom backplane. The simulation of a PU, using VHDL code shows that it fits into a big FPGA with 600,000 gates, 488 inputs/outputs and 150 memory blocks. Thus, an Altera APEX20K600 fulfills our needs.

5 Prototype results

We have performed several prototypes to validate key points of our architecture. Only the high speed optical link tests are presented here. The goals were to measure the bit error rate (BER), the clock jitter influence on the bit error rate and the sensitivity to SEU.

We have designed a board which is used both for signal emission and reception. It is shown in Figure 6. The board is composed of an FPGA, a serializer/deserializer (TLK 2501) and an optical transceiver. In emission, the FPGA generates bit patterns at 40 MHz which are serialized at 1.6 GHz by the TLK chip. The optical transceiver pushes them in the optical fibers. In reception, data follows the other way round and are analysed by the FPGA, which allows to count the errors.

We have measured the bit error rate with clock presenting various jitters. With a jitter of 100 ps, the BER is below 10^{-14}, which is excellent. With a clock jitter of 300 ps, which is roughly the one provided by the LHC timing system, the BER increases to 10^{-3}. This is too high thus we are studying a setup to filter this clock.

[1] Data Aquisition System
[2] Experimental Control System

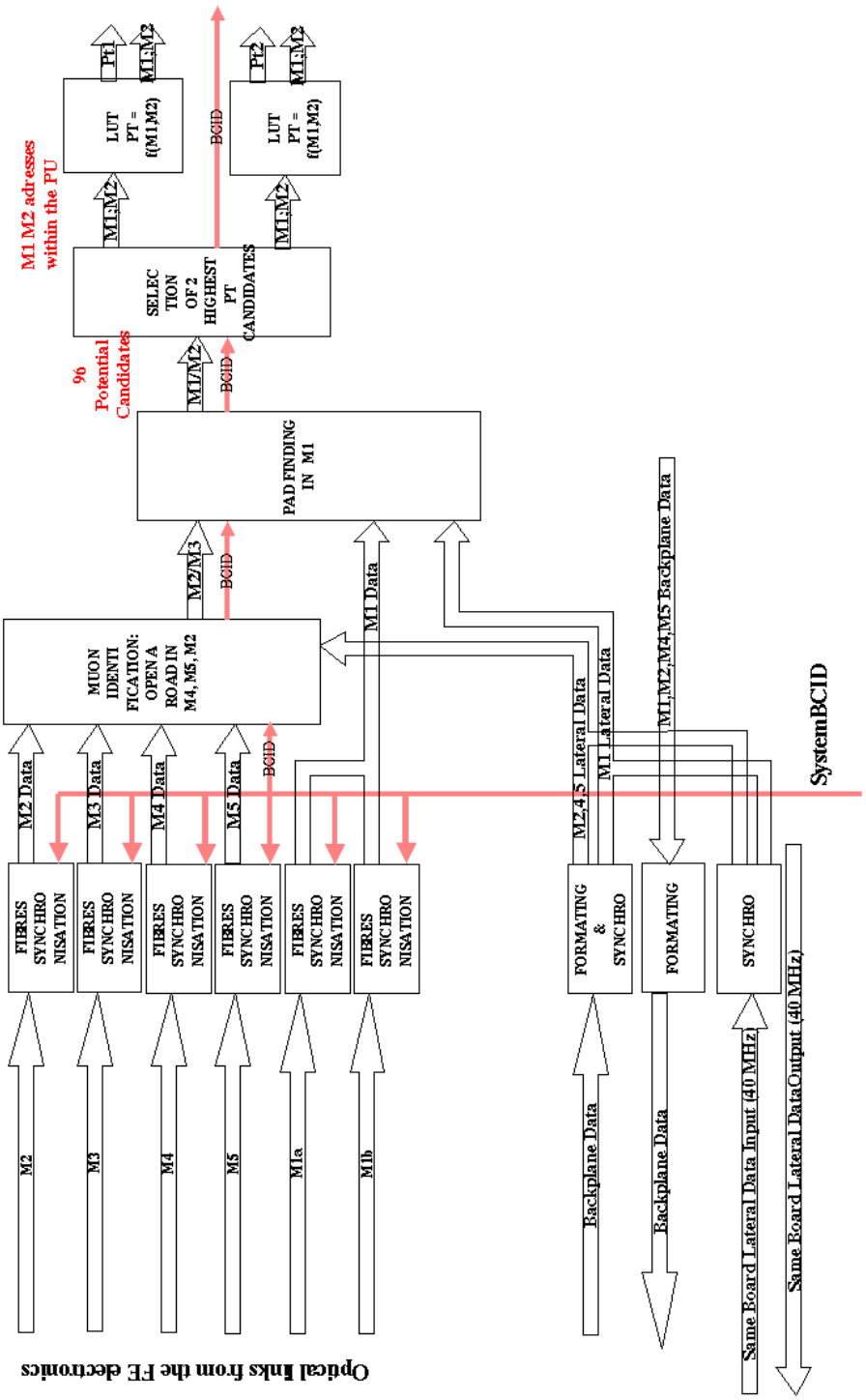

Fig. 5. Scheme of the processing unit

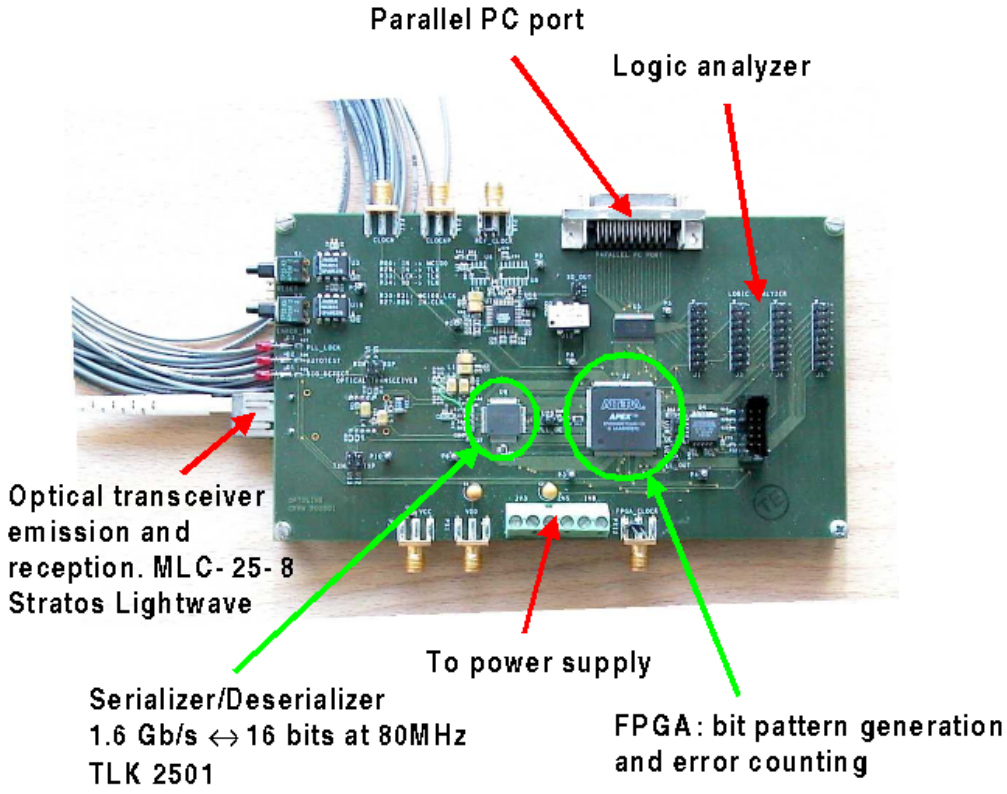

Fig. 6. Picture of the board used for optical links tests

We have measured sensitivity to SEU using a 60 MeV proton beam in the Cyclotron Research Center of Louvain-La-Neuve. In the LHCb muon detector environment, we observed an equivalent of 2 SEU per device per year on the optical transceiver chip and 1 SEU per device per year on the serializer. We conclude that the optical link devices present a good immunity to SEU.

6 Conclusion and prospects

LHCb has a powerful Level-0 muon trigger. It is based on macro FPGA's and high speed optical links. It is massively parallel, synchronous with the LHC bunch crossings and pipelined. It is immuned to single event upsets. It is housed in four 9U crates and it reaches the design physics performance. As an example, the selection efficiency of $B_d^0 \to J/\psi K_s^0$ events is $\sim$80% in nominal conditions.

We will build the first full scale processing board in 2002.

References

1. LHCb Collaboration, "LHCb Technical Proposal", CERN/LHCC/98-4, LHCC/P4, 20 February 1998.
2. LHCb Collaboration, "LHCb Outer Tracker Technical Design Report", CERN/LHCC/2001-024, LHCb TDR 6, 14 September 2001.
3. LHCb Collaboration, "LHCb VELO Technical Design Report", CERN/LHCC/2001-011, LHCb TDR 5, 31 May 2001.
4. LHCb Collaboration, "LHCb Muon system Technical Design Report", CERN/LHCC/2001-010, LHCb TDR 4, 28 May 2001.
5. LHCb Collaboration, "LHCb RICH Technical Design Report", CERN/LHCC/2000-0037, LHCb TDR 3, 7 September 2000.
6. LHCb Collaboration, "LHCb calorimeters Technical Design Report", CERN/LHCC/2000-0036, LHCb TDR 2, 6 September 2000.
7. LHCb Collaboration, "LHCb magnet Technical Design Report", CERN/LHCC/2000-007, LHCb TDR 1, 17 December 1999.
8. E. Aslanides et al., "A synchronous architecture for the L0 muon trigger", LHCb note 2001-010, January 23, 2001.