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## Front end electronics for silicon tungsten calorimeter

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**FRONT END**

**ELECTRONICS FOR**

**SILICON TUNGSTEN**

**CALORIMETER**

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# PLAN

**I– REQUIREMENTS**

**II– A DESIGN**

**III– ADAPTATIVE STAGE**

**IV– SHAPER**

**V– CODING**

**VI– FIRST IDEAS FOR ADC**

**CONCLUSION**

# I- REQUIREMENTS

**Maximum energy : up to 1 Tev.  
=> bunch crossing 150ns.**

**Time signal : between 20ns–60ns.**

**Train = 3000 bunch crossing.**

**One Train every 200ms.**

**Dynamic = signal/noise = 14–15 bits.**

**Accuracy: 0,4 % so 8 bits.**

**30 Millions channels with 4mW/channel max.**

**128 channels/chip so 240.000 chips.**

# SOME IDEAS

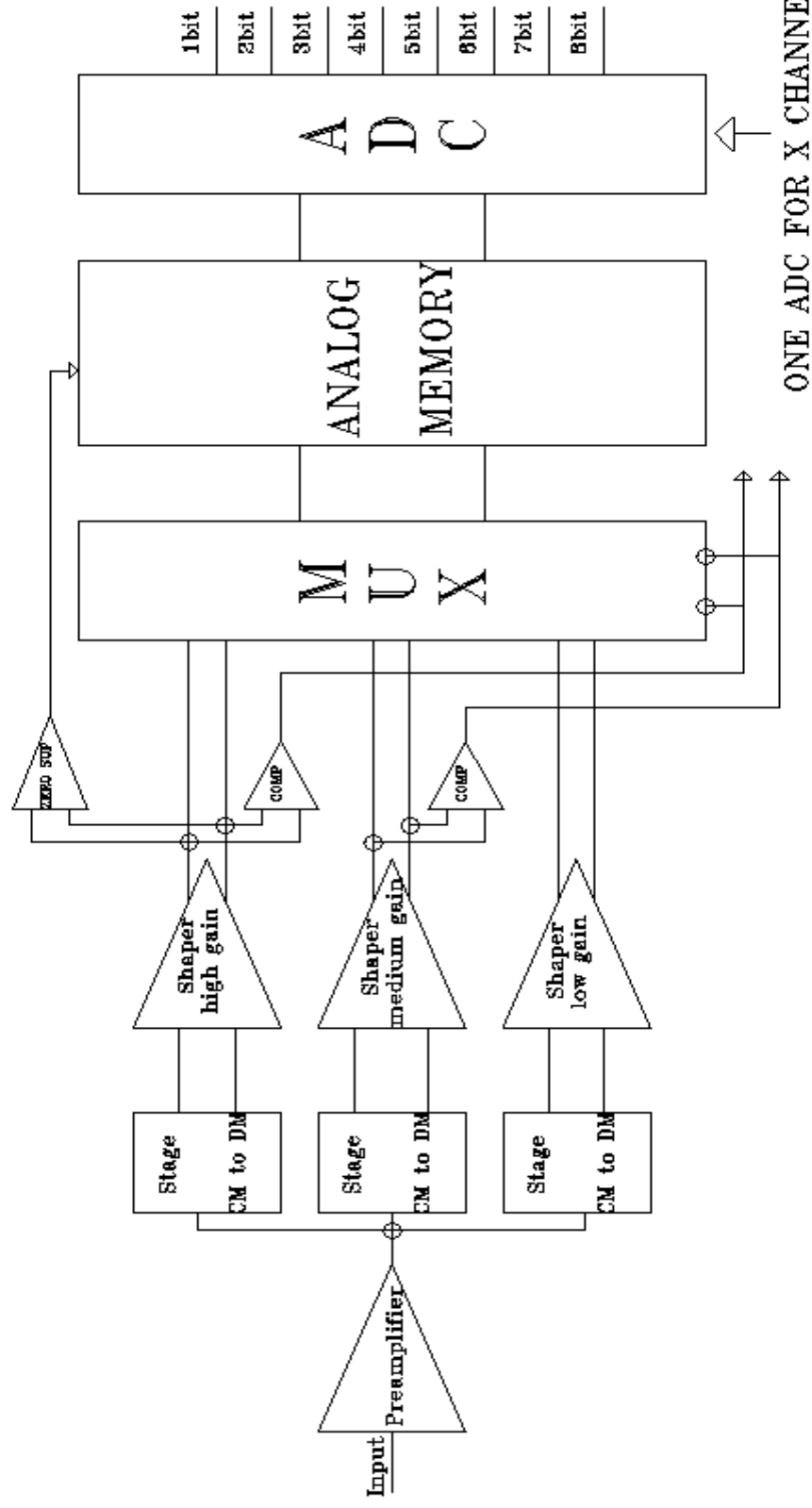
**Accuracy < Dynamic so multi gain wih choice of gain :**

**– No preamplifier with multi–gain : possibility??**

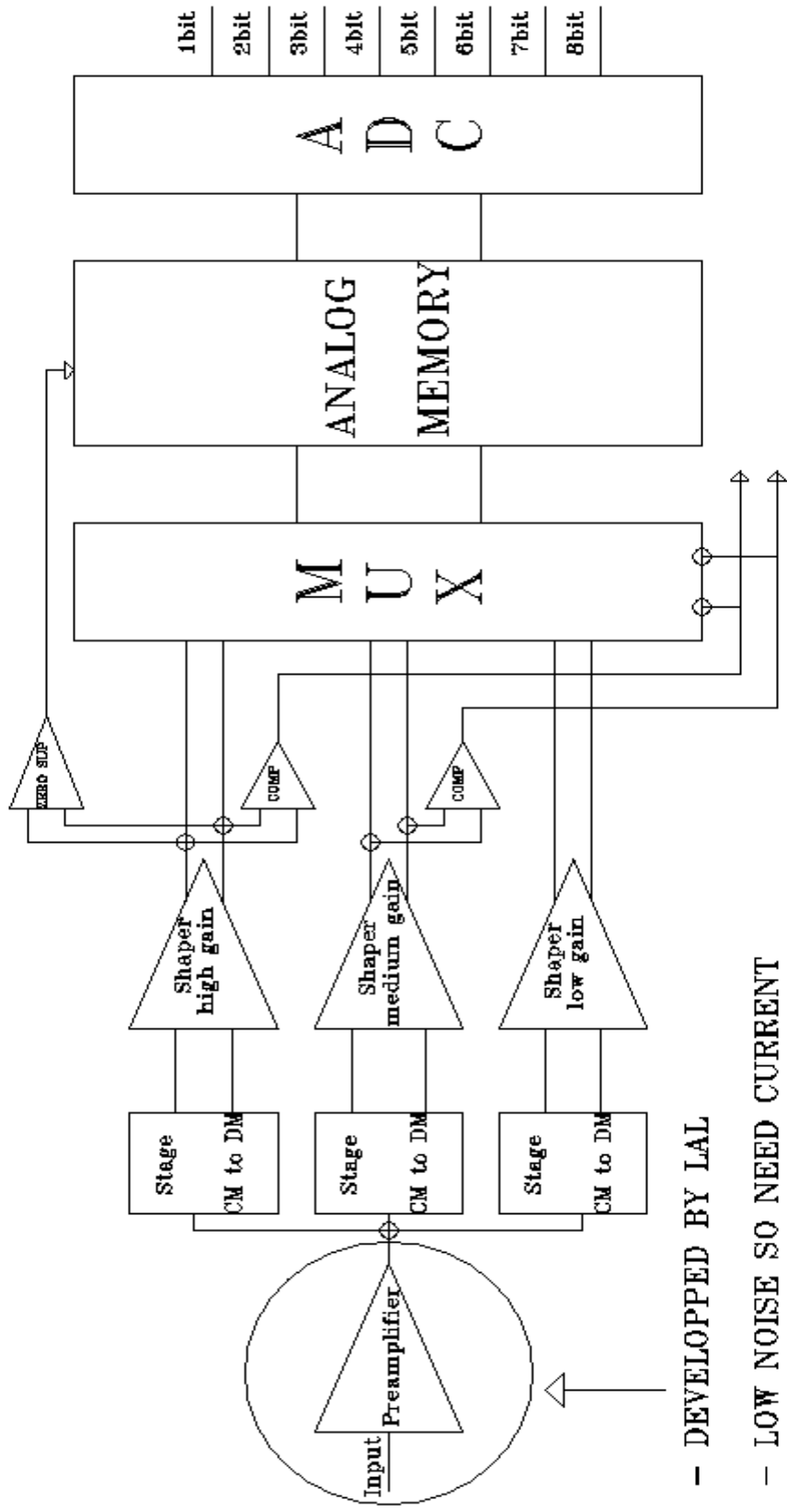
**– Shaper multi–gain,  $V_{out}$ = energy.**

**– Energy value only one measure.**

# A DESIGN FOR SIGNAL TREATMENT



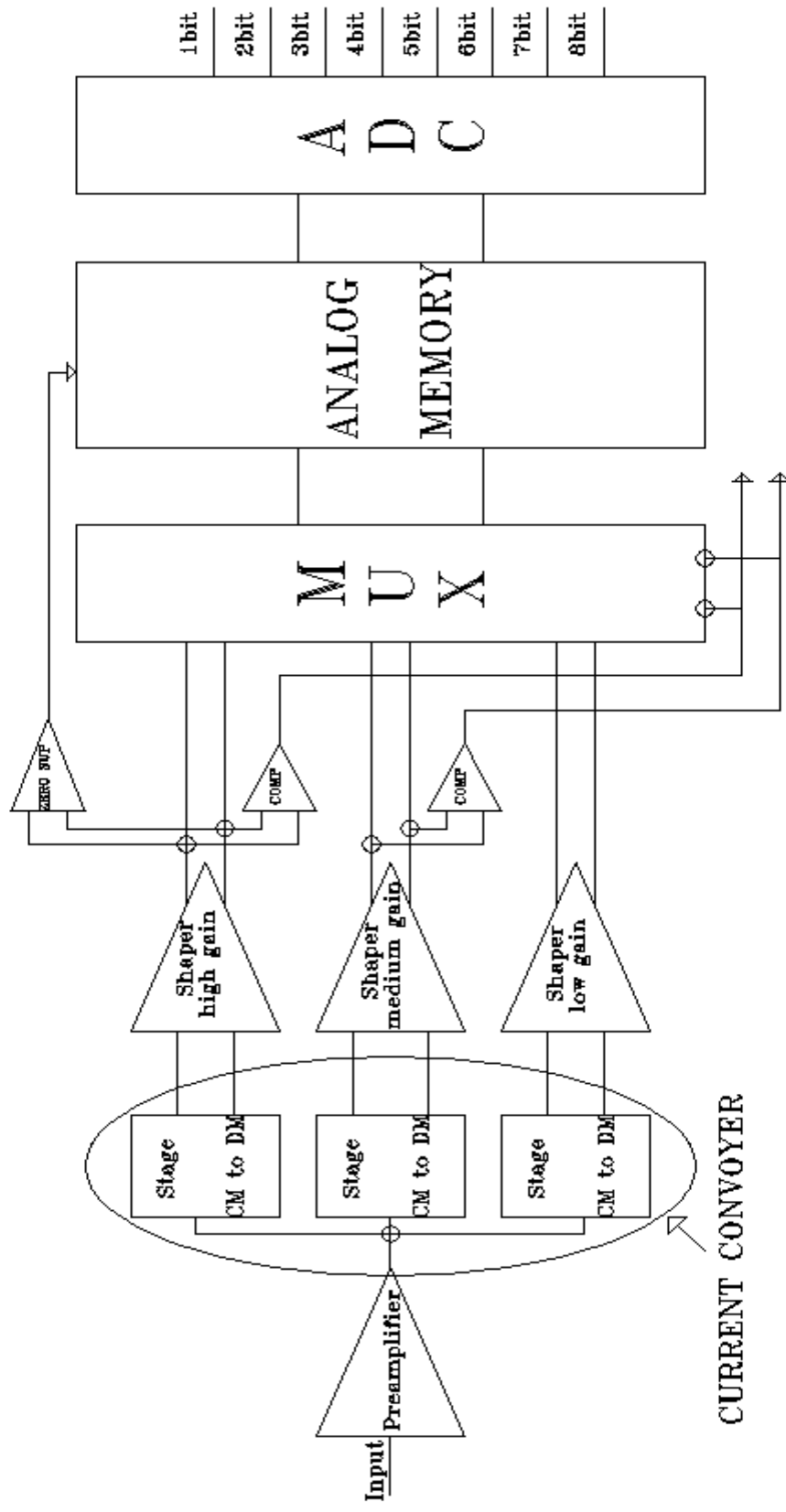
# A DESIGN FOR SIGNAL TREATMENT



- DEVELOPPED BY LAL

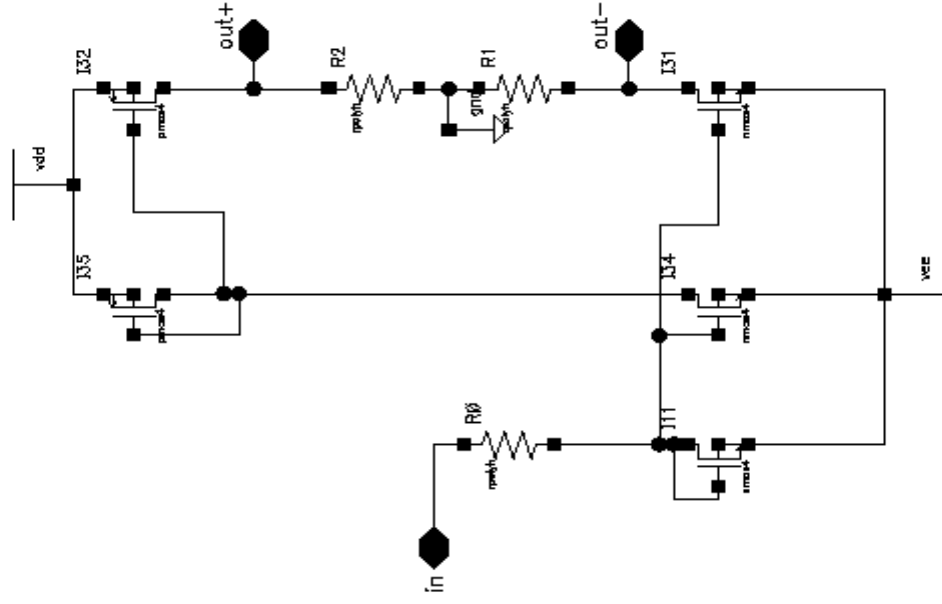
- LOW NOISE SO NEED CURRENT

# A DESIGN FOR SIGNAL TREATMENT





# CURRENT CONVOYER

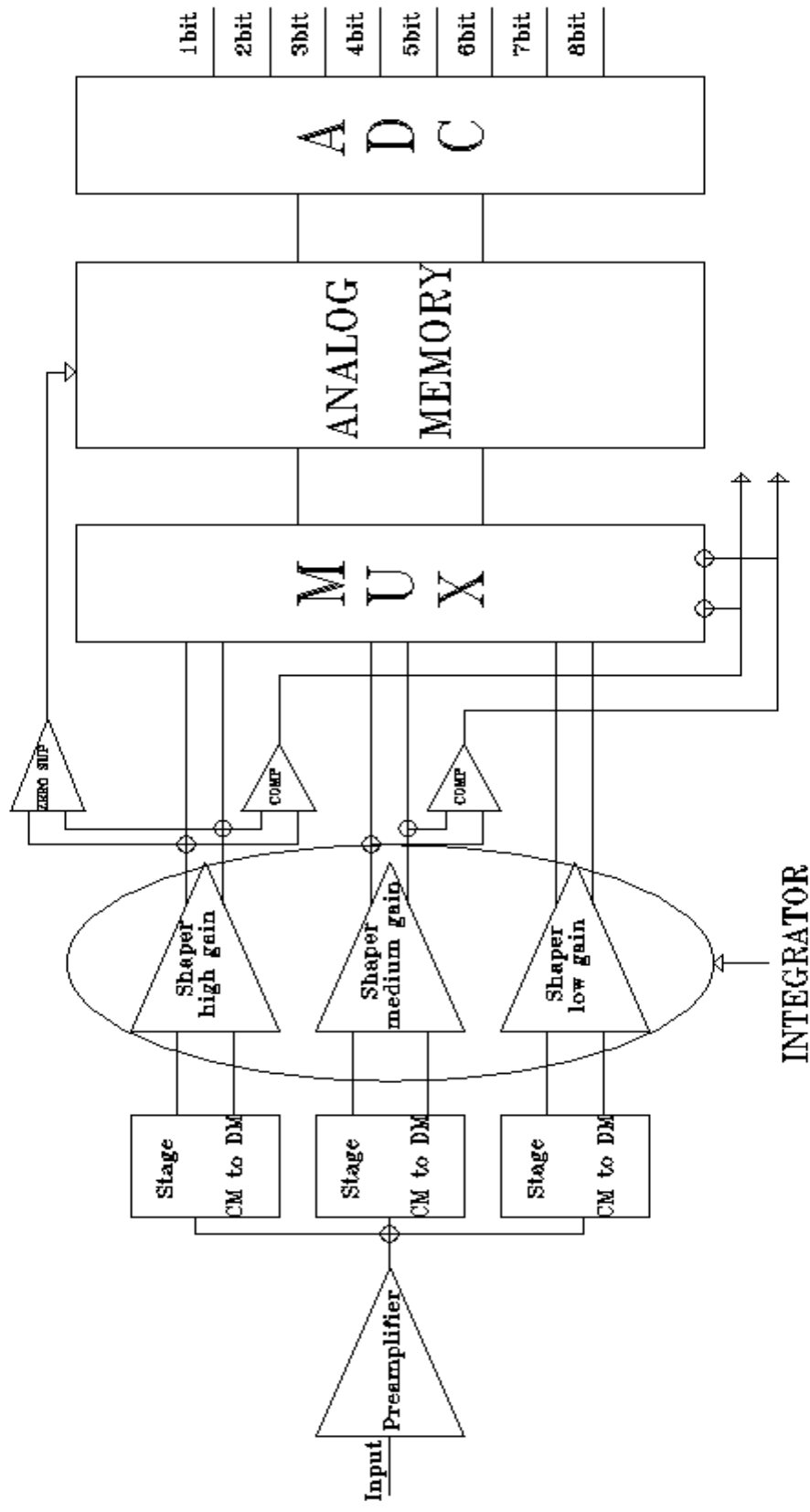


— COMMON MODE VOLTAGE INPUT

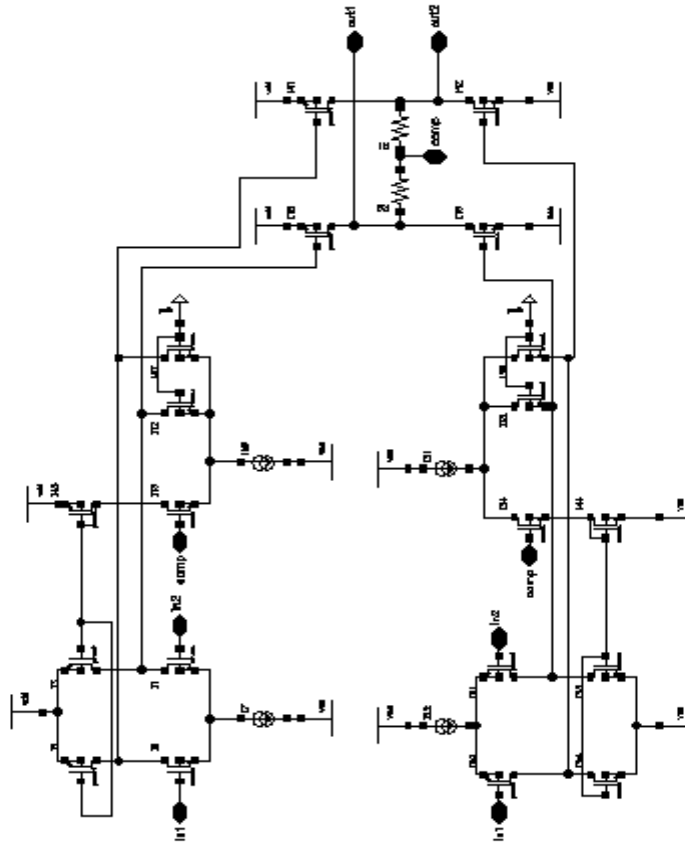
— DIFFERENTIAL MODE CURRENT OUTPUT

— TWO CURRENT MIRROR

# A DESIGN FOR SIGNAL TREATMENT



# AMPLIFIER



- LARGE DYNAMIC RANGE

- LOW POWER SUPPLY AND LOW CURRENT

- TWO DIFFERENTIAL PAIRS WITH ACTIVE LOAD

- COMMON MODE FEEDBACK

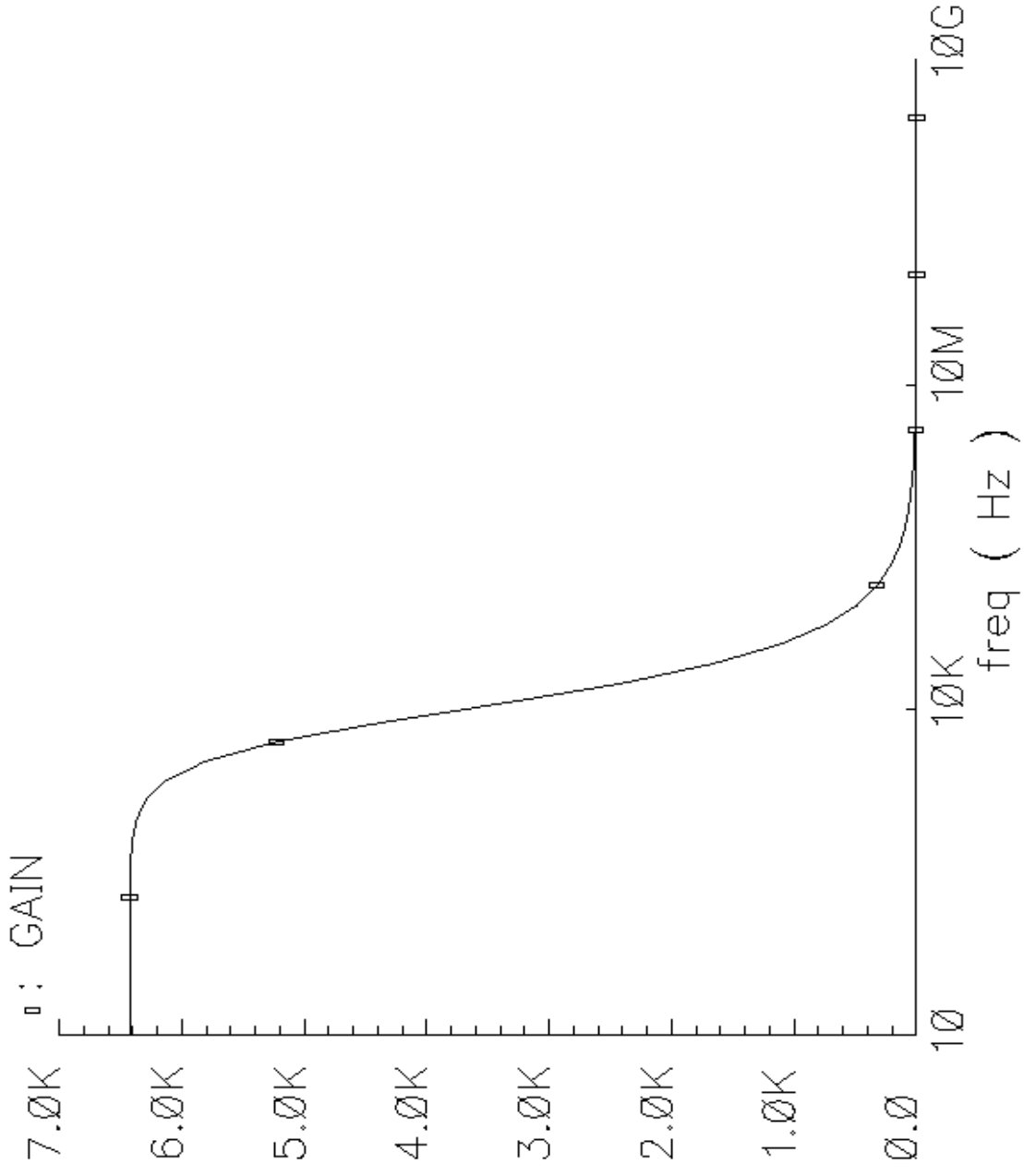
- OUTPUT RAIL TO RAIL

- CONSUMPTION : 250uA

# OPEN LOOP GAIN AMPLIFIER

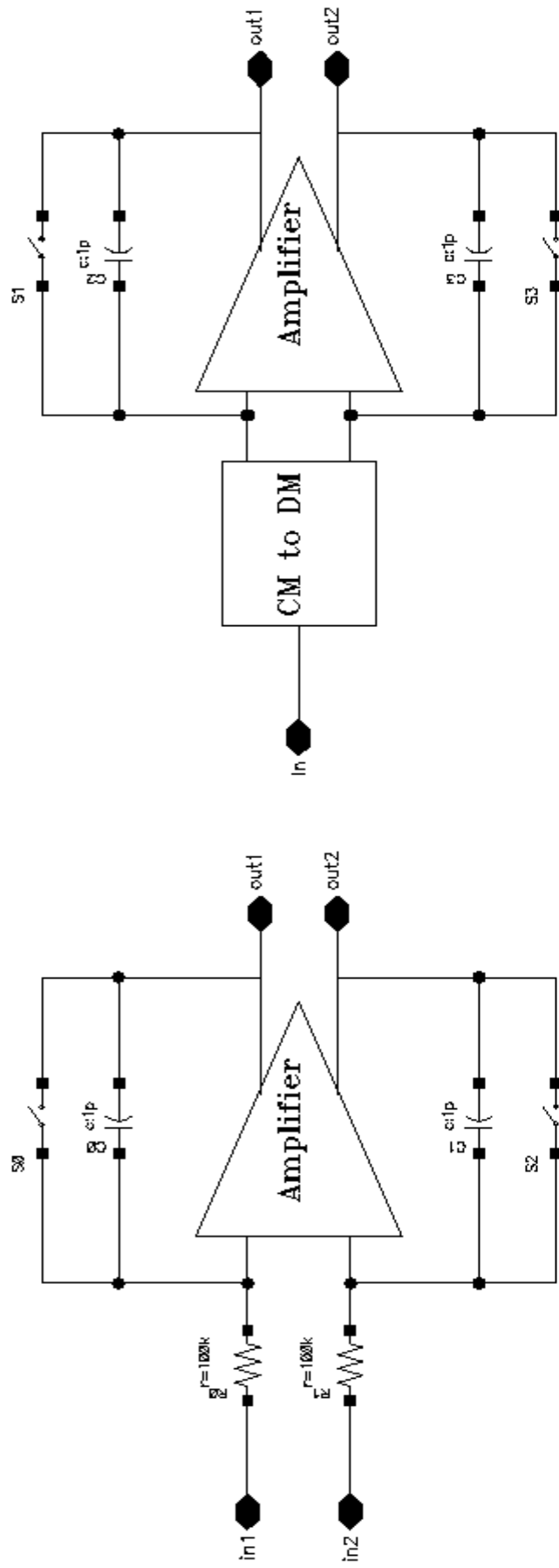
Simulation results with spectre Cadence

1



( 2 )

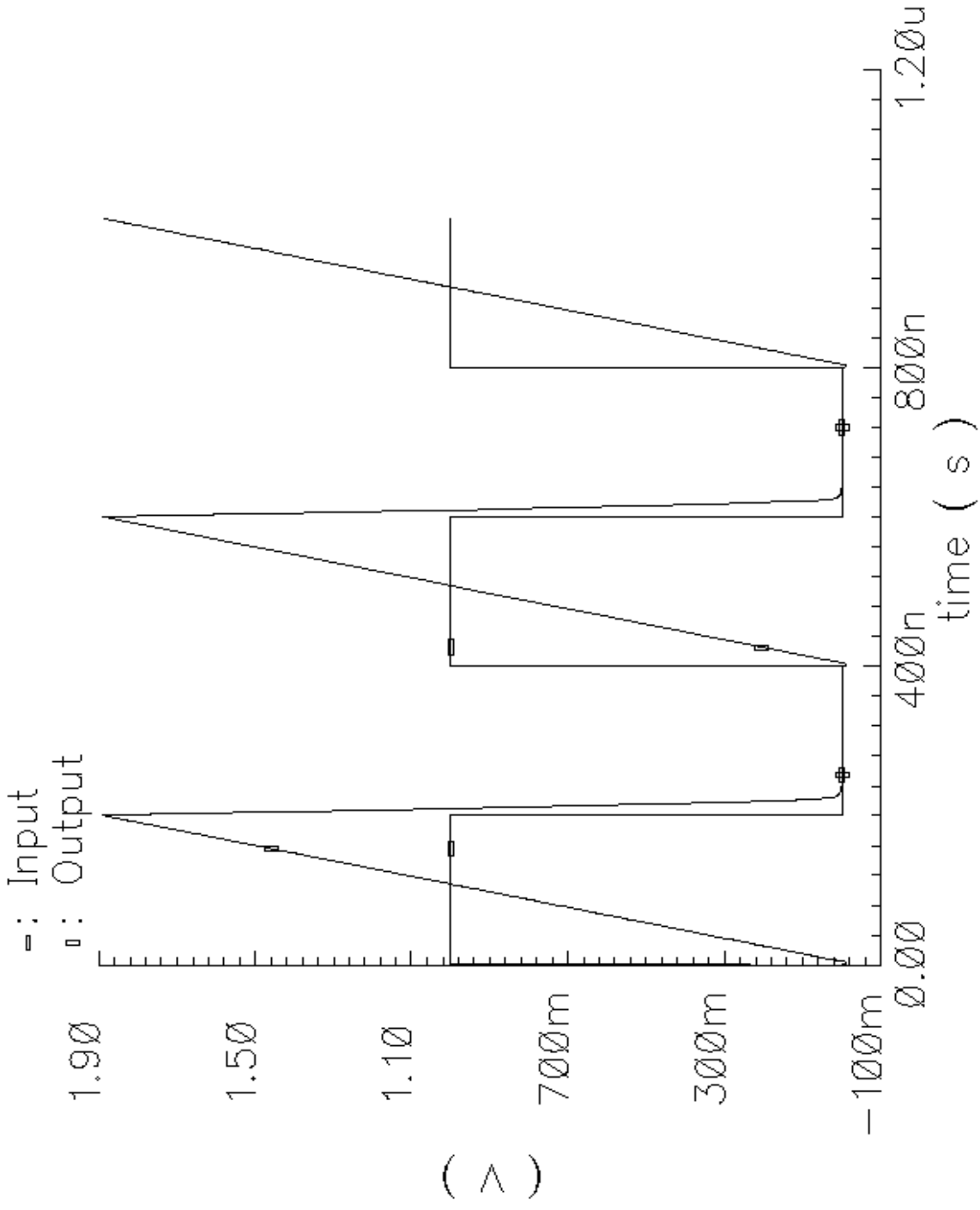
# CHIP SEND 08/02/2002



# SWITCHED INTEGRATOR

RESET TIME 20ns

1



# V-CODING

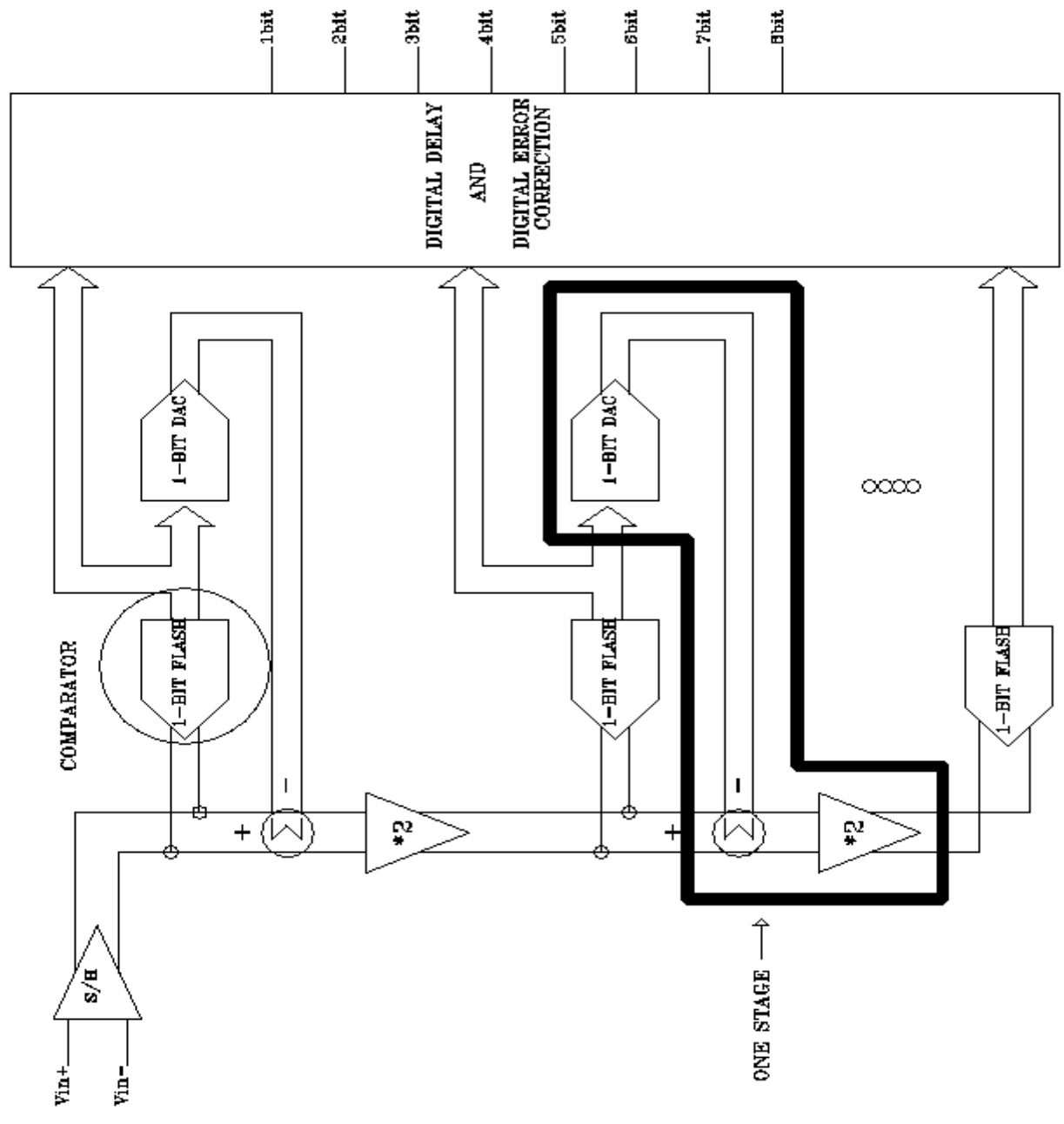
**Zero suppress with shaper high gain to have the better accuracy.**

**Channel identity (128 channels/chip).**

**Bunch crossing identity (3000 events).**

**Energy: analog memory (1 ADC for x channels).**

# ADC BLOCK DIAGRAM





## ANALOG TO DIGITAL CONVERSION

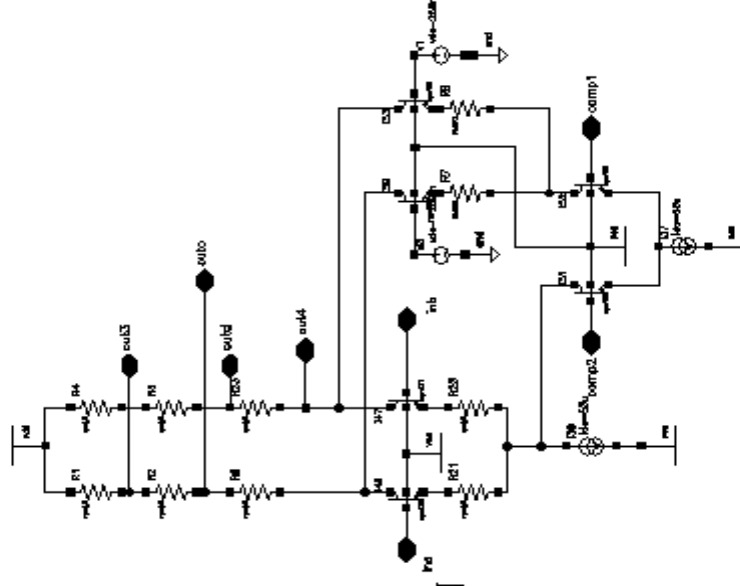
- PRINCIPLE: if  $V_{in} > V_{ref} \Rightarrow 1$   
then  $(V_{in} - V_{ref}) * 2 = V1$
- if  $V_{in} < V_{ref} \Rightarrow 0$   
then  $V_{in} * 2 = V2$

- ADC 1 BIT: COMPARATOR BIPOLAR OR CMOS

- ONE STAGE TO DO SUBTRACTION AND MULTIPLICATION

- MULTIPLICATION BY 2: AMPLIFIER GAIN 2

- SUBTRACTION COMMANDED BY COMPARISON BEFORE



# **CONCLUSION**

**Choice for technology : Cmos, SiGe...  
For the moment AMS 0.8 $\mu$ m BiCMOS.**

**Test amplifier verify good results.**

**Stage common mode to differential mode  
improve linearity.**

**Consumption ADC : bipolar or cmos ....**

**Multiplexer, analog memory....**

# LAYOUT 02/2002

