EUSO analog front end electronics

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For the EUSO Collaboration

Abstract

The design of the EUSO (Extreme Universe Space Observatory) Analog Front End Electronics (AFEE) is aimed at the detection of the bright, fast Cerenkov pulses and the extension of the dynamics towards very high energies (10^{21} eV). AFEE will allow in flight calibration. Dedicated ASICs have been designed with 0.35 μ CMOS technology. Performances expected from simulations and results of measurements with first ASIC prototypes will be presented.

1. Introduction

The EUSO telescope will detect the streak of fluorescence light and the spot of beamed or diffusely reflected Cerenkov light produced when Ultra High Energy Cosmic Rays interact with the Earth's atmosphere. EUSO will survey an area of 150.000 km2 and will have the potentiality to search for the very rare cosmic ray events with energy around and above the GZK edge. The signal generated by an Ultra Hight Energy Cosmic Rays is a bunch of fluorescence and Cerenkov light. The fluorescence light will last a few to few hundred microseconds and will arrive in most cases sequentially to the EUSO telescope. The main part of the Cerenkov light will arrive within a narrow time window of few tenth to few hundred nanoseconds.

The mean number of photoelectrons expected depends on the energy, the altitude and the direction of the shower and is typically a few to a hundred photoelectrons per microsecond. The instantaneous counting rate can be much higher for Cerenkov light and can be further increased when there is reflection from clouds with a large albedo. The single photon counting technique may still being operative for triggering but will have severe linearity problems because the counting efficiency depends on the photon rate. The measurement of intense photon flux is provided by integrating the induced electric charges of MAPMTs using analog electronics.

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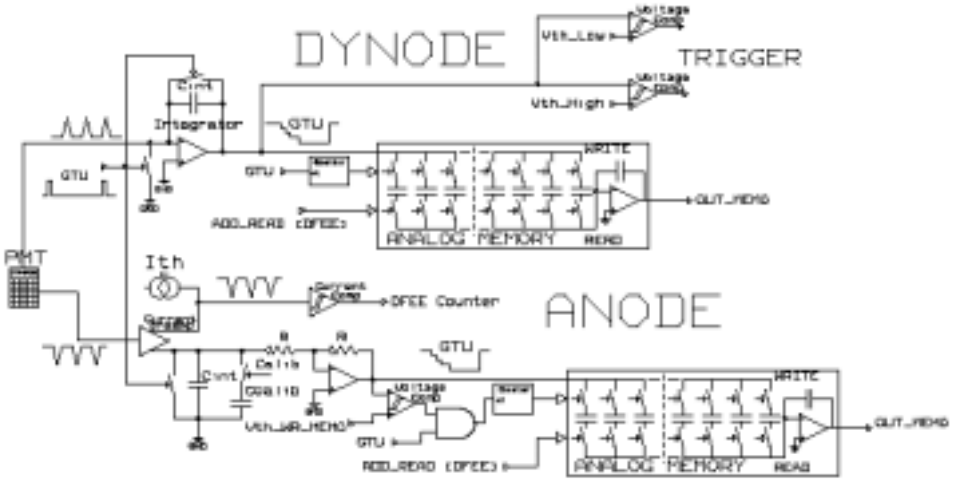

Fig. 1. Analog Front End Electronics block diagram

2. Options of AFEE

Both analog and digital front end electronics (DFEE) must be accommodated on the same ASIC. From considerations of power consumptions and feasibility, different approaches are under investigations: a simplified version with one analog channel per dynode sum, a full AFEE option with one analog channel per pixel plus one channel per dynode sum. If channel plates are selected as photon detectors, the common dynode will sum up 256 pixels and will not provide the appropriate analog signal. An intermediate option with one single analog channel for few (4-8) pixels could be considered if the full version is not compatible with the power budget.

3. AFEE Block diagram and functions

The AFEE block diagram is shown in Figure 1.

The specifications has been described [1]. The AFEE functions are mainly the following:

- Preamplify the photon detector signal: current pre-amplifier, with two independent current mirrors will be feeding both DFEE and AFEE channel analog integrator

- Discriminate anode and dynode signals with a programmable threshold and provide specific triggers: the signal from the MAPMT last dynode is integrated using a switched capacitor amplifier and is compared with two different thresholds. Specific triggers are delivered when high light yield signals are detected in a MAPMT.

-Integrate the currents from each anode and last dynode signals to provide correct numbers of collected photons within a GTU (Gate Time Unit)

- Store in internal analog memories the charge corresponding to each GTU (32 per anode pixels, 256 per dynode sums)

- Digitize signals with external ADC'S.

4. Cascoded outputs and auto-zero correction

The main feature of the analog front end circuit is that it has low input impedance, with high speed and small power consumption. To reduce output residual currents, two more sophisticated designs have been considered:

a) Current amplifier with cascoded outputs.

One of the crucial points of the charge integration during one GTU is the impedance of the output stage. Due to a finite output impedance, the leakage current can change with output voltage level. To increase the output impedance, a preamplifier with cascode composite transistors has been designed. The basic idea is to have two transistors in serial; one is connected to the variable point, the other is kept at a constant voltage value. This architecture increases the output impedance by a factor of about 20. The drawback is a small reduction of the dynamic range and of the speed.

b)Current amplifier with 'auto-zero' correction.

In practical implementation of current mirror amplifiers, a random mismatch between the transistors will create a base line current offset at the out. The integration of such an offset ($1\mu A$) during a GTU will lead to an important dispersion in the analog signals, making the calibration task more and more critical. The aim of the auto-zero amplifier is to measure and compensate such an offset it. Thus the variation and the drift of the baseline would be reduced. The difficulty of the task is that this compensation could take place only during the very short window available between two successive GTU. The power dissipation should be very low, compared to the preamplifier.

5. Preliminary results with first ASIC prototypes

We have designed and tested two different prototypes. The first one includes a full dynode channel. The second one has 12 anode channels (with different structures of preamplifiers and comparators) and a full dynode channel. Preliminary results are the following: For the dynode channel (Figure 2.),the non linearity of the full dynode channel (integrator + analog memory) is better than 1% in the full dynamic range (up to 3500 pe-). The charge loss in one analog memory cell is not significant up to 9ms of storage duration. In the anode channel an "auto-zero" amplifier reduced the output leakage current of the current

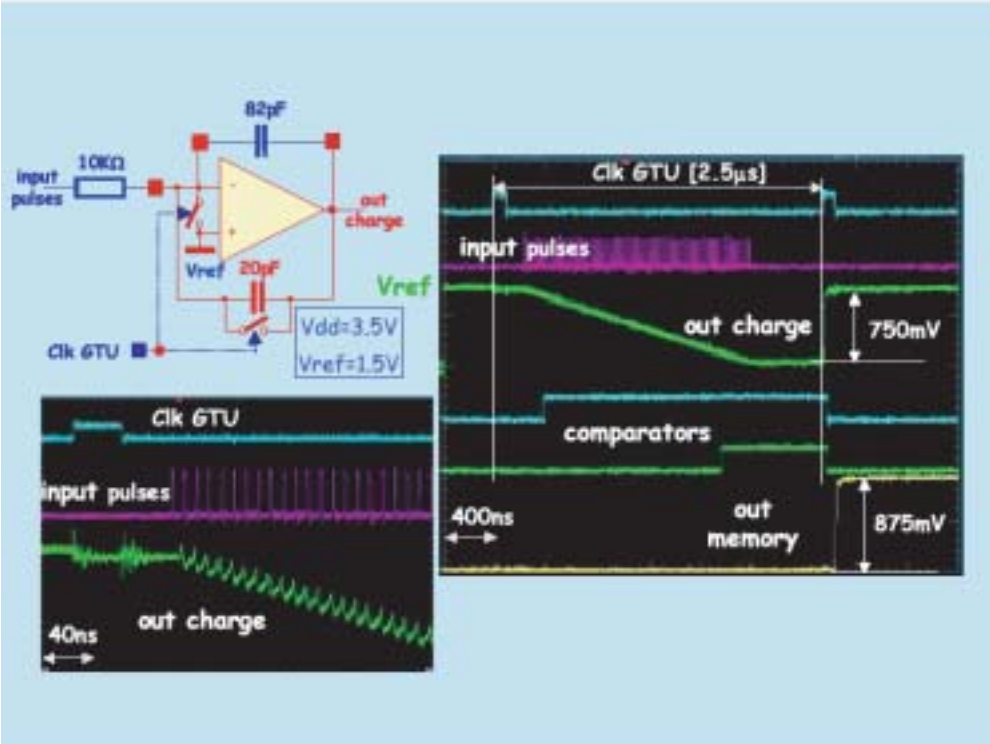

Fig. 2. Dynode channel

preamplifier by a factor of 10. The linearity of the preamplifier integrated output is better than 3% in the full dynamic range (up to 400 pe).

6. Conclusions

The prototypes have been processed in CMOS 0,35 μ technology. The future Prototypes will be designed in BiCMOS technology which is a better candidate for space qualification.

7. References

1. Pouxe J. et al. Analog Front End Specification and Design EUSO-AFEE-SP-001-1 May2002