Preshower very front end chips

G. Bohner, J. Lecoq, Pascal Perret

Preshower very front end chips
PRR
march 25^{th} 2 004

G. Bohner

L.P.C. Clermont-Ferrand

Université Blaise Pascal, 63177 AUBIERE Cedex

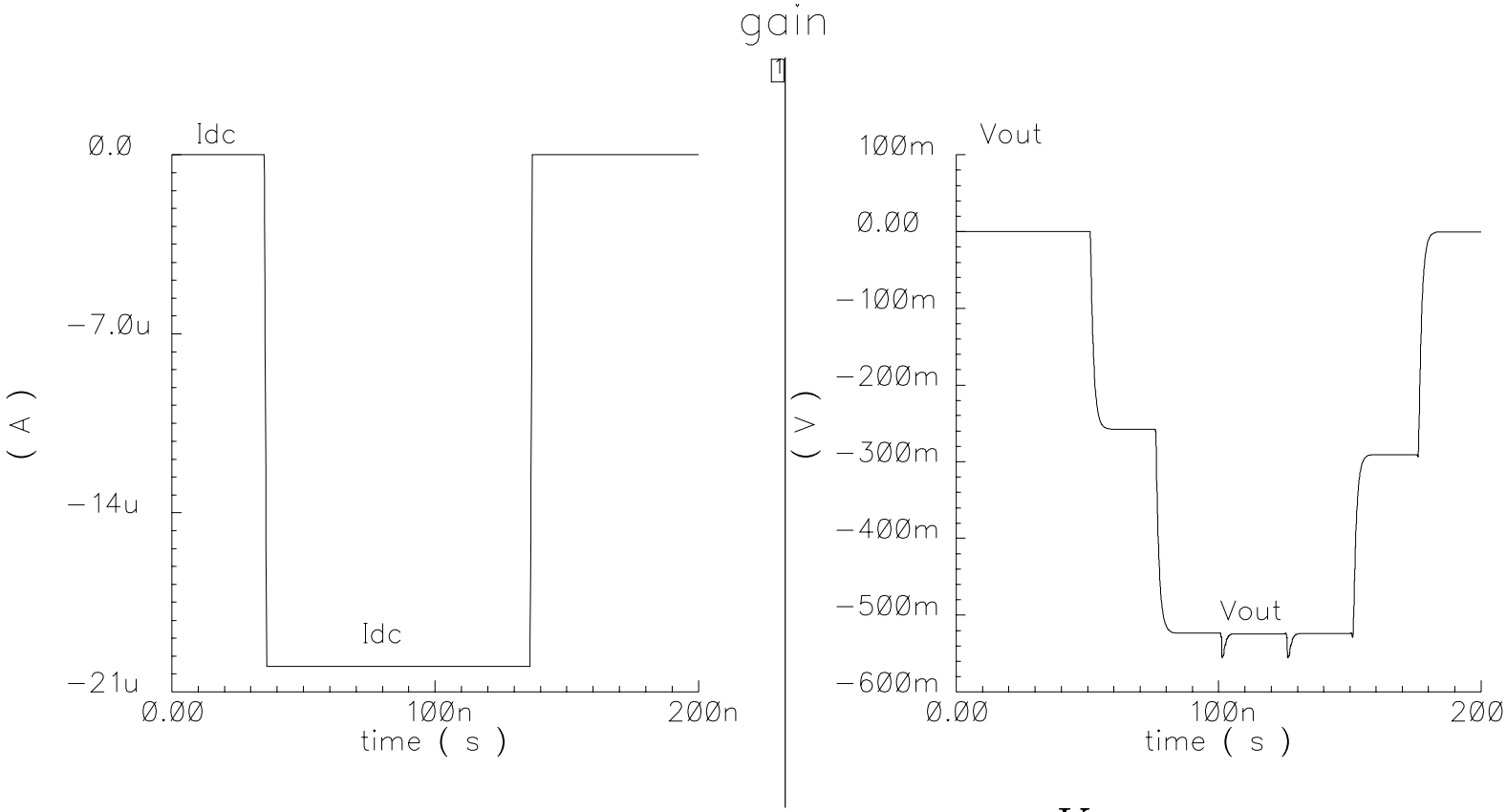
bohner@clermont.in2p3.fr

New VFE chip PRR

The first PRR of the VFE chip was done in 2001 November.

Since the gain has been multiplied by 10 and we had to find new solution for the noise and the offset. The first stage is completly new ; it is a current convoyer.

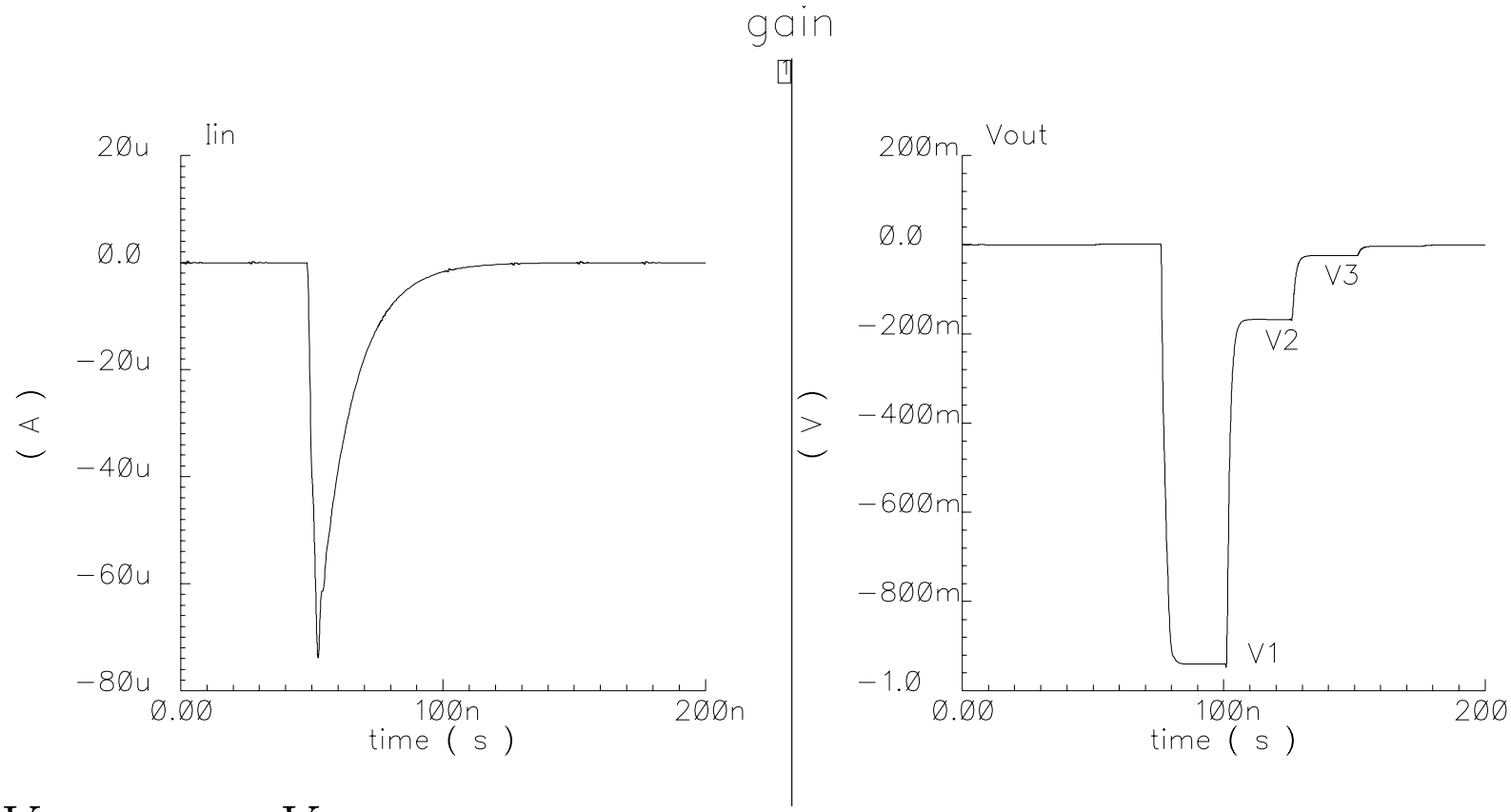
definitions :



Gain : V_{out} by I_{in} for a DC, 25 ns current, $\rho = \frac{V_{out}}{I_{dc}}$.

Or $\rho^{-1} = \frac{Q}{V}$ the ratio Q in 25 ns ($Q = I_{dc} \times 25.10^{-9}$) by output voltage, in Coulomb/Volt.

definitions 2 :



$$\alpha = \frac{V_2}{V_1},\ \alpha_2 = \frac{V_3}{V_1}$$

Three versions

All versions are 4 channels.

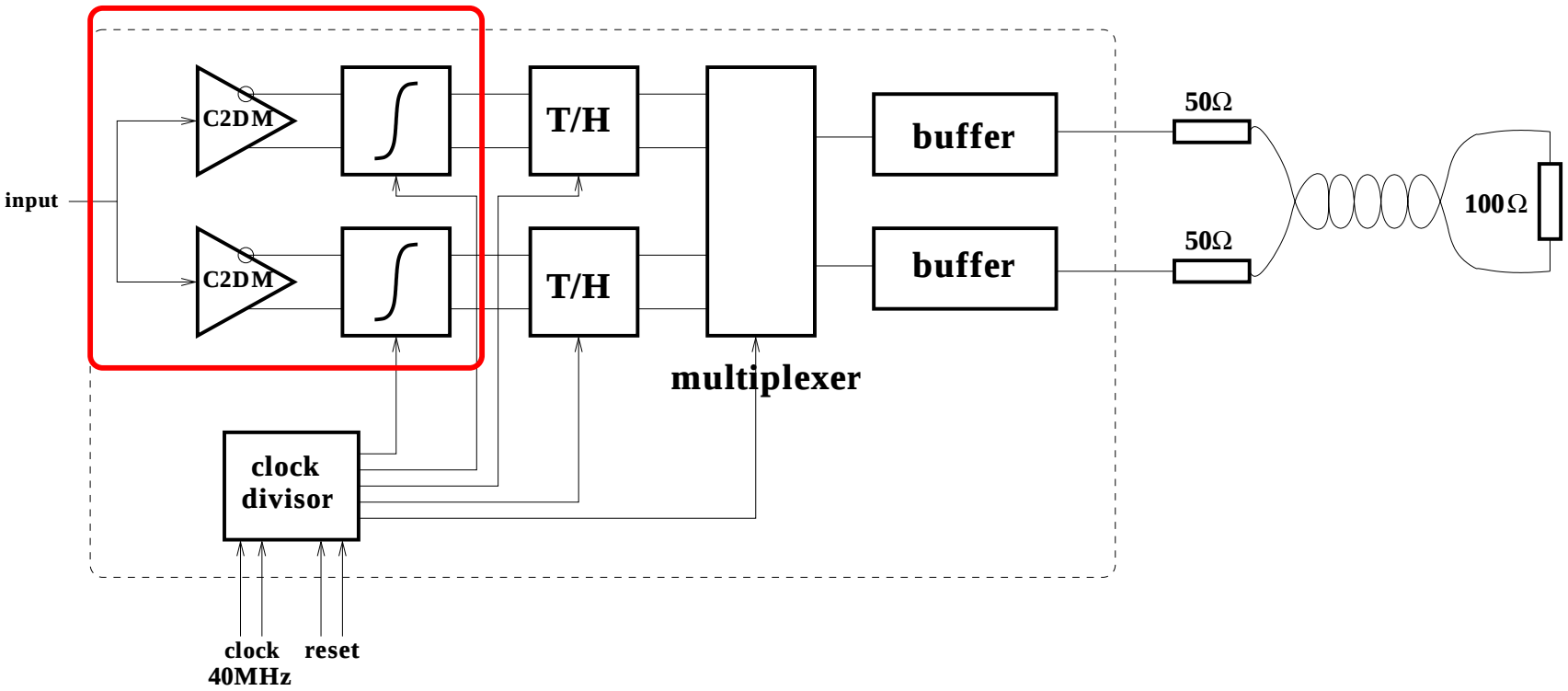
The technology is Austriamicrosystem BiCMOS $0.8\,\mu m$.

The first : gain is $\rho \simeq 26\,000\,\Omega$, it is necessary to tune the gain with external resitors and capacitors at VFE level to correct for MAPMT non uniformity (to decrease the gain). Prototype done and tested.

The second : gain $\rho \simeq 9\,000\,\Omega$, it is necessary to tune the gain with resistors at FE level (to increase the gain). No prototype.

The third : two gain values $\rho \simeq 26\,000\,\Omega$ and $\rho \simeq 13\,000\,\Omega$, selection by jumper. Another gain selection on the FE card (1 or 1.5), by jumper too. No prototype.

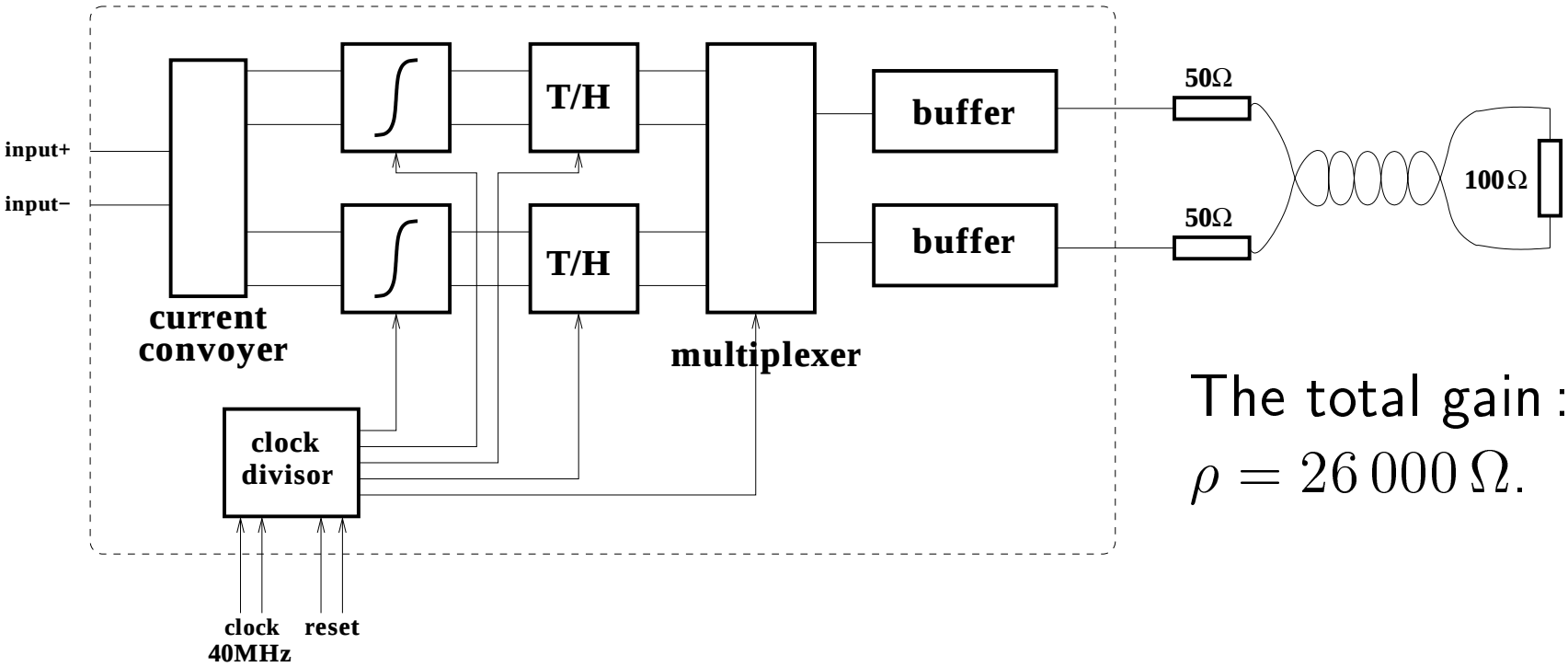
The 2001 version



The 2 001 gain : $\rho = V_{out}/i_{in} \simeq 2\,300\,\Omega.$

The first 2003 version.

Two half channels (no dead time). The first stage is a current convoyer, common mode current to differential mode current, with a gain 4.6 and two outputs, one for each integrator.

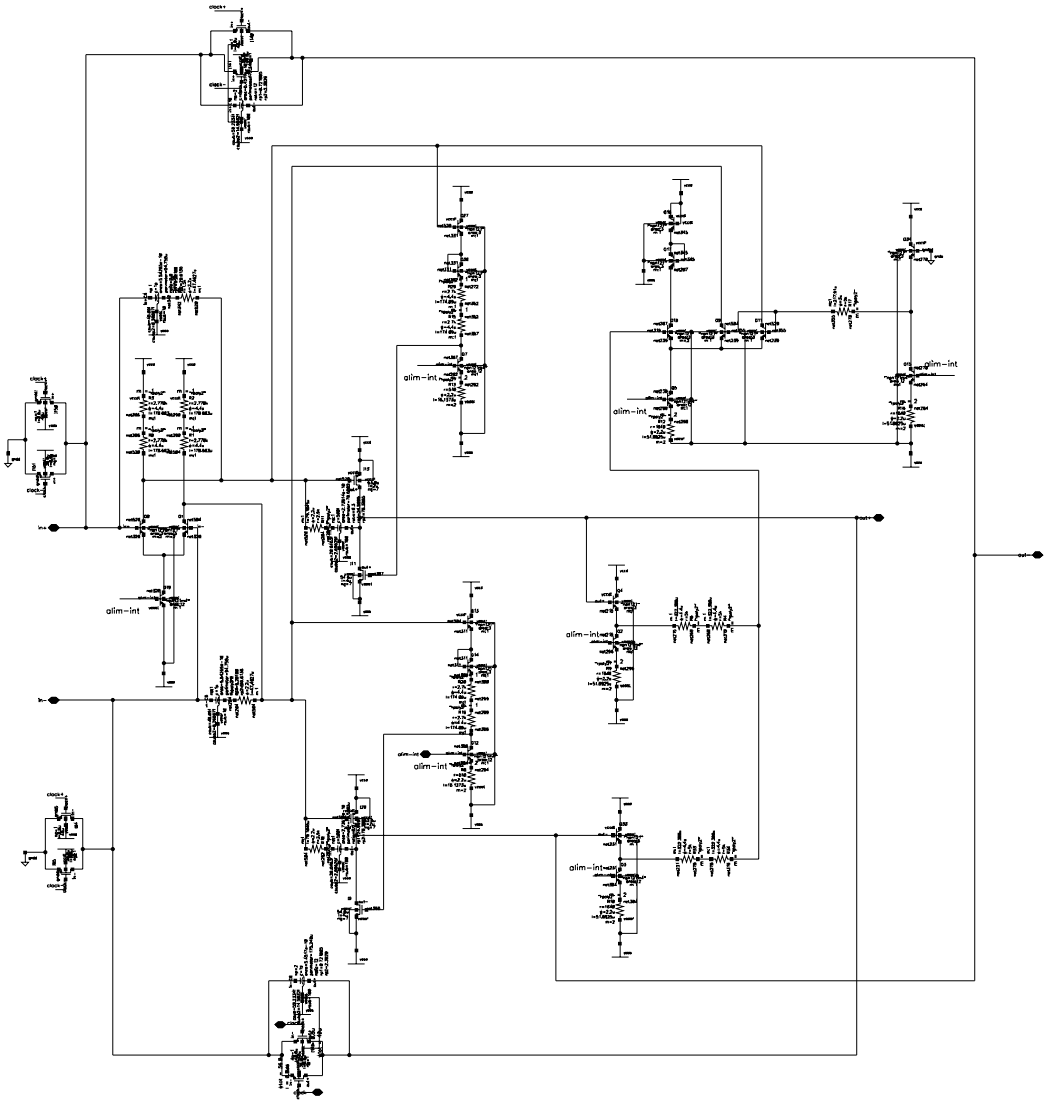


The total gain :
$\rho = 26\,000\,\Omega.$

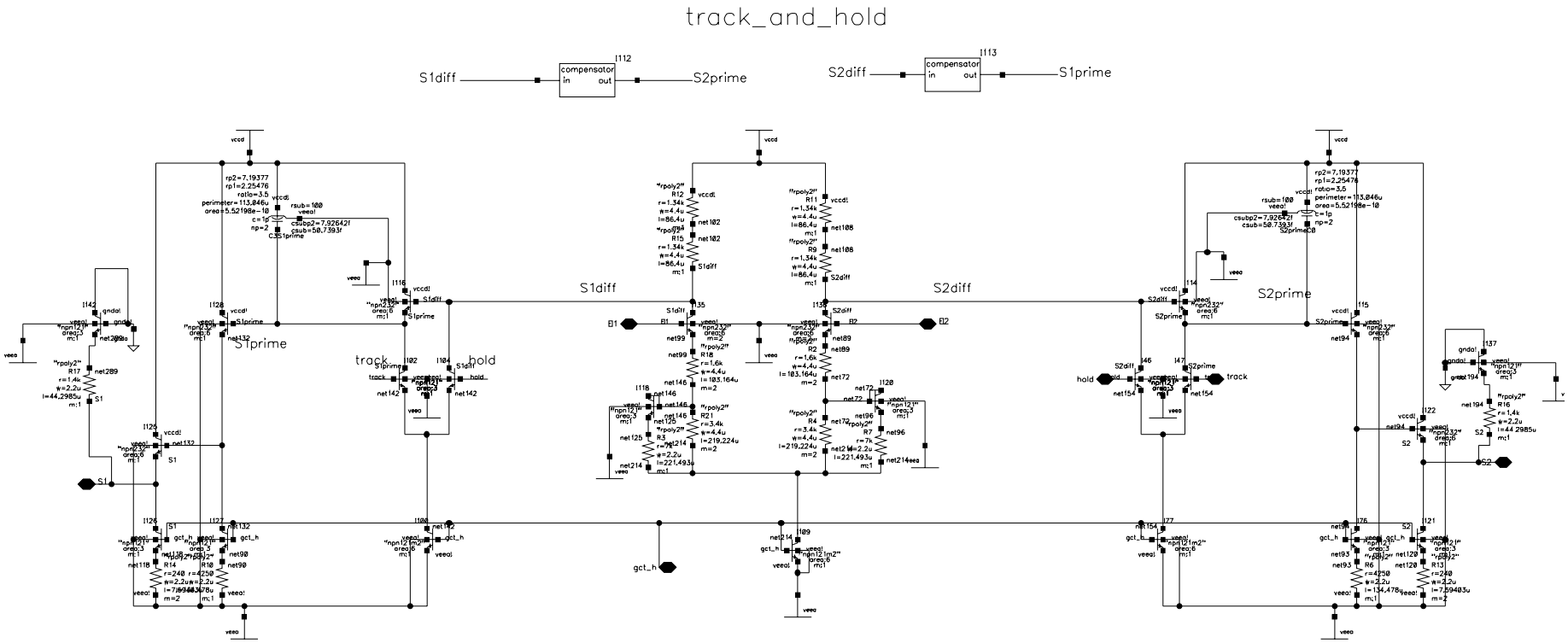
The first version : details.

Integrator, track and hold, multiplexer, buffer and clock divisor are the same as the 2001 version.

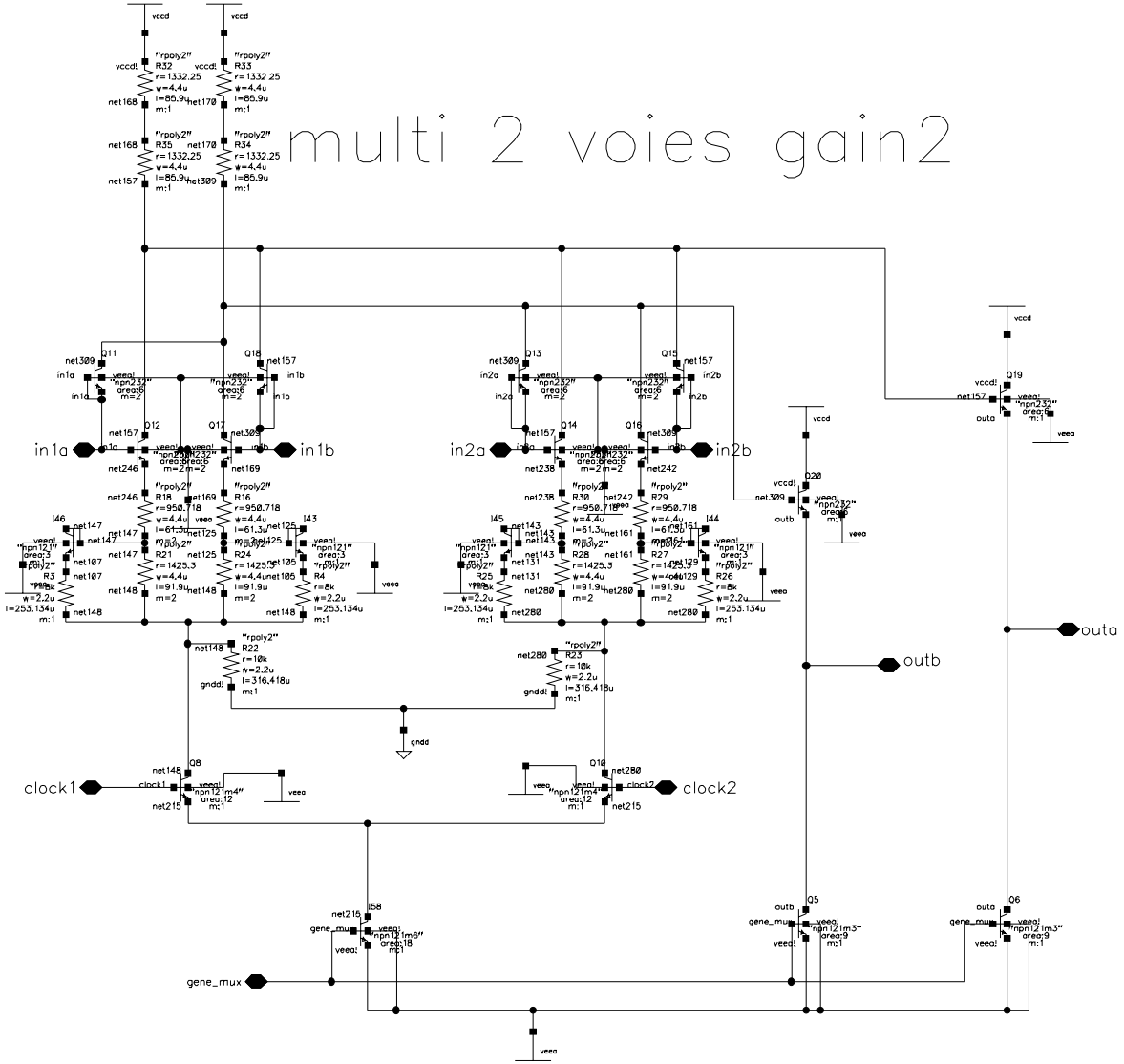
integrator (reminder)



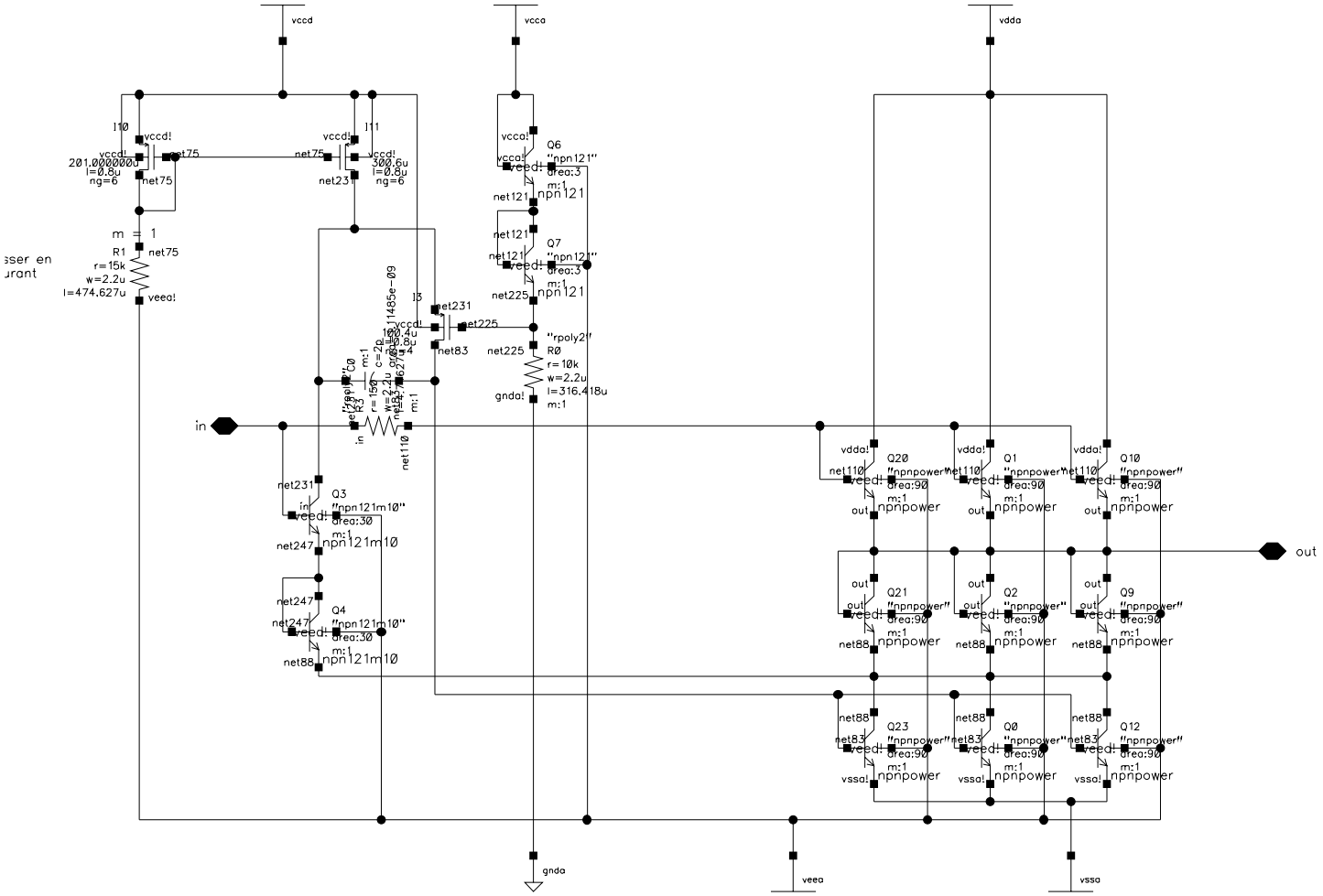
track and hold (reminder)



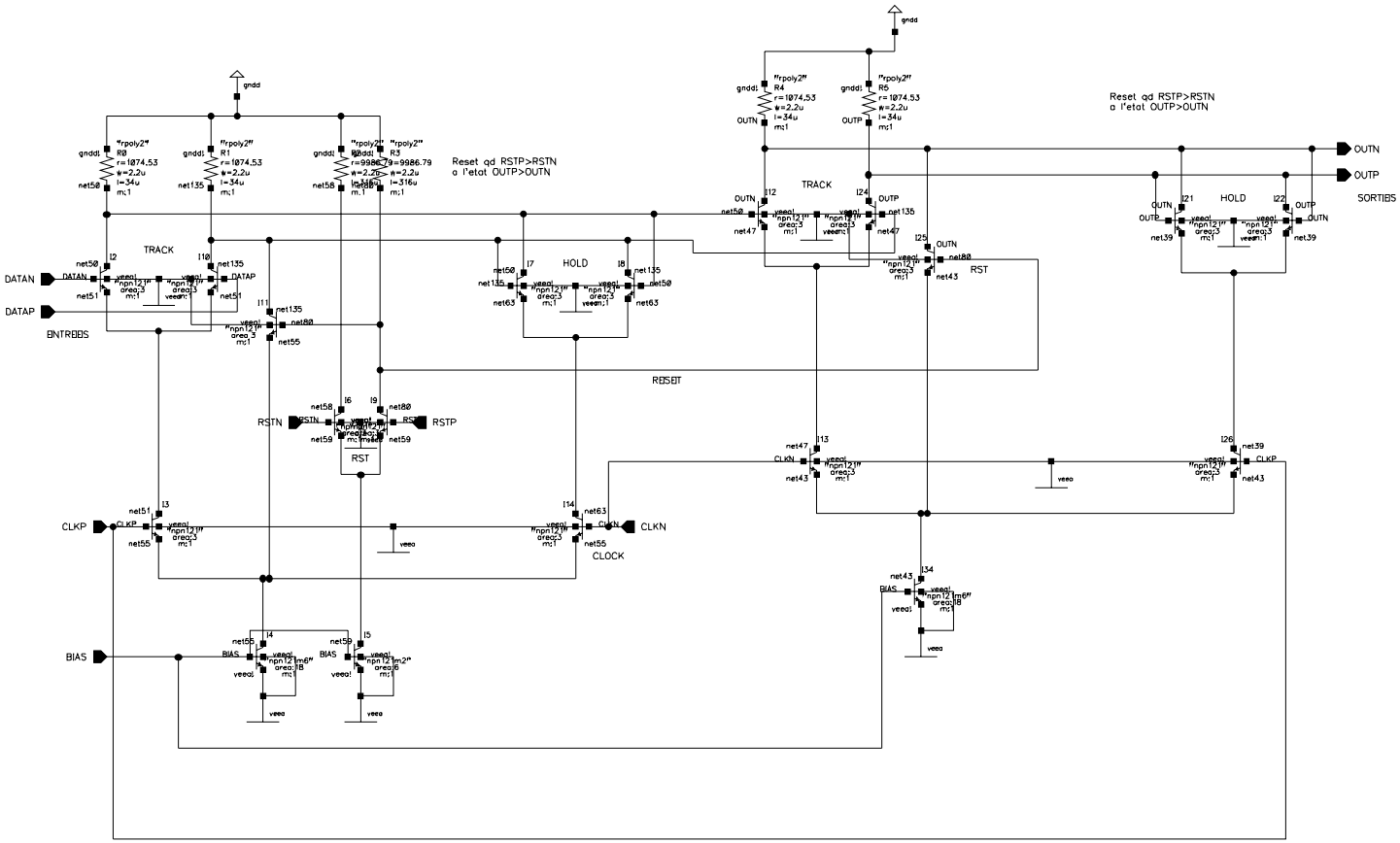
multiplexer (reminder)



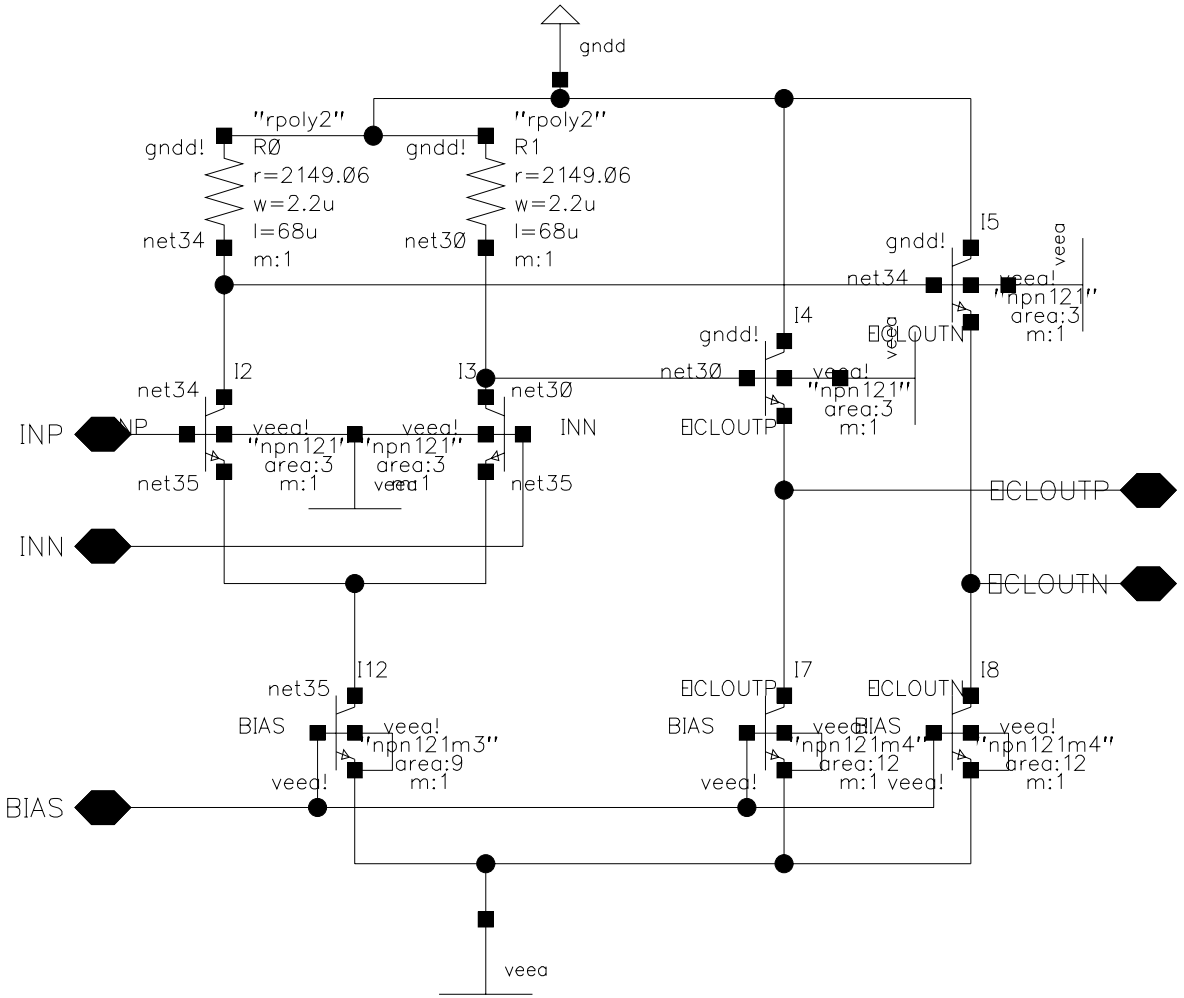
buffer (reminder)



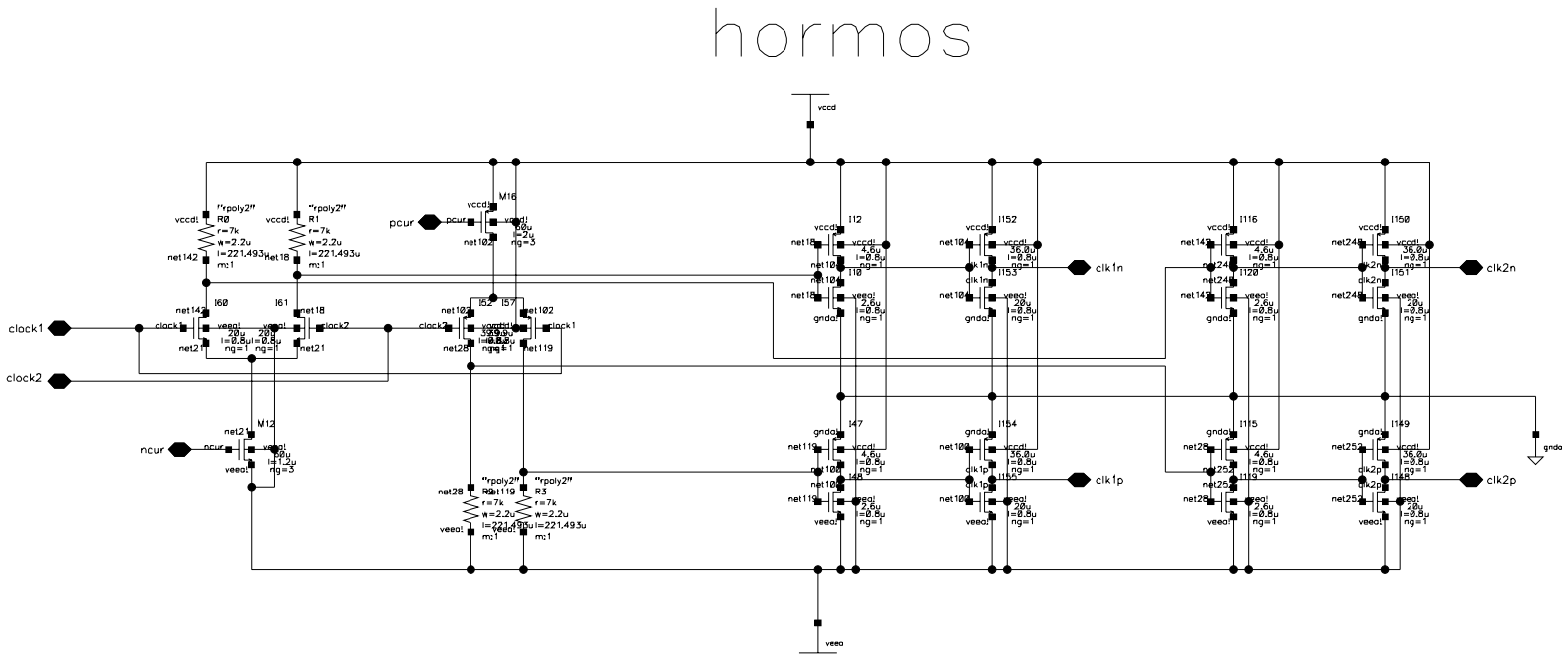
general clock input (reminder)



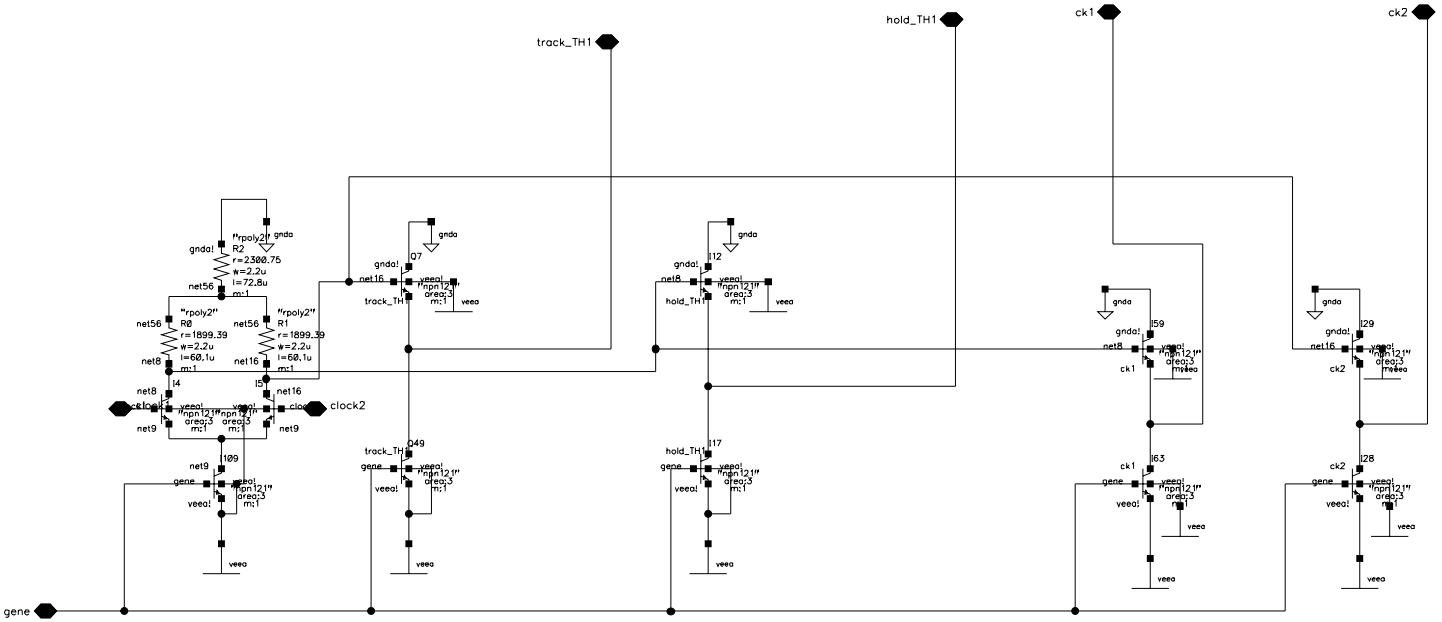
general clock output (reminder)



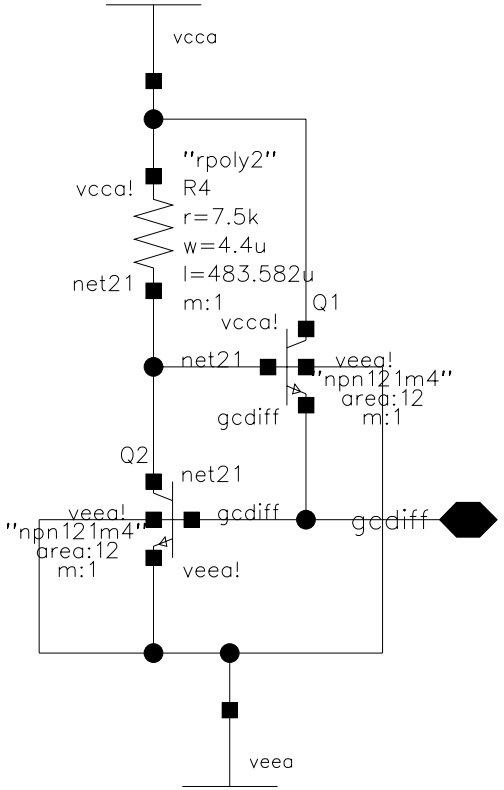
clock MOS for each intégrator (reminder)



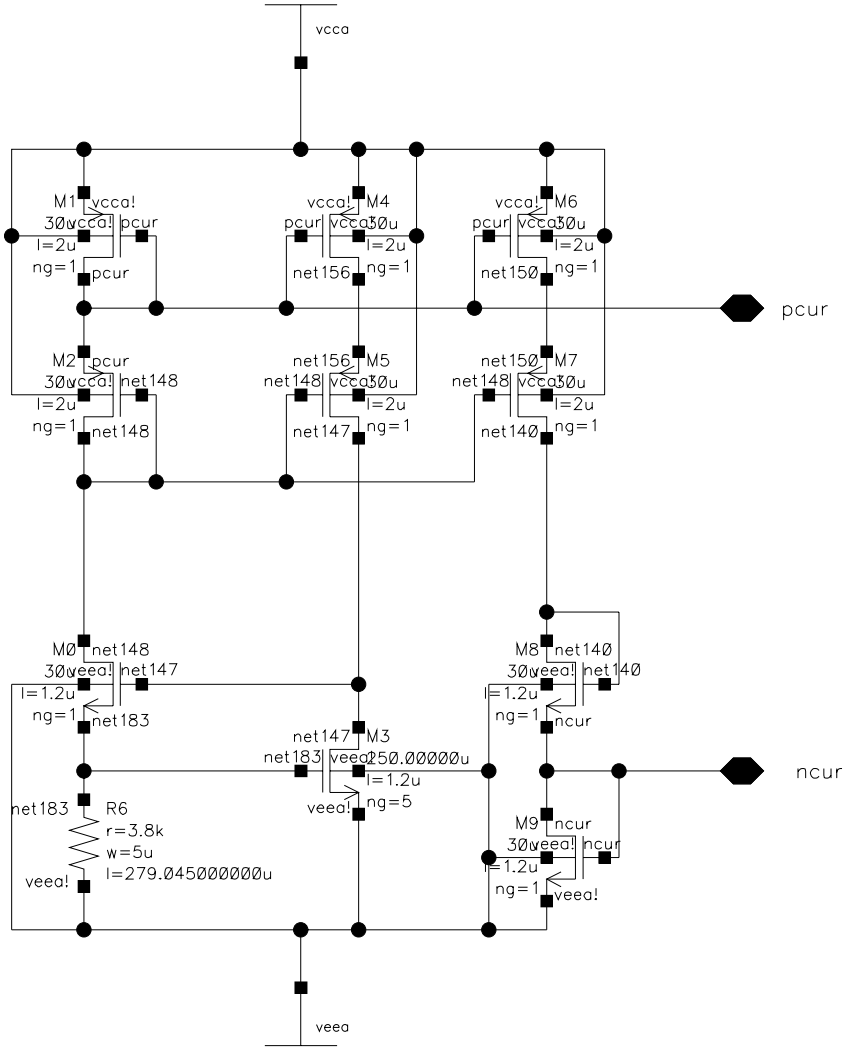
ECL clock for each channel (T&H, mux) (reminder)



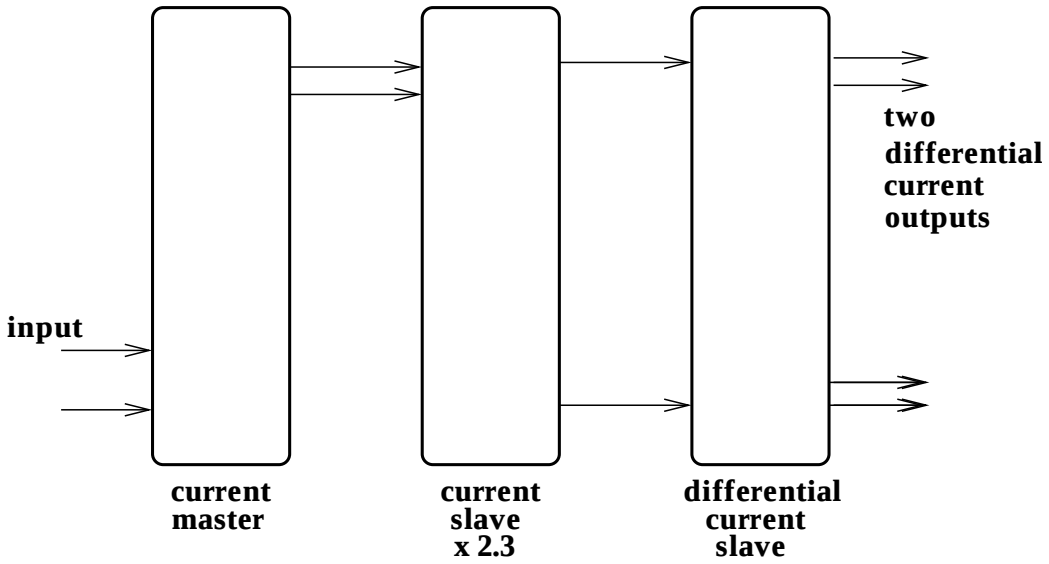
bipolar current generator : master (reminder)



MOS current generator : master (reminder)



The current convoyer.

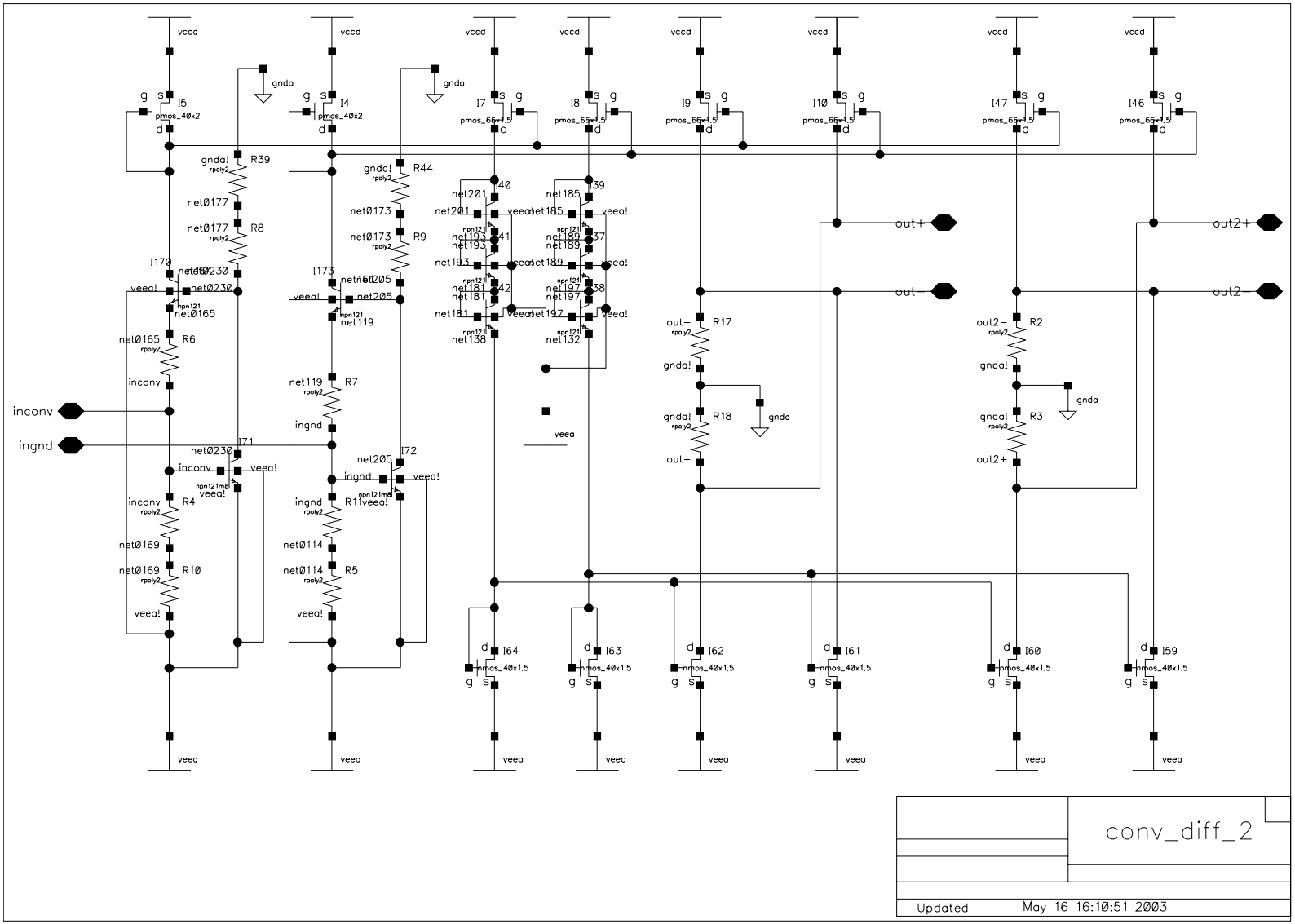


The current master measures the PM current and the polarization current.

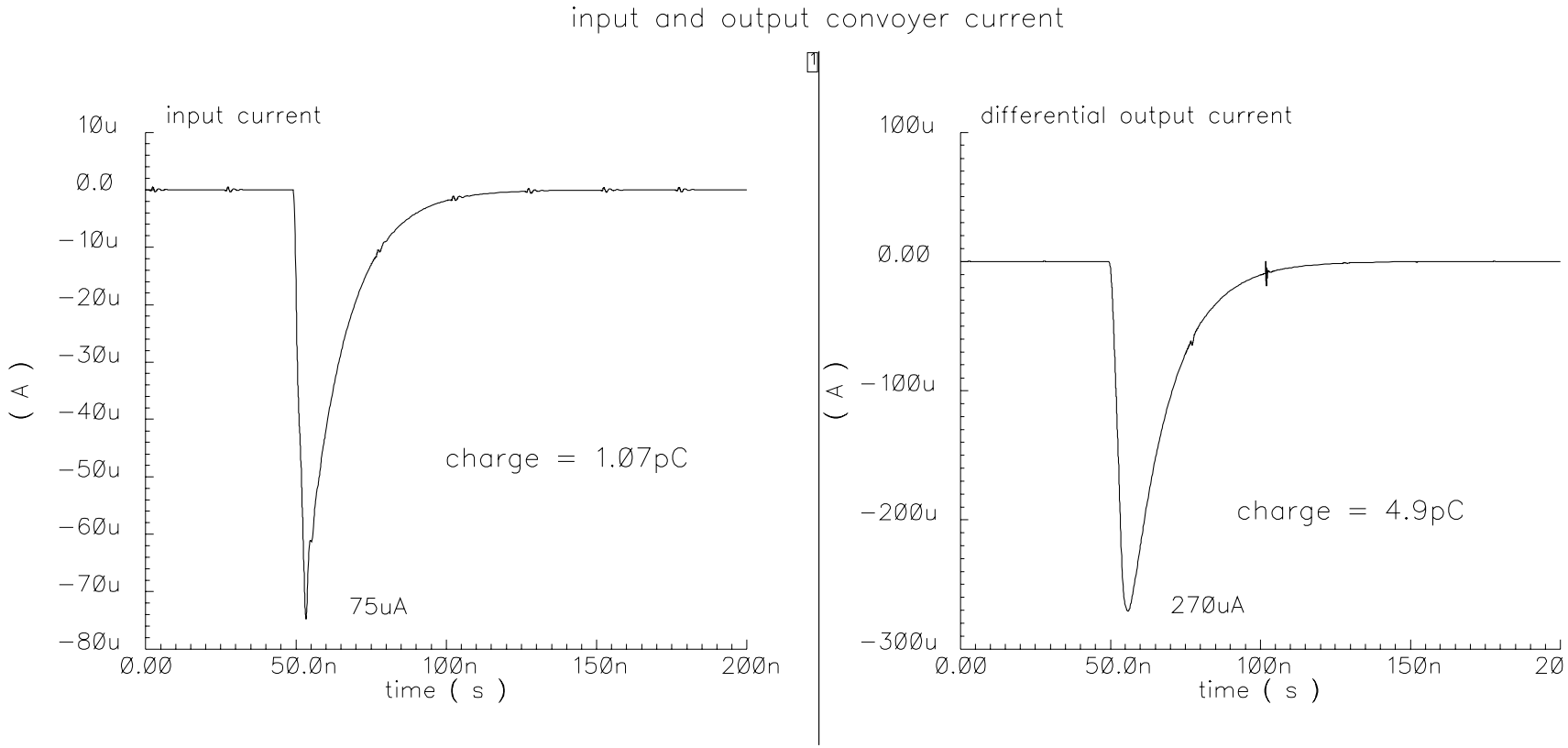
The first current slave multiplies the currents by 2.3.

There are two second current slaves, this makes differential currents. (The polarization current is substracted). The final gain is 4.6 (in charge).

Current convoyer schematic



Current convoyer gain : simulation results.

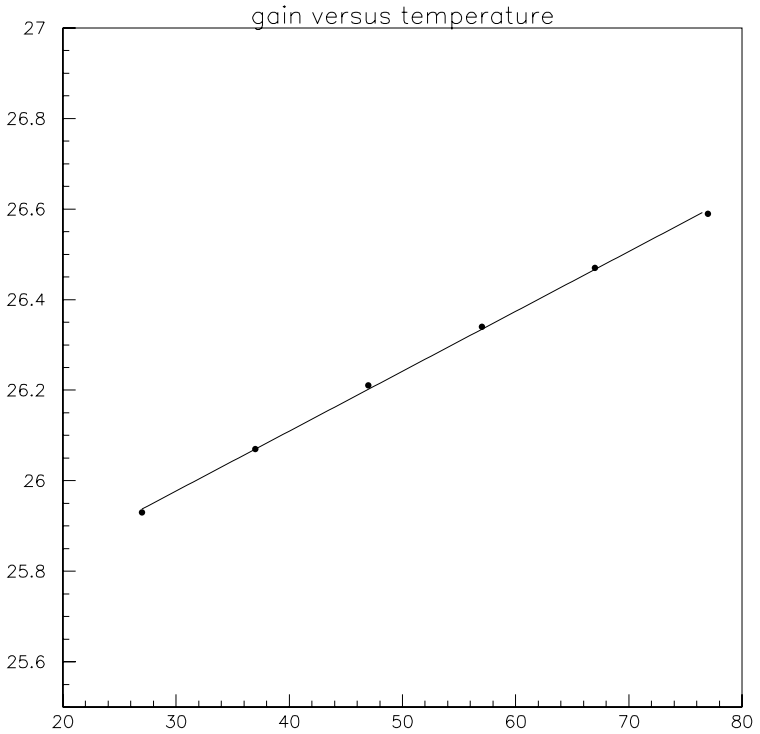


The convoyer gain is 4.6 (in charge).

gain versus temperature : simulation

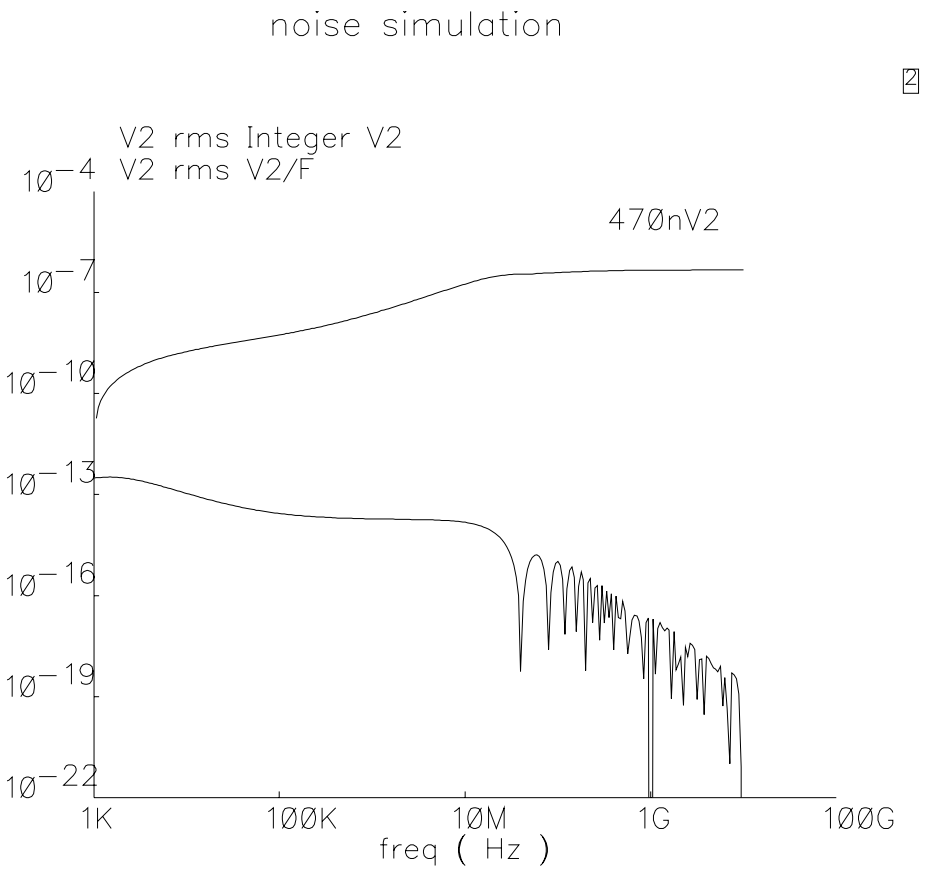
T in ^0C	gain in $k\Omega$	α
27	25.9	17.8%
37	26.1	17.8%
47	26.2	17.8%
57	26.3	17.8%
67	26.5	17.8%
77	26.6	17.8%

$\rho^{-1} = 960\, fC/V$



With the temperature, α is constant, the gain increases (0.05% per degree).

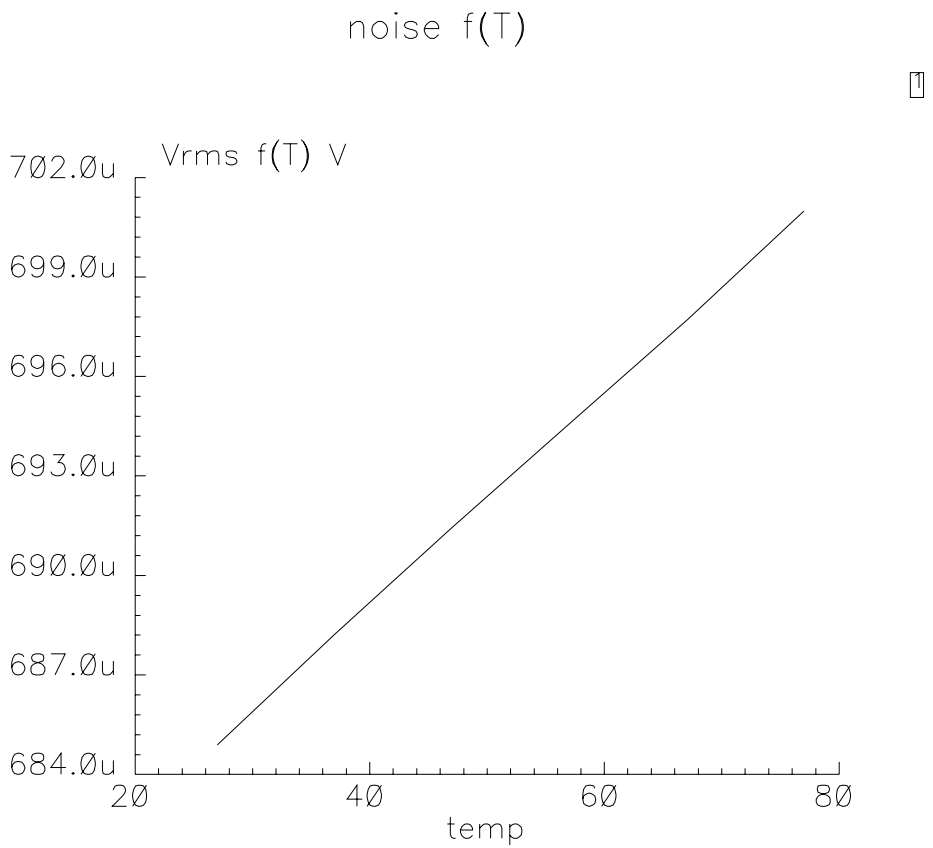
Channel noise : simulation results.



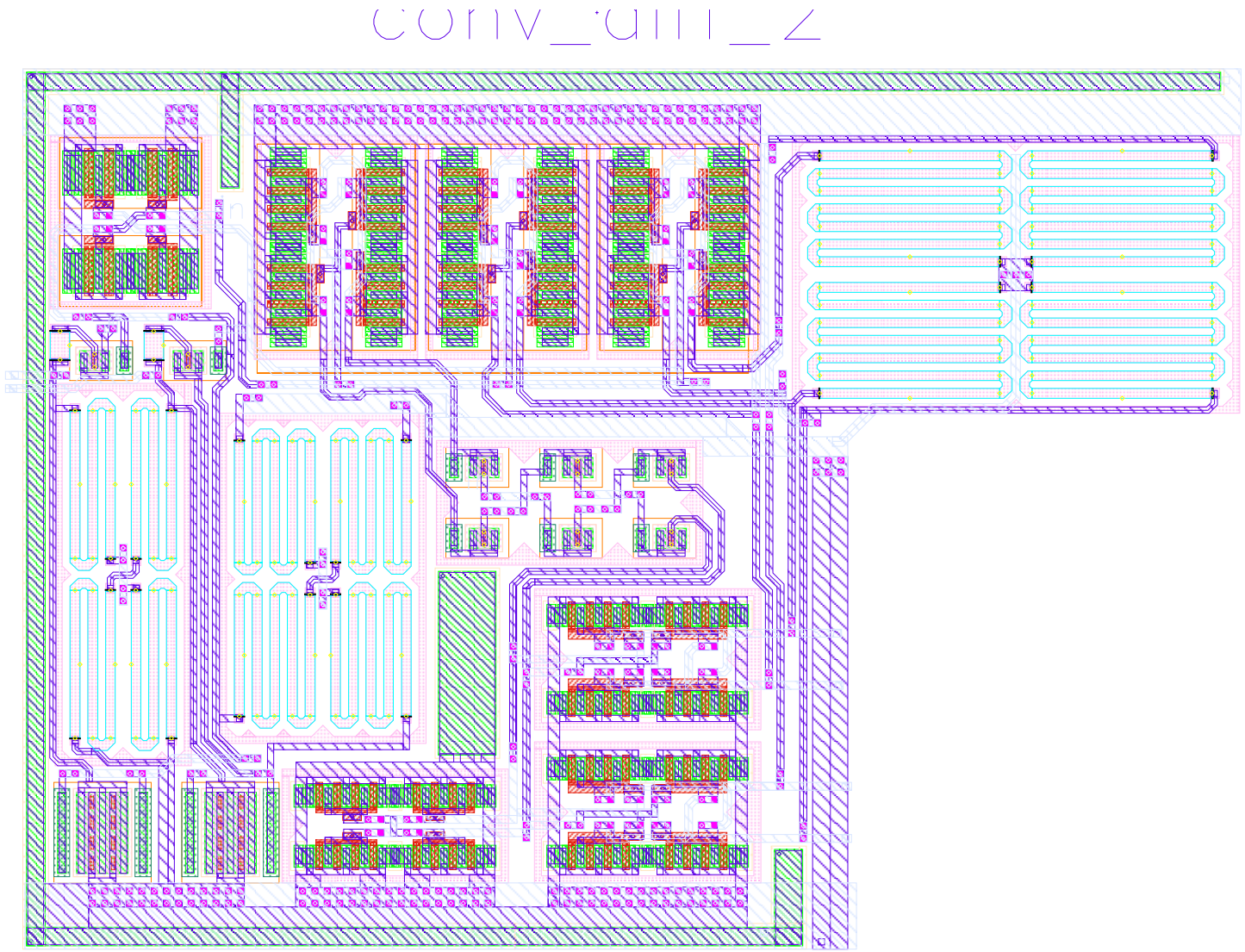
The output noise : $\sigma = 690\,\mu V$.

Channel noise : simulation results (2).

σ (in V) function of temperature (in ^0C)

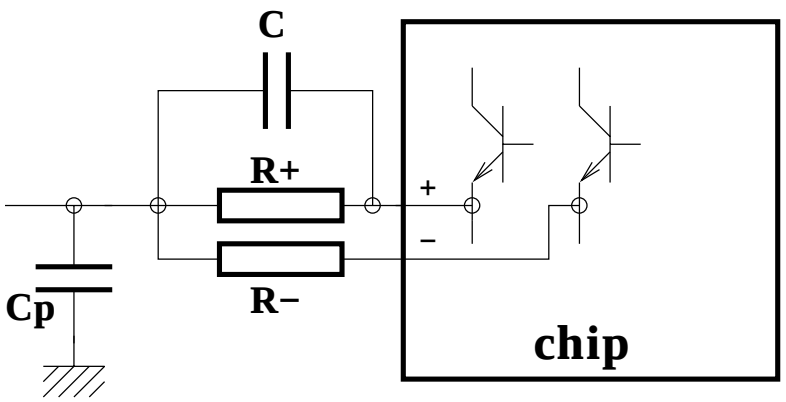


Current convoyer : layout



Current convoyer : gain tuning

It is possible to decrease the gain of the very front end card.



The largest R ($R = R_+ + R_-$) as possible for the noise : $R \geq 5\,k\Omega$

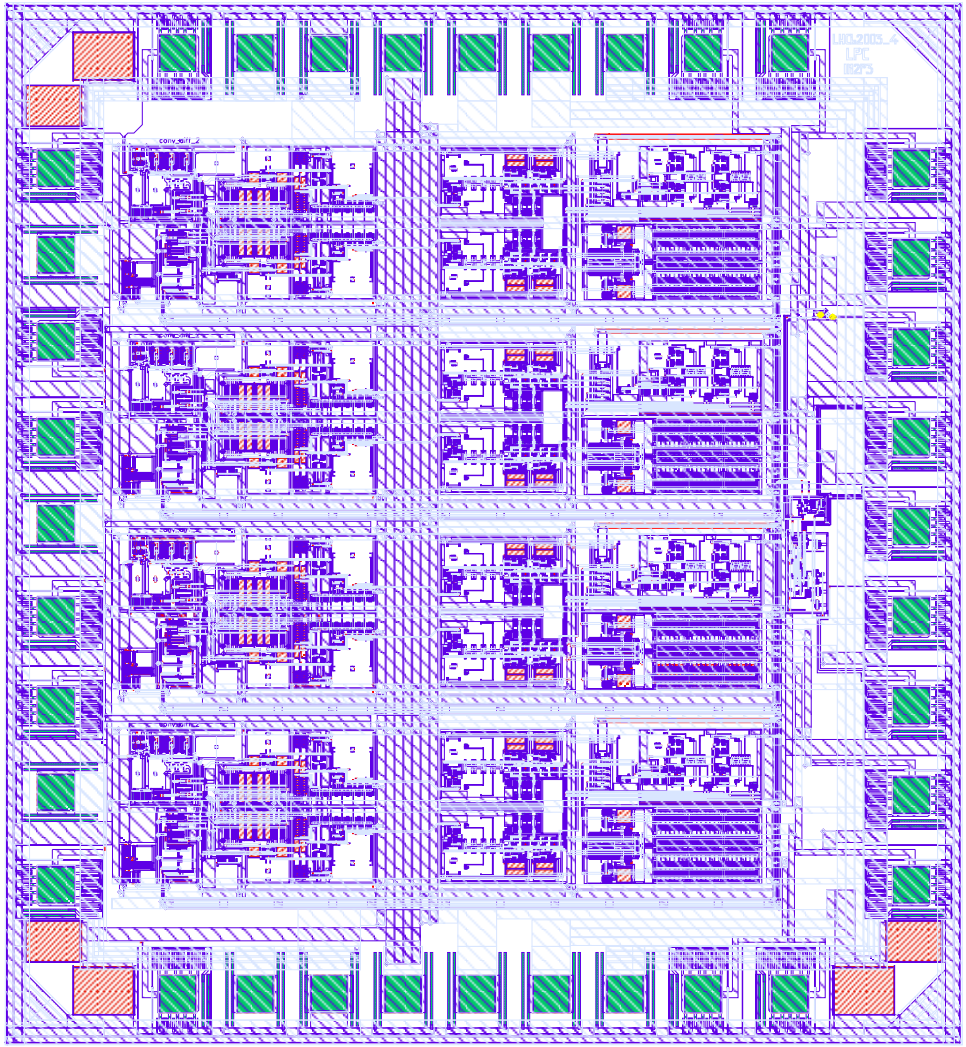
The smallest R as possible for the cross-talk.

$$Gain_{card} = \frac{R_- - R_+}{R_- + R_+} \times Gain_{chip}$$

$$C = C_p \times \frac{R_- - R_+}{2R_+}$$

C_p is the parasitic capacitor ($C_p \simeq 7\,pF$). The tune-up of the C capacitor is very important for the α coefficient !

The layout of the prototype.

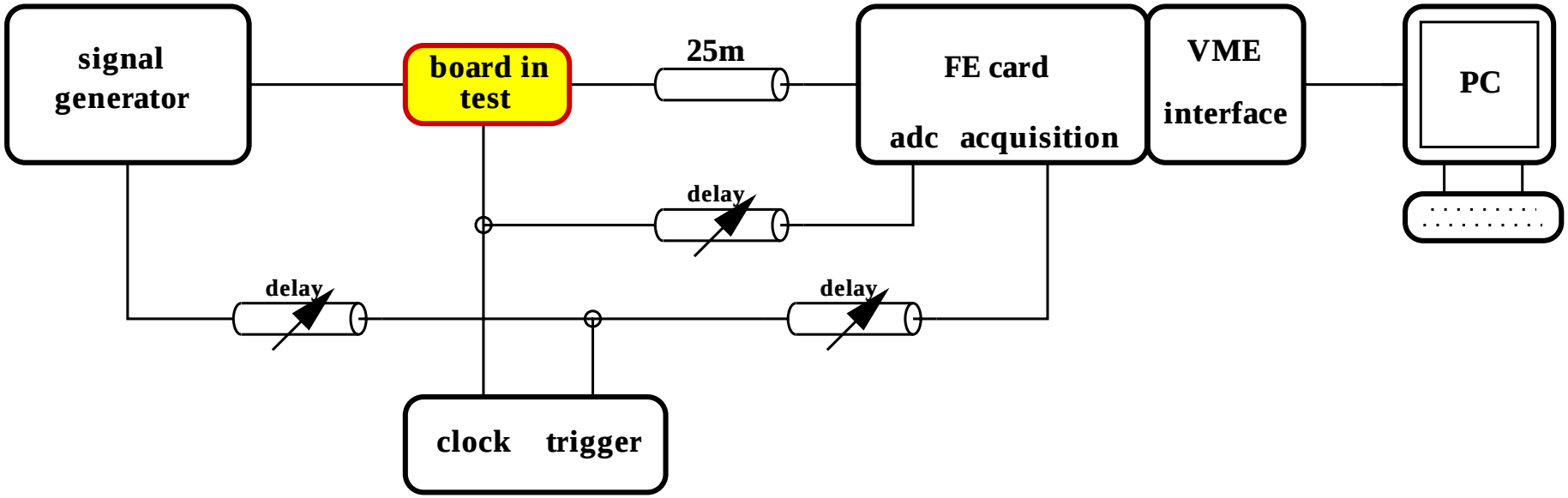


The layout of the prototype.

Large precautions about the power supply lines.

Separated supply lines for the master of current generators. So it is possible to tune the values of the current generator (Never used until now).

The test bench.



Test results :

We have 61 chips since November 2 003.

The gain is good (measurement and simulation with narrow and wide pulse). With a continuous input current, $\rho = 26\,k\Omega$ in simulation, $\rho = 28\,k\Omega$ in test.

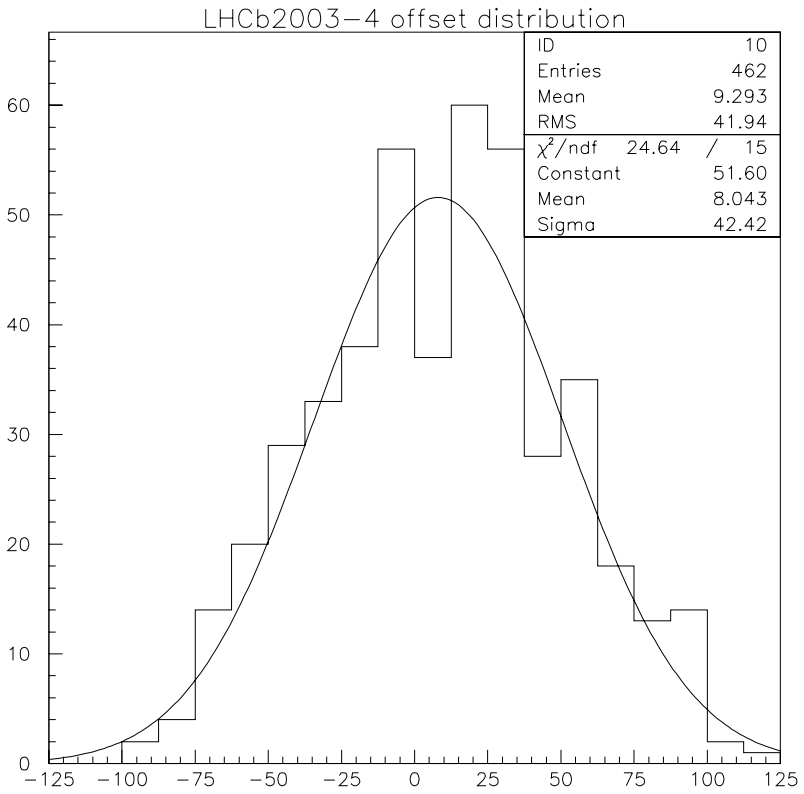
The noise : $\sigma \simeq 1\,mV$.

Two bad chips versus 61 (bounding default), two bad channels ($offset \geq 100\,mV$) versus 244 ; we refuse 4 chips versus 61.

If we reject chips with offset $\geq 100\,mV$, we refuse around 10% of chips.

Consumption : 100m A, 550 mW per chip, good agreement with the simulation.

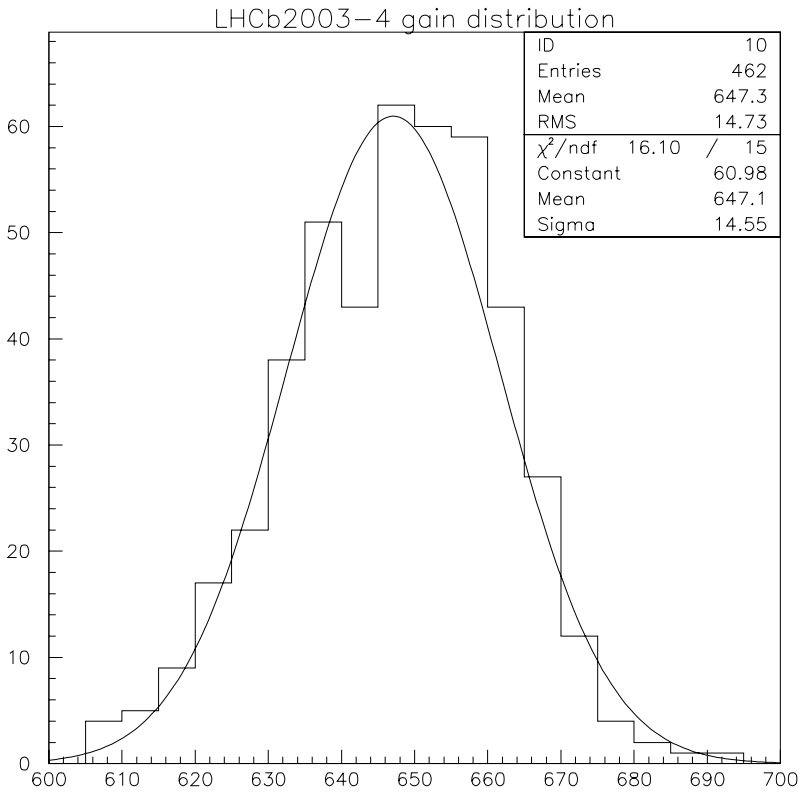
Test results : offset



offset mean value $\simeq 10\,mV$

$\sigma = 45\,mV$

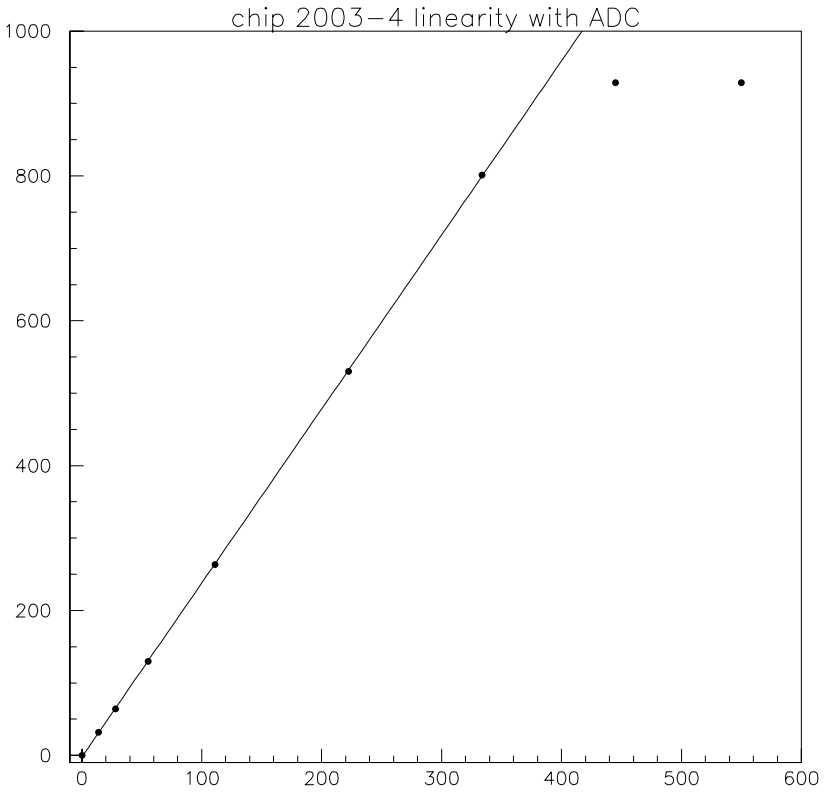
Test results : gain

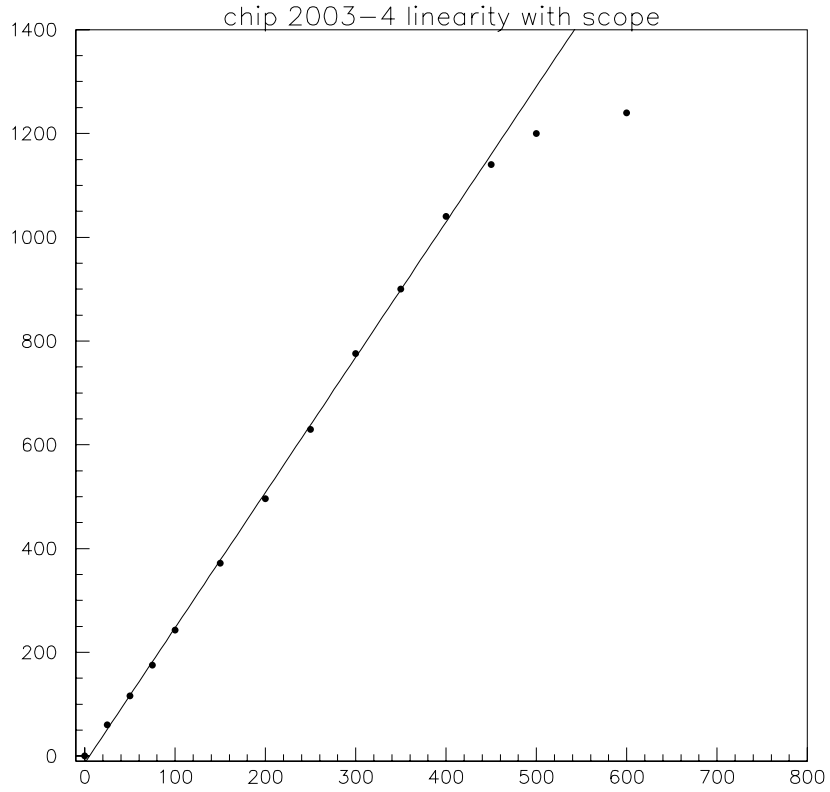


absolute value OK.

$\sigma = 2.5\,\%$

Test results : linearity and dynamics



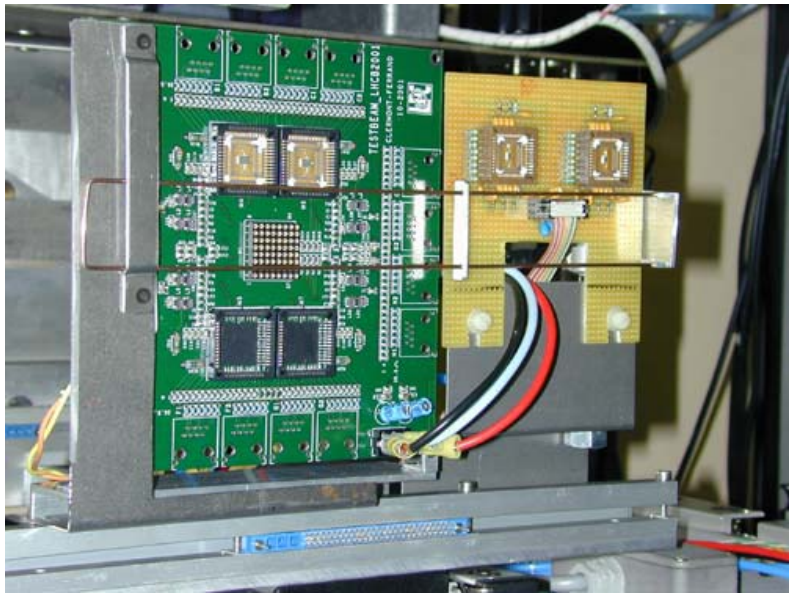


dynamics : 1.1 V

linearity : $better \quad than \quad \pm 5\%$

Irradiation tests

Performed with krypton ions at Ganil with the LAL :



DOSE : no cumulative effects observed : each components exposed to $\simeq 26\,krad$ or 45 years of LHCb.
after irradiations : consumption and functionalities are nominal.

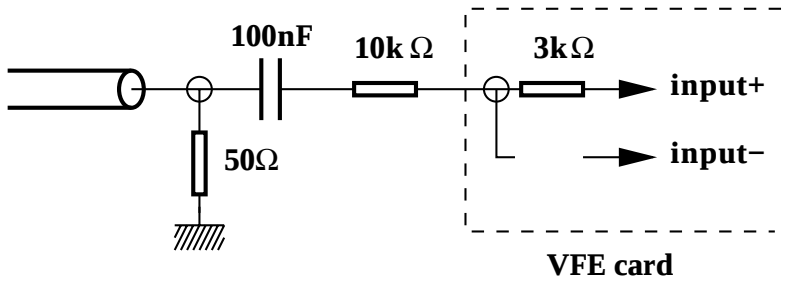
SEL : No SEL observed,
SEL Resistance (SR) :

- December 2 001 $SR > 1\,600\,year/chip$ $(< 0.5\,chip/year)$;
- April 2 003 $SR > 1\,800\,year/chip$ $(< 0.9\,chip/year)$;
- Combined $SR > 4\,000\,year/chip$ $(< 0.4\,chip/year)$.

The VFE card prototype :

We test the VFE card prototype with 16 chips, the clocks and the resets. The test setup is with the FE card after 16 m long RJ45 cable.

At the plus input of the chip there is a $3\,k\Omega$ resistor, and nothing at the minus input. The signal is made with a 100 nF serial condensator and a $10\,k\Omega$ serial resistor. So 1 V gives $77\,\mu A$



The card consumption is 1.70 A for the +2.75 and 1.45 A for the -2.75 A ; i.e. 8.7 W for each card. Good agreement with the simulation.

One LSB on the FE corresponds to 1.15 mV of the VFE card ouput.

The VFE card prototype : noise measurement.

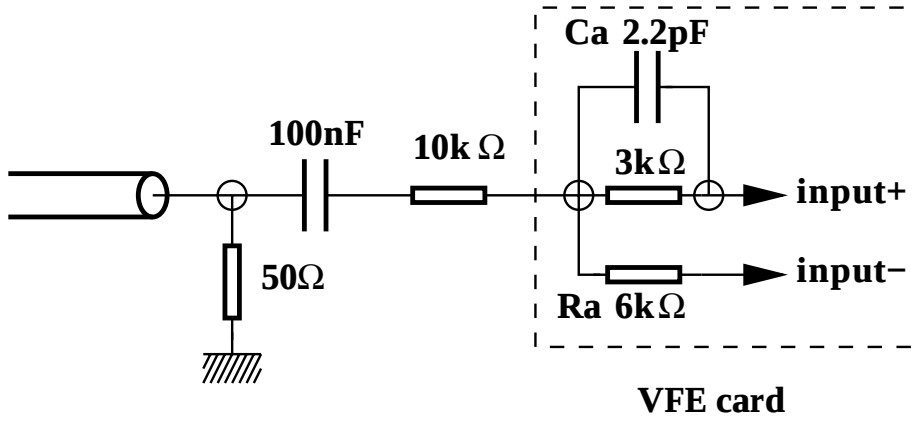
ADC noise : $\sigma = 0.45\, LSB$;

VFE card and ADC noise : $\sigma = 0.85\, LSB$;

$\Longrightarrow$ VFE card noise only : $\sigma = 0.72\, LSB$ wich corresponds to $\simeq 800\, \mu V$ at the chip output.

(simulation of VFE chip noise : $\sigma = 690\, \mu V$)

The VFE card prototype : gain tuning.



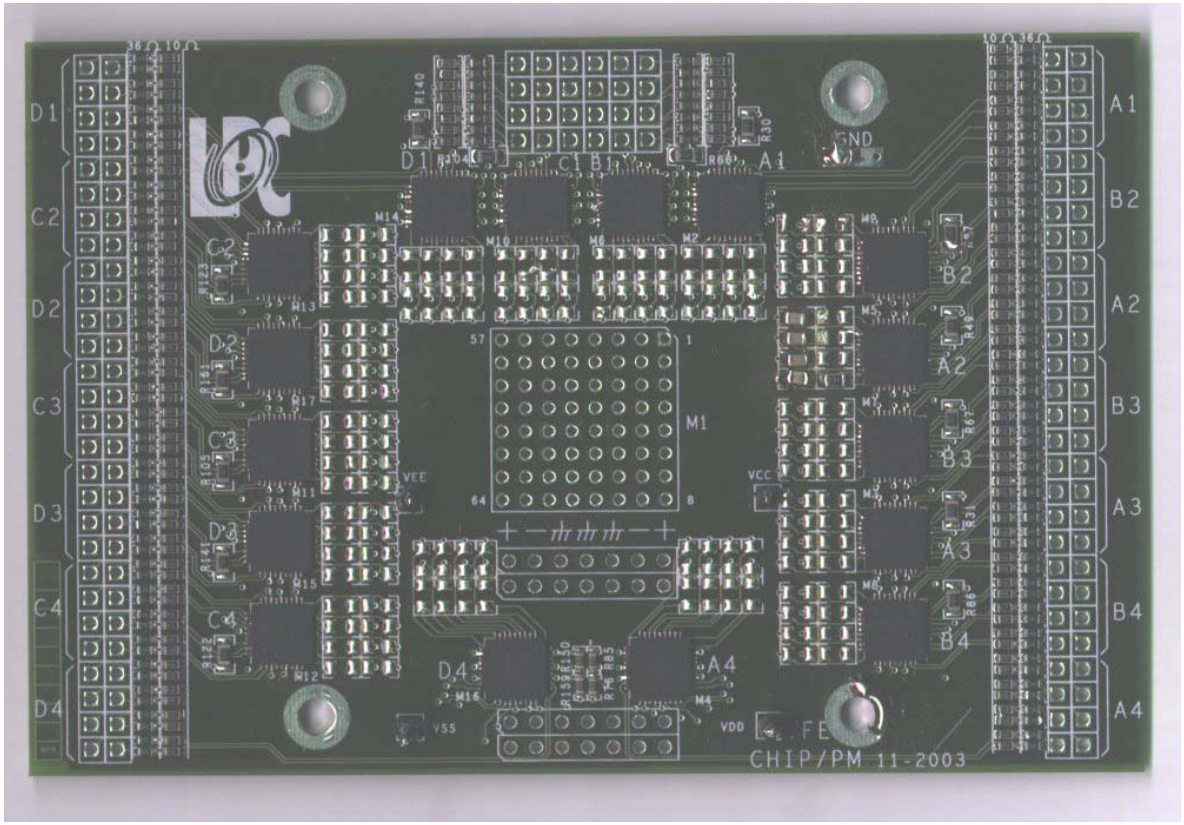
We tune the input signal shape with $Ca = 20\,pF$, $Ra \simeq \infty$:

$Ra = \infty$	$Ca \simeq \infty$	$\alpha = 23\%$	$\alpha_2 = 1.0\%$	$\rho = 28\,k\Omega$
$Ra = 6\,k\Omega$	$Ca = 3.2\,pF$	$\alpha = 16\%$	$\alpha_2 = 0.2\%$	$\rho = 13\,k\Omega$
$Ra = 6\,k\Omega$	$Ca = 2.2\,pF$	$\alpha = 27\%$	$\alpha_2 = 2.7\%$	$\rho = 10\,k\Omega$

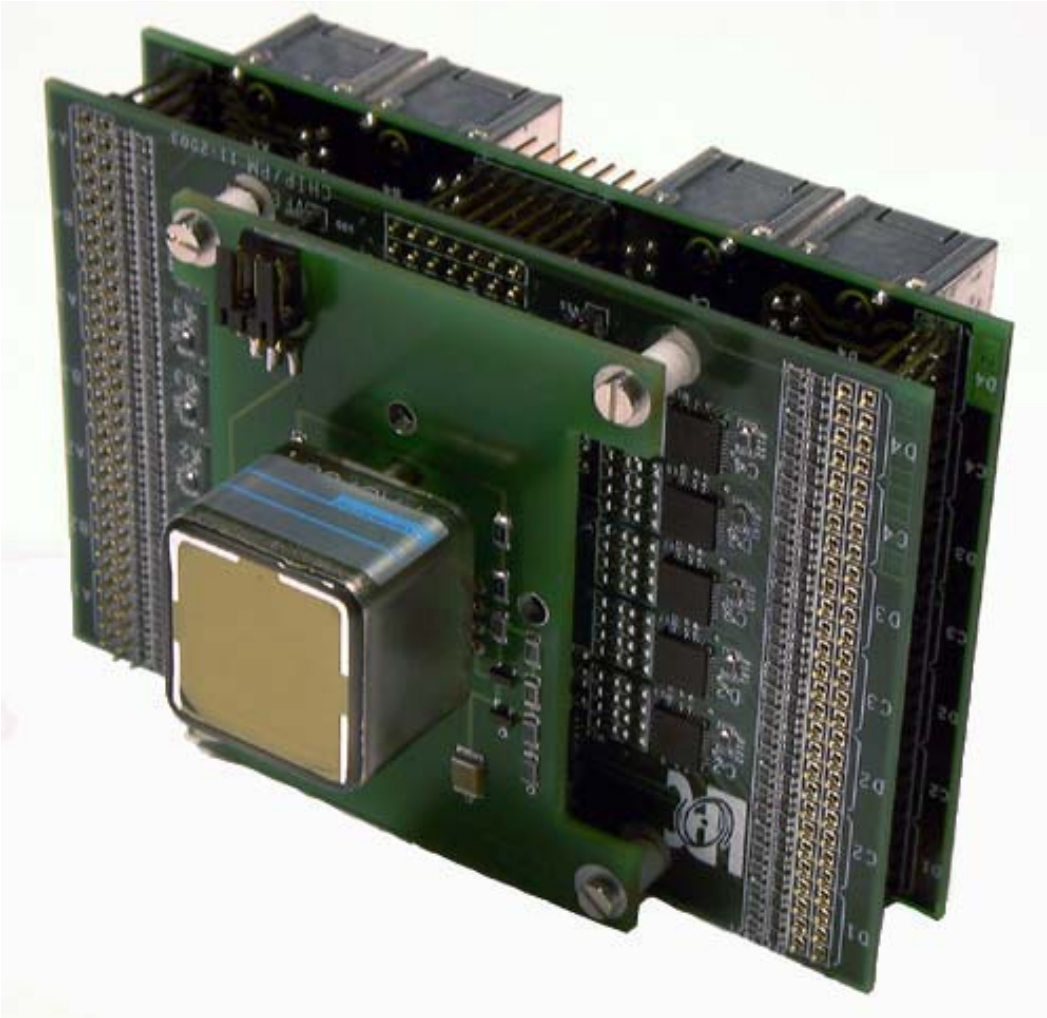
No cross talk, noise unchanged.

$\Longrightarrow$ it is possible to tune the gain, but it is not easy ; the precision to α needs a good precision to the capacitor Ca.

The VFE chip card prototype.



The VFE board prototype.



The VFE chip prototype : conclusion.

The prototype is done and tested with satisfaction.

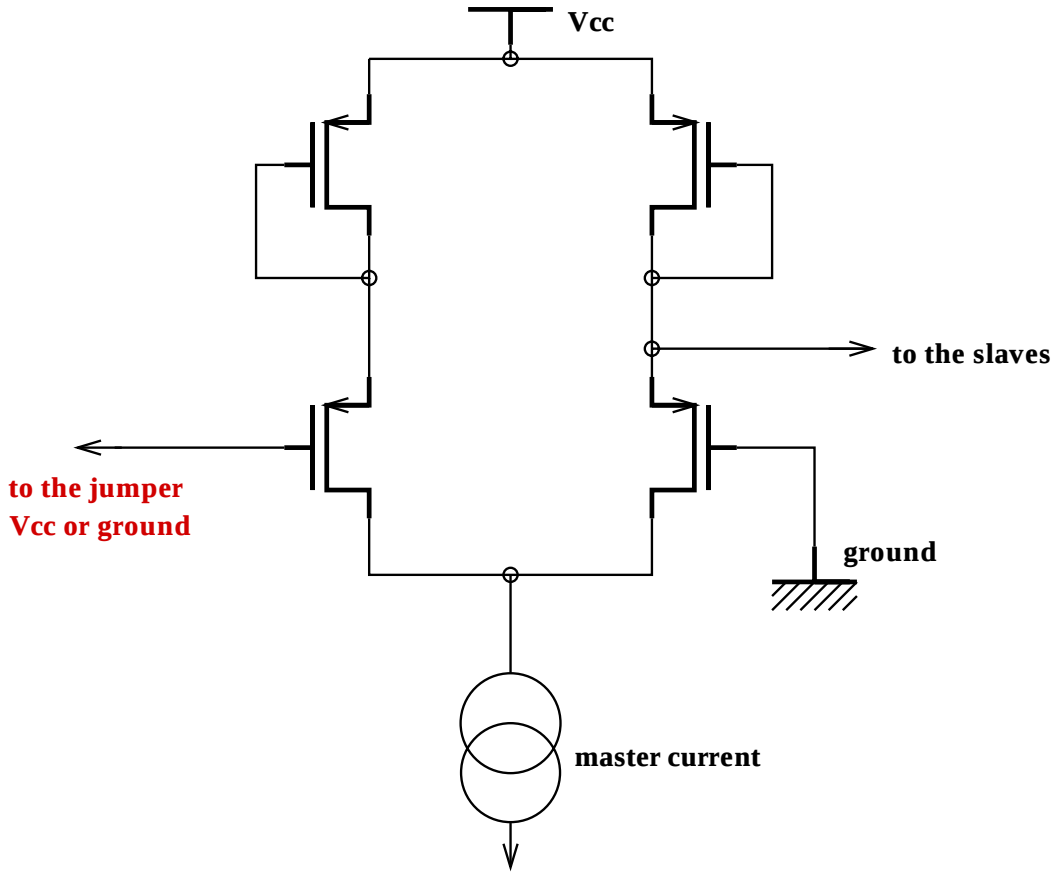
It is possible to tune-up the gain channel per channel on the VFE card, but it is not easy. We have to adjust 64 resistors and capacitors for each VFE card.

It is possible to tune the gain in the FE card, but in this case it is only possible to increase the gain in analog part. This gives up offsets and noise problems.

We have an other project, ready for production : a two gain values project.

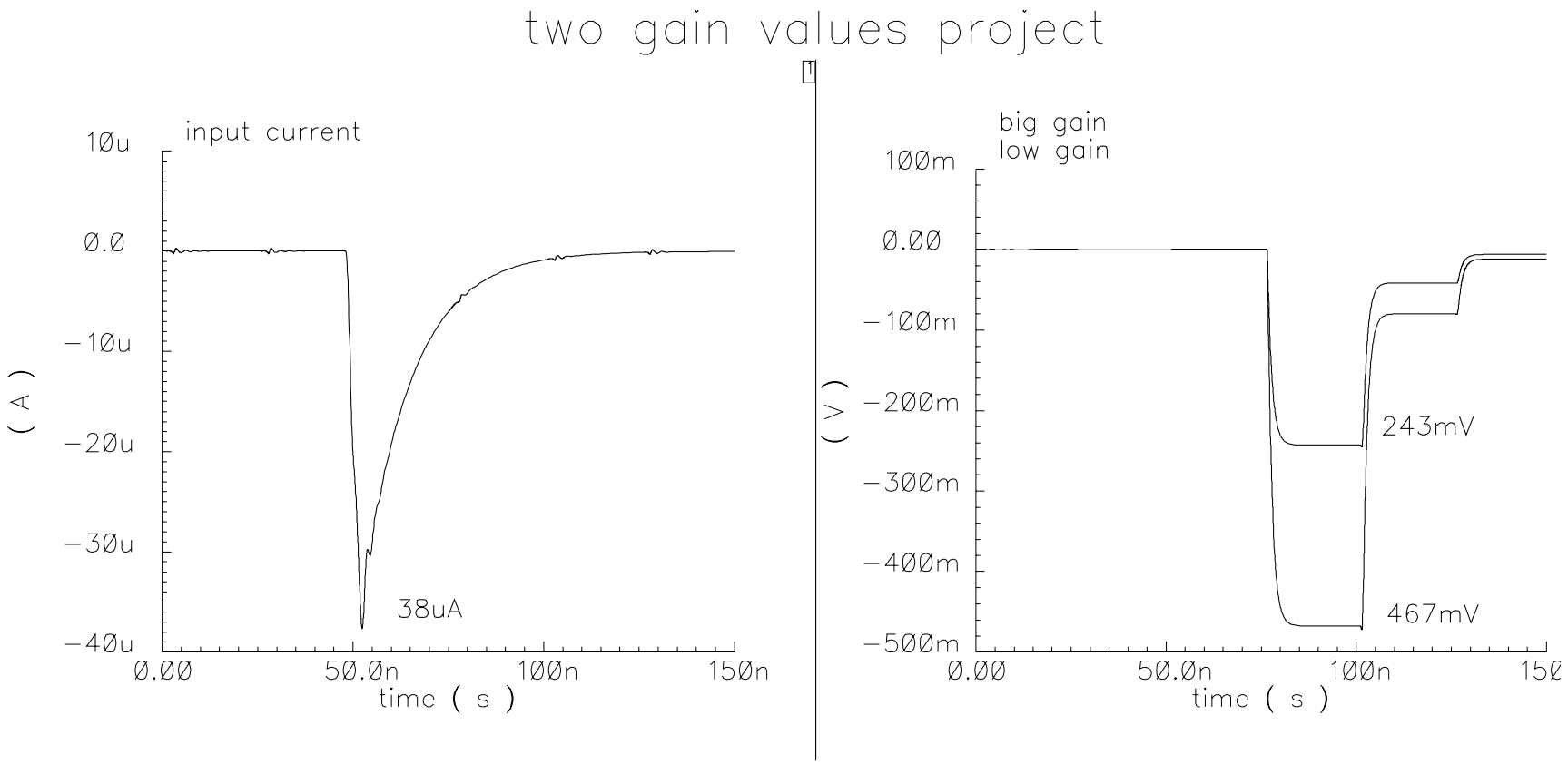
The two gain values project

We modify the current master.



We tune the gain with the jumper. If he is at ground, the current master passes one transistor, if he is at Vcc, the current master passes two transistors, the gain is decreased by a factor two.

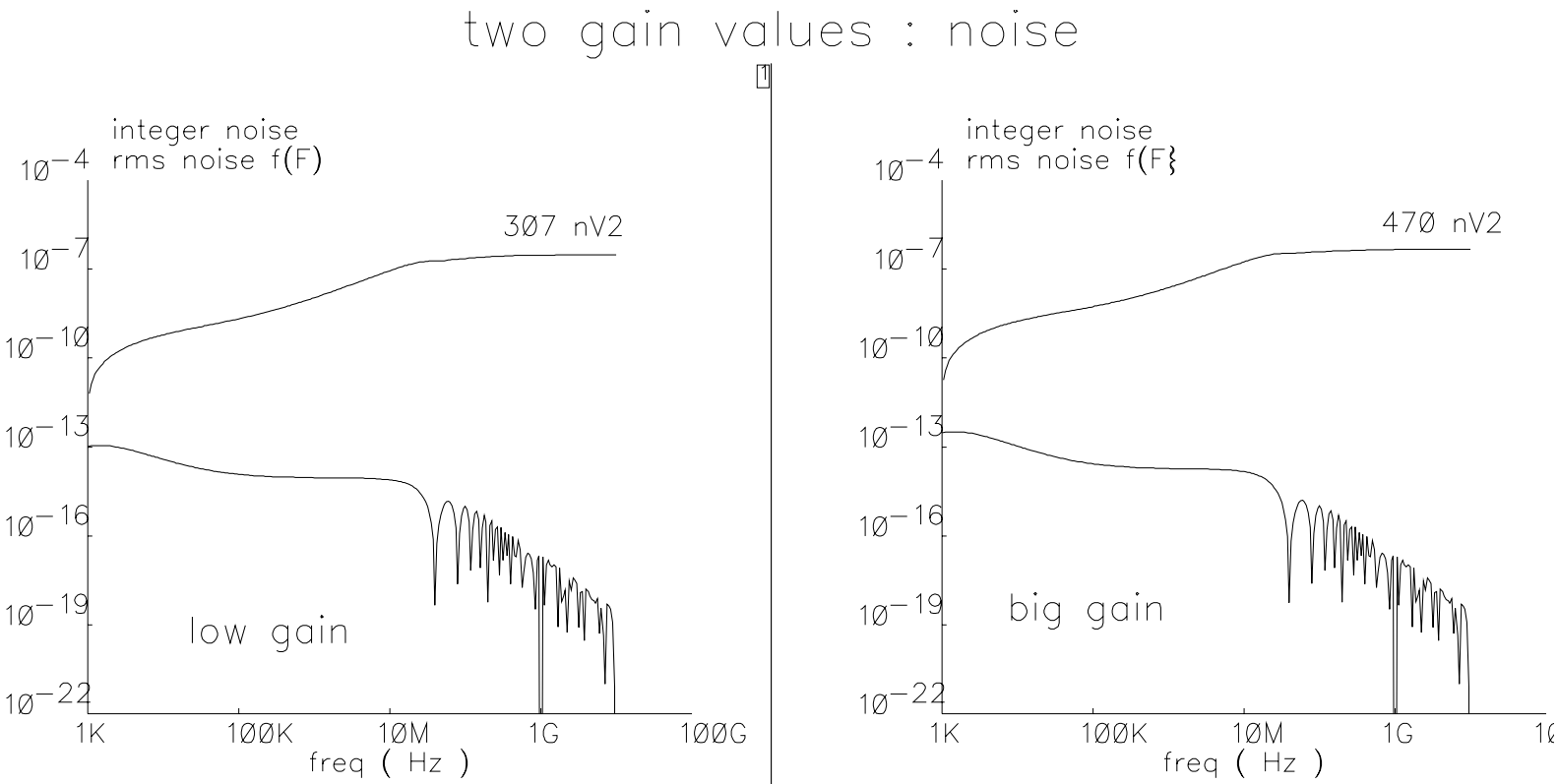
The two gain values project : gain simulation results.



The gains are $\rho = 25.9\,k\Omega$, $\alpha = 17.1\%$ $\alpha_2 = 2.5\%$

and $\rho = 13.4\,k\Omega$, $\alpha = 17.0\%$ $\alpha_2 = 2.5\%$.

The two gain values project : noise simulation results.

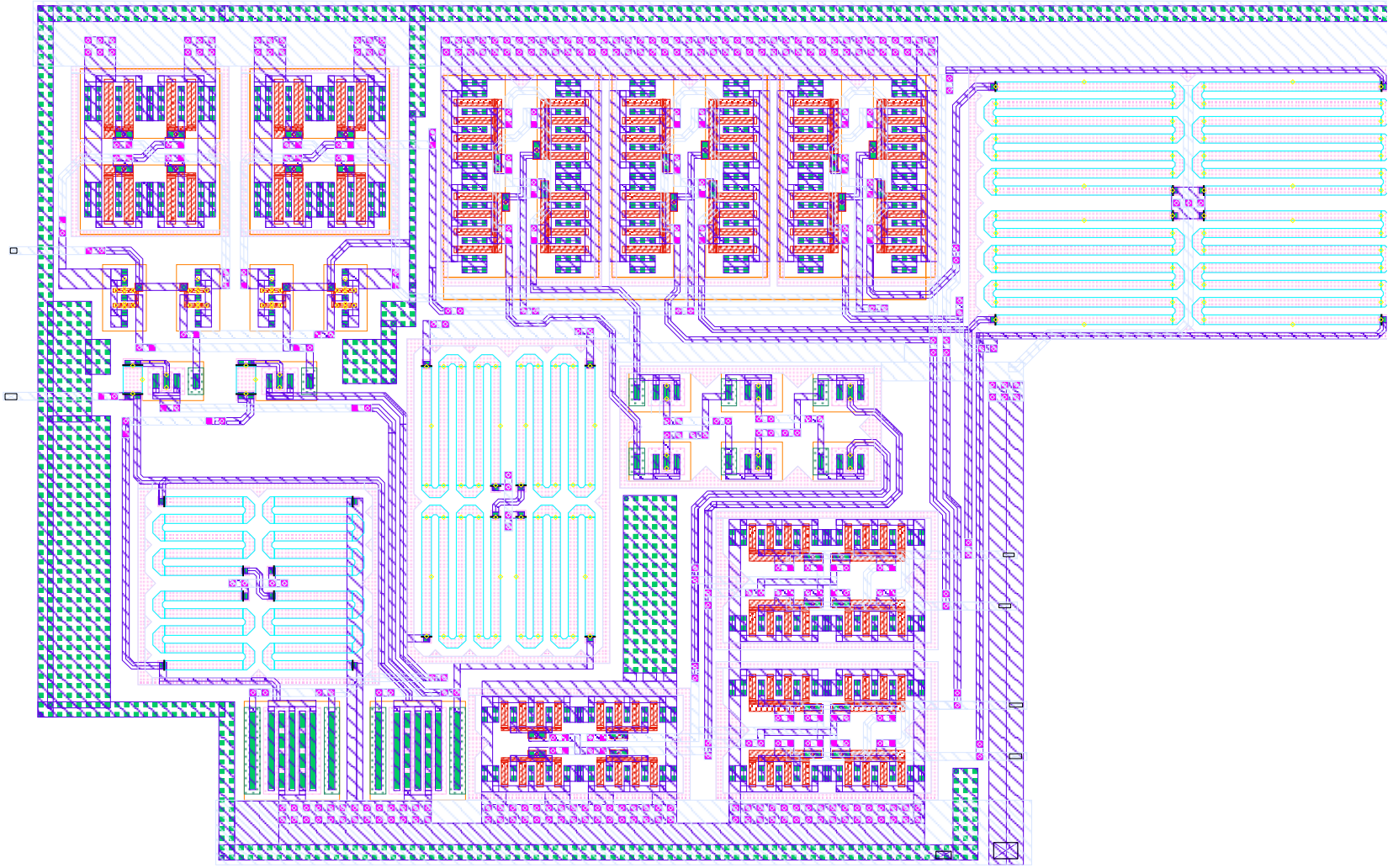


The low gain noise : $\sigma = 560\,\mu V$, it is correct.

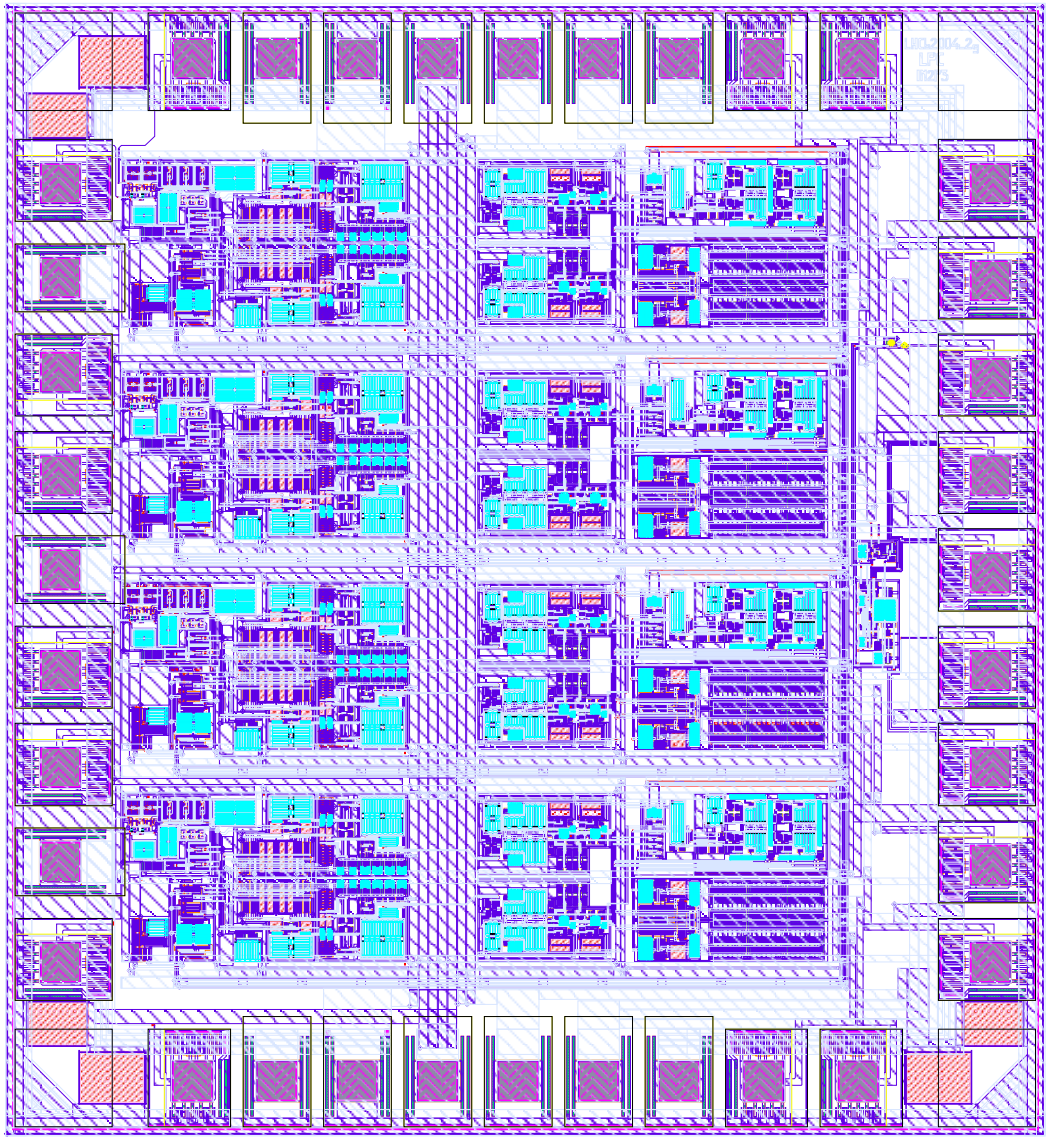
The high gain noise : $\sigma = 690\,\mu V$, it is correct.

Probably the offset is correct : less than or equal to the prototype offset.

The two gain values project : convoyer layout.



The two gain values project : chip layout.



The two gain values project : conclusions

We have a good project in simulation. The layout is ready.

Gain tuning is done by jumper at the VFE board and at the FE board.
4 gains available :

code	VFE gain	FE gain	ρ	ρ^{-1}
00	$13\,k\Omega$	1	$13\,k\Omega$	1 900 fC/V
01	$13\,k\Omega$	1.5	$20\,k\Omega$	1 270 fC/V
10	$26\,k\Omega$	1	$26\,k\Omega$	960 fC/V
11	$26\,k\Omega$	1.5	$39\,k\Omega$	640 fC/V

No more resistors, capacitors, all the boards are identical.

Noise is accurate.

Offset is probably accurate.

Summary

The high gain chip prototype is fine (good tests for the chip, good tests for the VFE card). But difficulties to tune 64 R and C on each VFE card. The cross-talk at the VFE board is $\leq 1\%$.

The two gain chip seems to be the best choice. Noise and offset are OK. All VFE and FE boards are identical. Probably no cross-talk problems. The layout is ready.