A large dynamic range integrated front-end for photomultiplier tubes

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LARGE DYNAMIC RANGE INTEGRATED FRONT-END ELECTRONICS FOR PHOTOMULTIPLIER TUBES

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Abstract

   A full custom analog CMOS circuit for obtaining a photomultiplier readout with a 16 bit resolution over 7 volts has been developed. It is part of the R&D program for the photomultiplier tube front-end readout of the Pierre Auger Observatory northern site. It performs signal duplication and amplification with three gains: 0.15, 1 and 6. Each amplifier has a resolution of 10 bits and can measure signals with durations of several microseconds with a good baseline stability, for an input charge of up to tens of nano-Coulombs. The amplification is performed by current feedback amplifiers with a bandwidth of 60 MHz. The input impedance, adapted to the coaxial cables, is stable over the whole working range.

A prototype was submitted in April 2004 and successfully tested. The linearity over the working range is less than 1 %. It was also successfully tested on the Auger surface detector element installed at Orsay (comprised of a Cerenkov water tank equipped with Photonis XP1805 9" diameter photomultiplier tubes). The resolution over 7 V is 16.6 bits.

This circuit is the first step towards a "system-on-a-chip" (SoC) solution for a photomultplier tube readout equipped with a fast ADC for signal digitization. A setup using a single cable for both the signal and the photomultiplier high voltage power supply was shown to be successful.

Keywords: Front-end electronics, ASIC, large dynamic range

84.30.Le   Amplifiers

85.30.De   Semiconductor-device characterization, design, and modeling

85.40.-e   Microelectronics: LSI, VLSI, ULSI; integrated circuit fabrication technology

1. INTRODUCTION

Astroparticle physics experiments require a large number of photomultiplier tubes (PMTs) for shape measurement over a large range in amplitude and time. This R&D program is being carried out with the needs of the northern site of the Pierre Auger Observatory [1] in mind. The aim is to produce a low cost "system-on-a-chip" (SoC) solution for signal digitization over an equivalent number of 16 bits at a speed of 100 megasamples per second (MSPS). The results form the first phase of this program, the front-end electronics (FEE) developments, are presented in this paper. CMOS 0.35 µm technology was favored as it is regarded as a standard for analog circuits for the coming years.

The field of application is discussed from the northern Auger requirements and uses previous experience gained form the southern site production. The design and the results of tests on prototypes are then presented.

2. FIELD OF APPLICATION

The Pierre Auger Observatory uses 5 000 photomultiplier tubes. They are grouped into clusters of three units. Each cluster manages the power supply and data transmission. The high voltage (HV) supply and control, and the signal digitization is done on the same board and from the same low voltage power supply (LV). This board is placed close to the photomultiplier tube. The digital signal transmission is then performed over long distances. For the northern site, the FEE, HV and LV functions are kept separate from the PMT, then, in case of a failure it is more efficient to replace only the electronics than the electronics with the tube. The above summarizes the basic criteria used in the R&D program.

The northern Pierre Auger Observatory will require an input dynamic range of 16 bits, and signal digitization over 20 µs. The data analysis consists of studying pulses ranging from a few, to some millions of photoelectrons. The pulse frequency range was measured on a prototype of the Auger Surface Detector in Orsay [2] which detects cosmic rays by the Cerenkov effect in 12 m^3 of water. The Cerenkov light is collected with the PMTs. Since the photoelectron distribution can be studied from the pulses' trailing edges, their overall bandwidth was measured and found to range from 1 to 50 MHz. The minimum sampling frequency, calculated from Nyquist's theorem, is 100 MSPS. Under nominal working conditions signal amplitudes can reach values of 150 mA (7.5 V on 50 Ω) or more. This value was set as the upper working limit for the current development.

The solar cell power supplies require a stringent power management. Industrially manufactured HV power supply modules were successfully used in the southern Auger project [2]. For the northern site, a compromise between the ADC input power and consequent output performance is required. The solution presented here proposes to amplify the input on several ranges in order to work with 10 bit ADCs. The overlap necessary to ensure a good cross-calibration leads to the implementation of three different gain ranges (approximately 0.1, 1 and 10).

During the R&D and production phases of the PMT bases [2] the connectors were seen to be one of the most critical elements influencing the failure rate. The number of connectors will therefore be minimized by using the same coaxial cable for both the signal and the tube HV power supply.

The proposed architecture is summarized in Figure 1. In order to reduce power dissipation, which arises mainly from the lines in the PCB (printed circuit board) driving the output buffers, the digitization and serialization will be implemented on the same chip. A reduced number of outputs also increases the reliability.
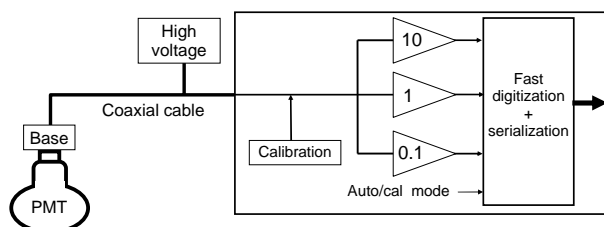

Figure 1 Proposed architecture.

3. DESIGN

A circuit with three amplifiers was designed. The principle is presented in Figure 2. The main difficulty is to ensure a stable input impedance of the circuit and a linear behavior of non-saturated channels whenever a given channel reaches its saturation level. Current feed-

back operational amplifiers (CFOAs) were chosen for this purpose as they maintain a high input impedance, even under saturation. The coaxial cable is terminated by an internal resistance. Its value (50 Ω for the prototype presented) always remains much lower than the amplifier input impedance. This resistance also acts as a voltage divider and consequently, the design is reduced to only two types of CFOAs, namely a follower and a gain 10 amplifier. The bias voltage has to be regulated as it is sensitive to small voltage variations. This is achieved by using an operational transimpedance amplifier (OTA). The coupling capacitors are kept external in order to reach high values, and so baseline variations due to large signals are minimized. The capacitor coupled to ground must have a low current leakage and must also provide a low equivalent series resistance in order to prevent any modification in the CFOAs' bias voltage.
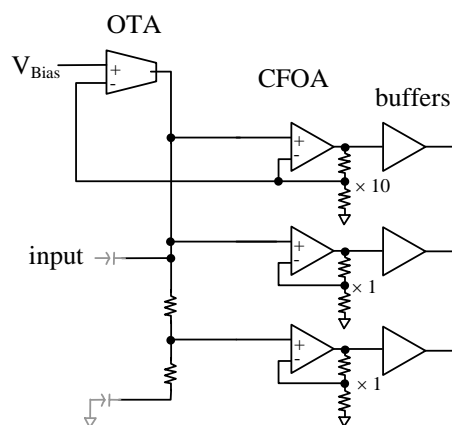

Figure 2 Circuit principle.The external components (capacitors) are represented in grey.

The principle of the CFOA is presented in Figure 3. The non inverting input ("in+" in the figure) is the gate of transistor MP_IN, which provides the high input impedance. The bias voltage determines the current flowing through R_g and therefore the transistor bias current. The non inverting input value commands the drain current. This current is mirrored (by MN1 and MN2) until the output cascade (transistor MN_C), which increases the open loop gain. MN_C is biased by a degenerated current mirror (MP1 and MP2), its function being to prevent the breakdown voltage from being reached with large input signals. The feedback is achieved at the inverting input ("in-" in the figure) by the subtraction of the current in resistor R_f from the input transistor current. The closed loop gain is determined by the ratio of R_f over R_g and the gate-source voltage in MP_IN.
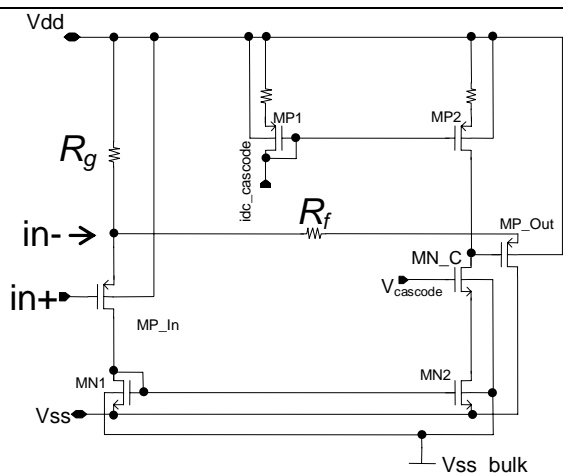
Figure 3 Principle of the CFOA.

The circuit is supplied between 0 V (V_{ss}) and +5 V (V_{dd}). Since this circuit has to measure signals up to 7.5 V, a protection against voltage overloading is necessary. This is the function of the high value series resistances (at the OTA output and the 1 kΩ at the CFOA input). To reach the largest dynamic range, it is necessary to bias the CFOA close to V_{dd}. This led to the use of cascaded transistors on the OTA input (see Figure 4), in order to bias the current mirrors. This OTA is very slow and therefore prevents oscillations that could affect the signal.
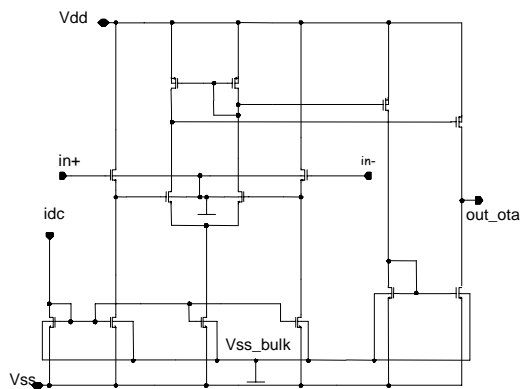

Figure 4 Principle of the OTA for the CFOA input transistor bias regulation.

The total power dissipation is less than 400 µA.

The baseline stability was checked by simulation. A input pulse with an amplitude of 7.5 V on 50 Ω, a 0-100 % rise time of 50 ns, a plateau of 10 ns, and a 100-0 % fall time of 500 ns was injected. This corresponds to a total charge of 42.75 nC, i.e. 1.3×10^6 photo-electrons at a gain of 2×10^5. There is a non-negligible undershoot for the gain 10 channel (of around 90 mV). However, the baseline perturbation is less than 1 mV on the other channels, and is less than 0.5 mV on the G10 output 20 µs after the pulse.

4. PERFORMANCE

The design was submitted to Austrian MicroSystems (AMS) in April 2004. Seven chips were tested on a standard test bench and on a prototype of the Auger Surface Detector.

The main results are presented in Table 1. The three outputs are "G01", "G1" and "G10" for the lowest, medium and highest gains, respectively. The circuits were tested with external output buffers able to drive 50 Ω lines. These buffers (CLC 430) have a 3dB bandwidth of 100 MHz. The rise time results given in the table are obtained after a deconvolution. Though the error bar due to this operation is around 0.5 ns, they are compatible with those of the simulation. Since the necessary bandwidth is 50 MHz (for 100 MSPS digitization), this limit was not a problem, even for noise measurements. Noise was measured with a low noise wideband gain 100 amplifier on the MatacqVME board [3], chosen for its good noise performance (200 µV RMS). Then the resolution was calculated with the assumption that the input noise on the G10 channel corresponds to less than 1 LSB RMS and is found to be 16.6 bits for an input range of 7 V.

The linearity of each channel was investigated by injecting voltage steps at the input, set by a 12 bit DAC. The output amplitude was measured by a 12 bit ADC.

	G01	G1	G10
Gain	0.15	1.3	6.2
1% linearity range (at the input)	>5 V	1.3 V	230 mV
Output noise (µV RMS)	90	90	430
Rise time (ns)	3.1	3.5	6.1

Table 1 Result summary for the outputs. The noise was measured over a bandwidth of 175 MHz. The rise time is calculated after a deconvolution in order to compensate for the output buffer.

The input impedance of this chip was designed to be 50 Ω. It was verified for various input amplitudes by the measurement of reflected signals in a coaxial cable. Steps were injected at the inputs. The input signal was controlled by a digitizing oscilloscope. The reflection was measured after averaging the signals. The measured input impedances range between 48.5 and 51.5 Ω. A slight decrease of 0.4 Ω was observed when the input amplitude was increased from 10 mV to 5 V.

The effects of using a single 3 meter long cable for the high voltage and the signals were measured with a Photonis XP1805 photomultiplier tube in a light tight box. Light pulses were generated with a pulsed LED. The signals were acquired with the MatacqVME board. A first set of measurements was carried out with a standard resistive base. A second set was carried out with a base for which the signal was brought by a 75 Ω high voltage coaxial cable. The trailing edge durations were compared: both measurements in standard configuration and with the "G01" output are around 8 ns. No degradation in noise was observed.

Measurements with large amplitude pulses were performed on the Orsay Cerenkov 12 m^3 water tank, on a single Photonis XP1805 9" diameter photomultiplier tube equipped with the Auger base. Its output was split in two by a large bandwidth power divider (manufactured by JFW industry and designed to work up to 4 GHz). A signal was directed to the first channel of the Matacq board, the other sent directly to the test board. The PMT gain was multiplied by two to compensate for the effect of the splitter. The three output channels were also directed to the Matacq board. The acquisition was triggered by the board's internal comparator. An example of a single muon signal response is shown in Figure 5. Signals of up to 8 V were detected on the input. The 1 % linearity limit of amplifier G01 was measured around 7 V. The signal recovery after saturation is less than 100 ns. The circuit performance was not altered after several days of continuous working in stable conditions. The series resistance at the input of the amplifier is sufficient to protect against the effects of large amplitude pulses.
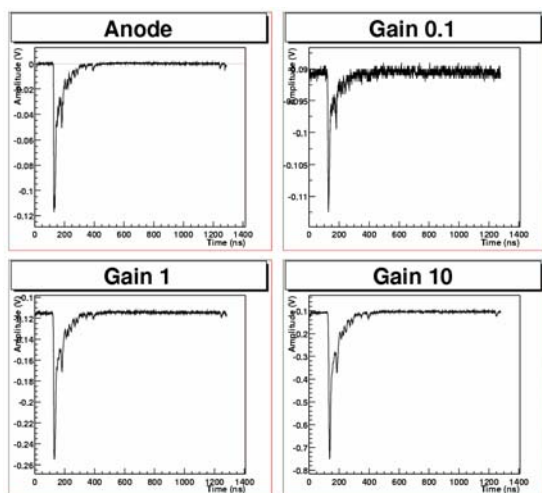

Figure 5 Comparison of the input signal ("anode") with the three outputs of the circuit. The signal comes from the anode of a PMT of the Orsay Cerenkov water tank. The offset is due to the test board external buffers.

5. CONCLUSIONS

A front-end circuit for photomultiplier tubes was developed in AMS CMOS 0.35 µm technology. It has an input dynamic range of 16.6 bits over 7 V. This performance is achieved by splitting the output over three ranges (gains of 0.15, 1, 6.2). The architecture ensures a stable input impedance over the whole working range, which is essential to work with coaxial cables. The saturation of one channel does not interfere with the others nor with the input impedance. The smallest bandwidth of the three output channels is 60 MHz. This is enough for signal digitization at 100 megasamples per second (MSPS).

A further design will implement a built-in calibration for the amplifers as well as a 100 MSPS 10 bit FADC. Cable impedance matching has also to be validated, because the measured input impedance differed of up to 1.5 Ω for the seven valid circuits tested.

We plan to integrate this circuit in a "system-on-a-chip" (SoC) for PMT signal digitization.

6. REFERENCES

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