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Abstract

The Silicon Strip Detector (SSD) forms the two outermost layers of the Inner Tracking System (ITS) of ALICE. The SSD detector consists of 1698 double-sided silicon microstrip modules. The electrical connection between silicon sensor and the front-end electronics is made via TAB-bonded aluminium-polyimide cables (chip-cables). The module assembly is challenging because of the module geometry and the use of chip-cables. This article describes the assembly procedure and the test protocol used.

1. Introduction

ALICE [1] is one of the four experiments that will be installed at the Large Hadron Collider (LHC) at CERN. The ALICE detector has been designed to operate in the high track density environment which is typical of relativistic heavy ions physics. The Inner Tracking System (ITS, [2]) consists of six layers of silicon detectors: the two innermost layers are Silicon Pixel Detectors (SPD), the two intermediate layers are Silicon Drift Detectors (SDD) and finally, the two outermost layers are Silicon Strip Detectors (SSD). In this paper the SSD detector assembly will be described from the initial production phase up to the final quality controls of modules.

2. The SSD detector

The ALICE Silicon Strip Detector is formed by two concentric cylindrical layers whose radii are 384 mm and 434 mm, respectively. Each layer is formed of about one-meter long carbon fibre ladders, which overlap in azimuth. There are a total of 72 ladders: layer five counts 34 ladders, each populated with 22 modules, while layer six counts 38 ladders, each populated with 25 modules [3]. In each ladder, modules overlap along the Z-direction.

A module is composed of a double-sided silicon microstrip sensor read by two hybrid circuits, each populated by 6 front-end chips (see fig. 1). The sensor is 300 μm thick and has a 35 mrad stereo angle, which is obtained by tilting the implanted strips of 7.5 mrad on the p-side, and of 27.5 mrad on the n-side. There are 768 strips on each side with a pitch of 95 μm. Each hybrid is obtained by connecting 6 HAL25 chips [4,5] to an aluminium-on-polyimide hybrid circuit (flex), which is supported by a stiffener of carbon fibre. The flex hosts power lines as well as digital and analog lines needed for driving and reading the chips. Electrical connections, chip-to-sensor (128 connections) and chip-to-flex ($\sim$55 connections), are made by means of a chip-cable

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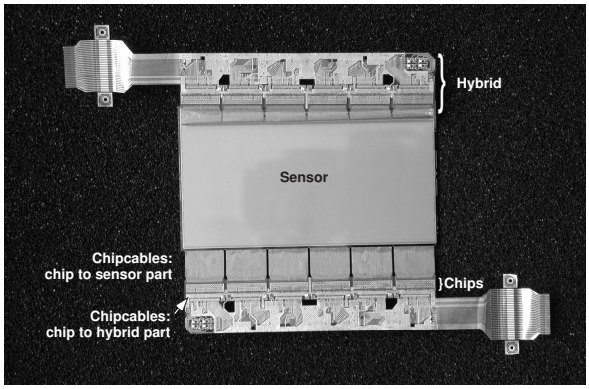

Fig. 1. A SSD-module in the so-called flat configuration. Bottom (Top), a hybrid is connected to the sensor rear (front) face. The chips do not appear since they are hidden by the chip-cables.

[6]. A chip-cable consists of a network of 14 μm thick aluminium traces supported by a 10 μm polyimide foil. Chip-cables fit in a plastic frame in order to facilitate both their handling and testing. They are connected via a Tape Automatic Bonding (TAB) technique; that is the traces are directly bonded to the component pads without any additional wire. The HAL25 chip has been developed by LEPSI [7] in a 0.25 μm CMOS technology. HAL25 is 11 mm long, 3.8 mm wide and it is as thin as 150 μm in order to minimise the mass of the detector. HAL25 is a mixed analogue/digital chip, designed to be radiation tolerant, and to stand a wide range input range of about $\pm$ 300,000 electrons.

3. Assembly procedure

The SSD detector consists of 1698 modules. However, the overall number of SSD modules to be produced is about 2000 modules (including spares), which means 4000 hybrids, $24 \cdot 10^3$ chips and chip-cables connected for a total of $\sim 10^7$ TAB-bonds. These large numbers require an efficient assembly procedure and an exhaustive test protocol. The module production is shared among three sites: Helsinki, Strasbourg and Trieste.

In order to keep the material budget as low as possible, the connections are made by using 24 μm thick aluminium/polyimide chip-cables.

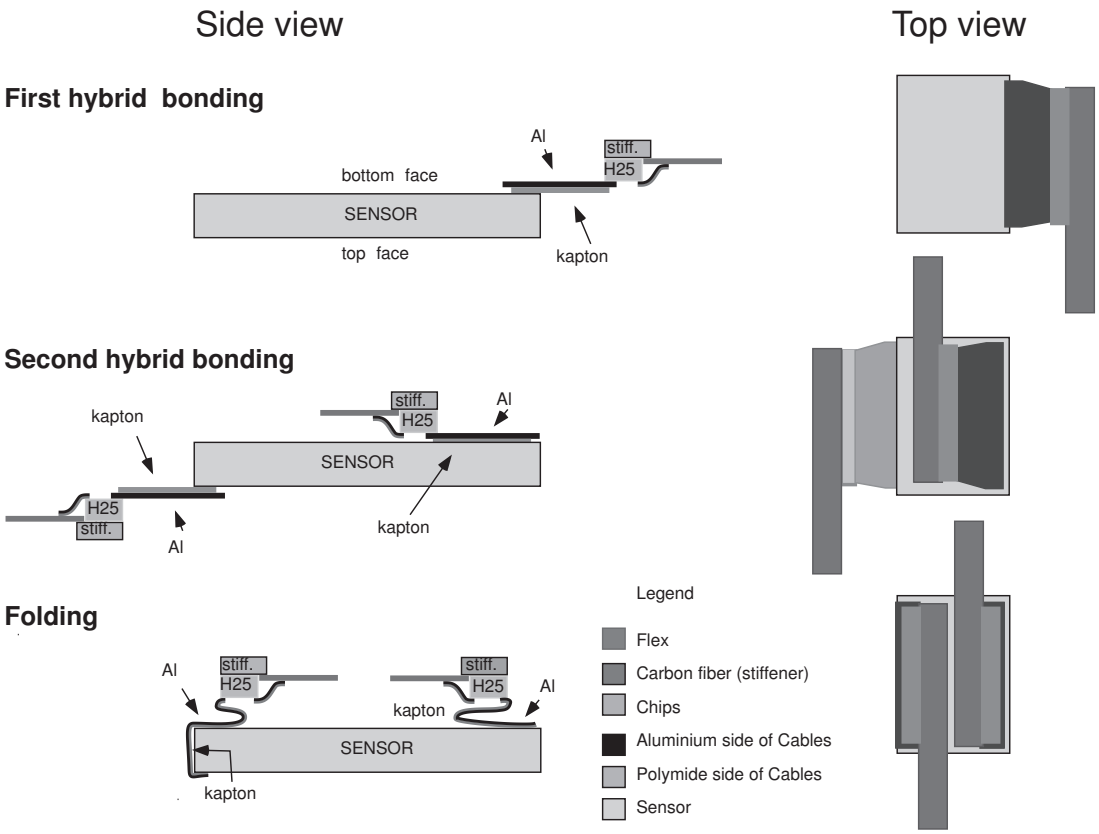

Fig. 2. The figures sketches the assembly procedure of a hybrid pair on a sensor.

This choice also facilitates the folding of hybrids on top of the sensor (see fig. 2). However, there are some drawbacks related to the TAB-bonding technique. For example, the damaged parts of a module are difficult to exchange, and the parts to be assembled must be carefully aligned.

The first assembly step is joining chips to chip-cables, thus forming tabbed chips. Tabbed chips are then mounted on a sub-hybrid to make a hybrid, and finally two of them are micro-connected to a sensor. Sub-hybrids are the only parts which are pre-assembled having SMDs mounted on them.

The amount of pieces to be arranged calls for an industrial process, which in Trieste is accomplished in collaboration with a private company [8]. The Trieste's approach will hereafter be described. The parts to be assembled are hosted in separate jigs, which however can be composed in order to build a module. The newly formed module is then tested. All the bonding operations are performed using a Palomar 6300 bonder, operating at 60 kHz.

The production is organised such as to divide the complex process of module assembly and testing in handy sub-processes. The sub-processes are largely automated to speed-up the production rate; however a number of operations are manually made by operators. Two separate sets of jigs have been designed and machined: one is used to connect chip-cables to chips, the other is for the assembly of hybrids and modules. The first of the two sets consists of two coupled holders (see fig. 3): one hosts a chip the other hosts a framed chip-cable. Both holders have mechanical references to roughly align a single component, and a vacuum system to keep it firmly in position. The coupled holders fit in a four axis (x, y, z, θ) aligning system, where an operator

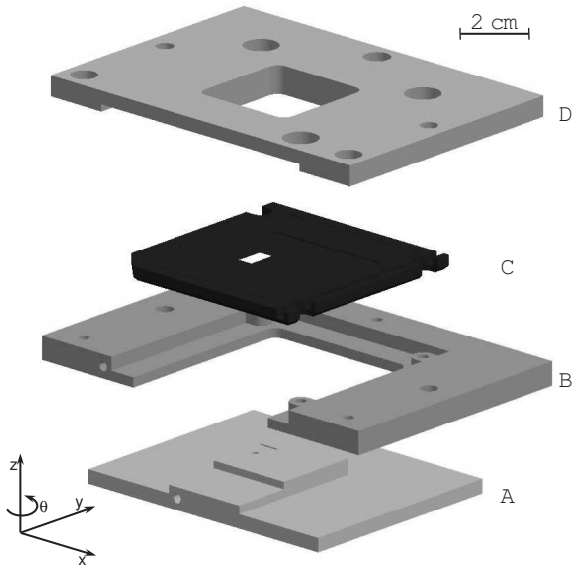

Fig. 3. Exploded view of the jig used to connect chip-cables to chips. A chip is initially accomodated in the lower holder (A) while a chip-cables, in its frame (C), is sandwiched between the cable holder (B) and the mask (D), which keeps the cable flat. The whole system is subsequently aligned by means of a specific tool.

completes the alignment by drifting the chip holder guided by a microscope. The matching required between chip-cable pads and chip pads (better than 5 μm) can be achieved in less than a minute. Vacuum and mechanical locks keep steadily in position the chip and chip-cable holders which can be removed from the alignment station and stored on the bonder feeding buffer.

The second set of jigs is formed of a hybrid holder, an aligning base and two module holders. The hybrid holder is equipped with seven separate vacuum lines to keep in position a sub-hybrid and six tabbed chips. The sub-hybrid position is defined by mechanical references. In the hybrid building phase, the hybrid holder is placed on the aligning base, where also a dummy sensor sits. Mechanical references maintain the sub-hybrid parallel to the sensor and at the right distance from the sensor pads, while the alignment in the orthogonal direction is made visually. Once this procedure is accomplished, the operator glues the six tabbed chips on the sub-hybrid by using the dummy sensor pads as reference. The alignment is done chip-by-chip; once achieved, the position is held firmly by a vacuum system. When all the six tabbed chips are aligned, the hybrid holder is removed from the aligning base and then stored to allow the glue to cure. Finally the holder is shifted to the bonder for interconnecting the tabbed chips to the sub-hybrid. In the last phase, two hybrids are mounted on a sensor in two steps according to the scheme of fig. 2. In the first step a sensor is accommodated in the first module holder and a hybrid is connected, thus forming a half-module. In the next step, the half-module is initially flipped up side down and then accommodated on the second module holder and finally the second hybrid is aligned and interconnected. In both steps, the hybrid holders keep the hybrid face down while mechanical references maintain the system aligned. Once a fine alignment is reached, vacuum and mechanical locks hold the hybrid in position. The system is ultimately shifted to the bonder feeding buffer.

4. Quality protocol

The quality of each operation is constantly monitored since the final goal is to keep the amount of defective module channels below 2%. The quality protocol is applied to all the components:

- sensors are tested at the INFN-Trieste laboratories [9];
- chip wafers are tested on a sample basis before thinning and dicing;
- sub-hybrids are tested by the producer;
- chip-cables are dimensionally checked using the optical system described in [10].

The quality of bonds is monitored via visual inspection and destructive pull-tests on samples. An acceptance test is done at each step of the production. The large amount of tests needed along with the necessity to compare the output from the three production sites call for an automated test. For this purpose, a so called TestBox and software were developed [11]. The TestBox is coupled to a PC, which is equipped with two ADC cards. The TestBox generates all the signals necessary to test a single HAL25 chip as well as the six daisy chained chips which form a hybrid. Chips are connected to

the TestBox via a "chip-adapter", a clamshell unit designed to fit tabbed chips. The hybrids are connected to the TestBox via a pitch adapter. A software program, written in LabView, runs a complete series of tests and saves the results in a report file. The test procedure is articulated as follows:

- the system automatically recognises, via JTAG, wheter a tabbed chip or a hybrid (or nothing) is connected;
- the JTAG registers are checked and a boundary scan is performed;
- the current consumption is checked;
- the pedestal and noise of each input channel are measured;
- the gain of each channel is tested by using the chip internal pulser;
- a search for open inputs and short-circuited inputs is performed;
- the bad channels are spotted by setting a threshold to the pedestal, noise and gain values.

The full test takes 30 seconds for a chip, and about a minute for a hybrid. Care must be taken in selecting the correct thresholds, in order to have stable and reproducible results.

A distinct test set-up was developed for automatic module testing. The system makes a complete test of a module, which includes an I−V curve, automatic definition of depletion voltage and search for open channels, for short-circuited bonds and for sensor-related defects (broken AC, etc.). A full test takes about 10 minutes.

5. Conclusions

An assembly procedure and a test protocol have been set up for the ALICE silicon strip modules. At present, the production has reached quota 1000 modules. Production yields are $> 90\%$ for tabbed chips (chips are just tested on a sample basis before dicing), $> 95\%$ for hybrids and $> 90\%$ for modules ($\sim 75\%$ before repairing). The collaboration between the Istituto Nazionale di Fisica Nucleare (INFN), Trieste and a private company (MIPOT) has been successful.

6. Acknowledgments

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