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FLC_SIPM: Front-End Chip for SIPM Readout for ILC Analog HCAL

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An integrated front-end chip has been developed to readout the Silicon PM for the ILC analog hadronic calorimeter. It is built around a variable gain low-noise preamplifier followed by a variable peaking-time shaper (20-200 ns), track and hold and multiplexed output. This structure allows to produce single photo electron spectrum with well separated peaks for absolute calibration at fast shaping (40ns) as well as physics signals from the scintillating fibers (up to 2000 photo-electrons) with a slower shaping (150ns) compatible with the W-Si Electromagnetic Calorimeter DAQ. Besides, an input DAC allows to tune the detector gain by varying the operating voltage by up to 5V. The chip accommodates 18 channels and 1000 circuits have been produced in 2004, the design and the measurement results of which will be presented.

1. INTRODUCTION

A hadronic calorimeter prototype is now designing for ILC with scintillator tiles read by silicon photo-multipliers (fig. 1), developed by MEPhI and PULSAR[1]. Dimension of that prototype is around 1m³ with scintillator tiles from 3 by 3 cm to 12 by 12 cm over 36 layers for high granularity. The silicon PM (SiPM) is a matrix of pixels directly coupled to the tile (fig. 2) and the tiles are grouped to form a mini HCAL with around 10000 readout channels.

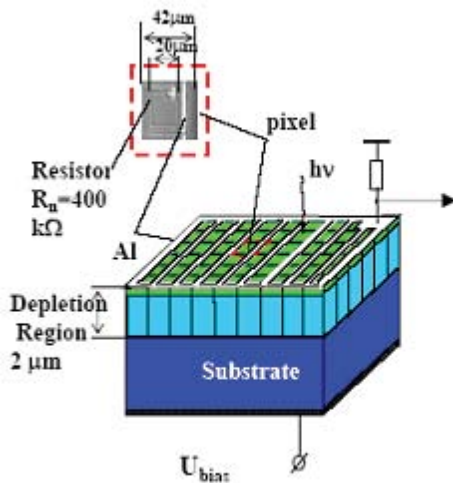


Figure 1: Silicon photo-multiplier schematic

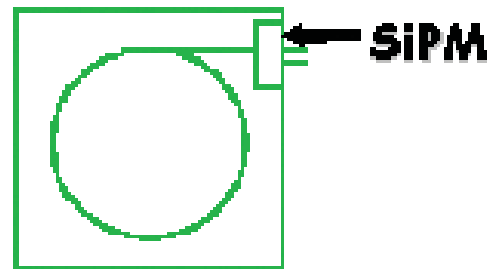


Figure 2: tile with SiPM

A front-end chip has been developed to read out 18 SiPM. This paper describe that chip (fig. 3) called “flc-sipm”. Its general architecture will be explained and measurements will be shown.

1.1. SiPM electronic characterisation

When the PM works with a gain of 106, the photo-electron is a signal of 160 fc and the MIP taken at 20 p.e. gives a signal of 3.3 pc. The maximum signal is around 120 MIPs so the input dynamic range of the circuit should be 400 pc. The SiPM pulse shape is set by the wavelength shifter fiber : it is a very fast signal with a rise time of few

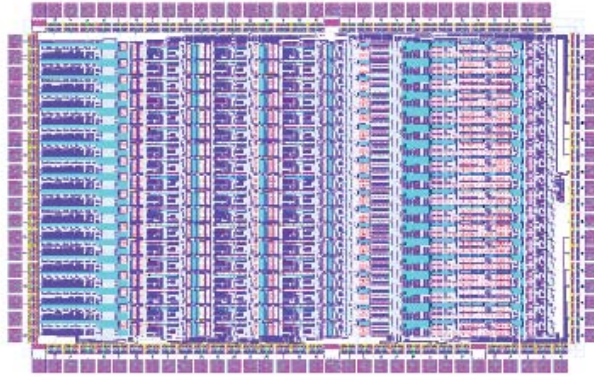


Figure 3: “flc-sipm” chip layout

ns. The noise rate is around 2MHz so a calibration is necessary on single photo-electron and must be done at fast shaping to avoid pile up.

The SiPM gain varies a lot with high voltage value (It can go up to 7% for 100mV of high voltage variation). To have quite the same gain for each SiPM, we need to adjust the high voltage from 63 to 67 V, so a DAC (digital to analog converter) is added on each channel of the chip to compensate for SiPM gain variation.

2. PHYSICS CONTEXT

In the CALICE collaboration, the HCAL prototype[2] has to be added to the ECAL physics prototype for test beam in DESY mid 2005 and going on in higher energy beam in 2006. The chip has been designed in a very tight schedule in order to be ready in time with the HCAL prototype.

2.1. SiPM electronic characterisation

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2.2. SiPM connection to the chip

The SiPM is directly connected to the chip as shown in fig. 4. The high voltage is provided by the cable shielding. There is no external circuitry except high voltage decoupling and cable matching components. The DAC comes directly at the chip input and it is necessary to filter its noise.

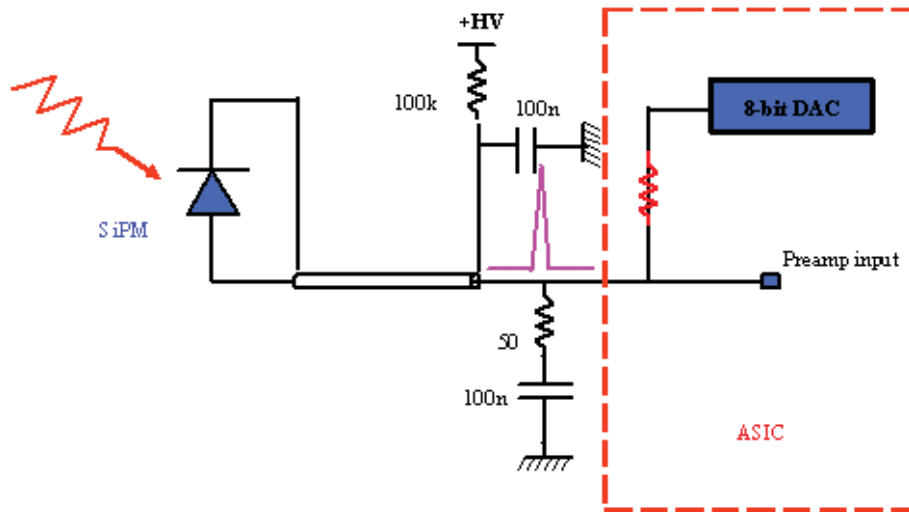


Figure 4: SiPM connection to the readout

3. CHIP DESCRIPTION

3.1. General description

The `flc_sipm` is an 18 channel charge input front-end circuit. It provides a shaped signal proportional to the input charge. The chip houses 18 channels made of a low noise variable-gain charge preamplifier followed by a CRRC2 shaper with a variable shaping time. Each of the shaper output comes into a track and hold system giving a single multiplexed output. The bias of each stage is common for 18 channels. An 8-bit DAC is in parallel to the preamplifier input.

The total power consumption of the chip is around 200mW with 5V supply voltage. The chip is designed in a 0.8 μ m CMOS technology of AMS[4] and has an area of 10 mm² (fig. 3). Around 1000 circuits have been produced at the end of 2004 and are packaged in a QFP100 case.

3.2. One channel description

The channel architecture is shown in fig. 5

At the input of each channel, there is an 8-bit DAC to provide 5V of DC voltage change, it is coupling with a capacitor at the input of the preamplifier. This capacitance is also used for high voltage decoupling and it is followed by a resistor in order to make a first derivative constant time. For speed and noise reasons, this resistor could be shorted.

A low noise charge preamplifier follows : it gives 1300 electrons of noise at fast shaping compared to the 106 electrons given by a single photo-electron. The gain of this preamplifier (feedback capacitance) can be externally chosen on 4 bits : it varies from 0.7 to 10 V/pc.

The filtering is done by a CRRC2 shaper with variable time constant which can be externally chosen on 4 bits from 12 to 180 ns. The fast shaping (called calibration mode) is used for SiPM calibration on single photo-electron and the long shaping (called physics mode) is necessary to be compatible with the ECAL readout.

3.3. DAC description

The DAC used is an 18 channel 8-bit DAC, its structure is based on scaled current mirrors. It provide 5V of excursion in order to adjust the high voltage value and then the SiPM gain. Its output comes at the preamplifier

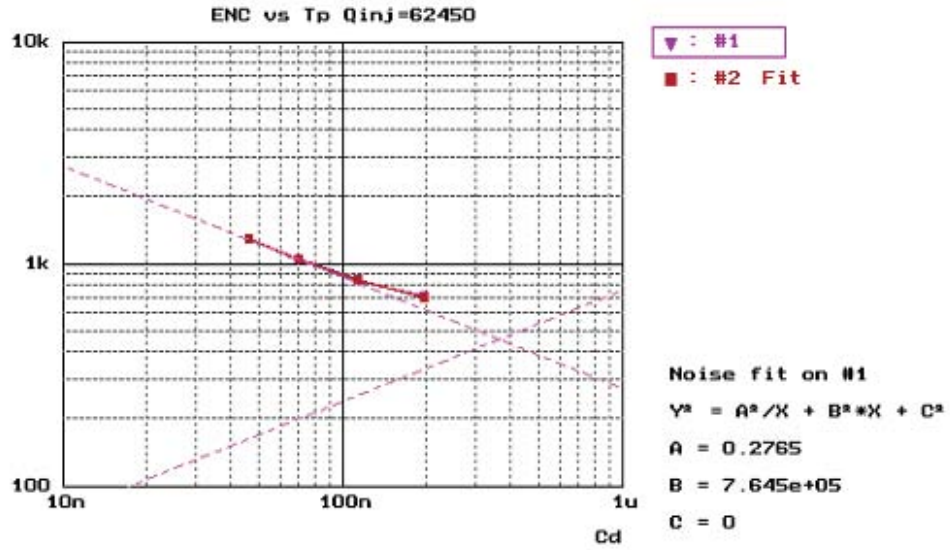


Figure 6: preamp noise

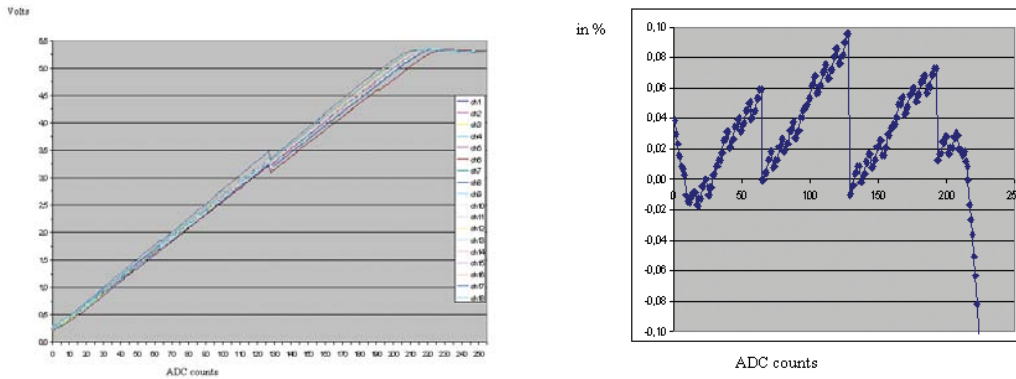


Figure 7: 18 channel DAC linearity and residuals

4.4. Physics mode

In physics mode, we take a long time constant (180 ns), a gain preamplifier of 2.5 V/pc (the feedback capacitance is 0.4pF) and the input resistor is used. In these conditions, a MIP electronically injected (without detector and with 9.5mV in 270pF) gives at the output a signal of 23mV with a peak at 160ns as shown in fig. 9.

4.5. Cross-talk considerations

The cross-talk between channels was measured and it is negligible (less than 0.2%). Fig. 11 shows output of one channel with signal at input compared to neighbour and non-neighbour outputs without signal at input and multiplied by 100.

The neighbour channel shows the capacitive coupling contribution and the non- neighbour channel shows the long distance cross-talk due to common reference voltage on chip.

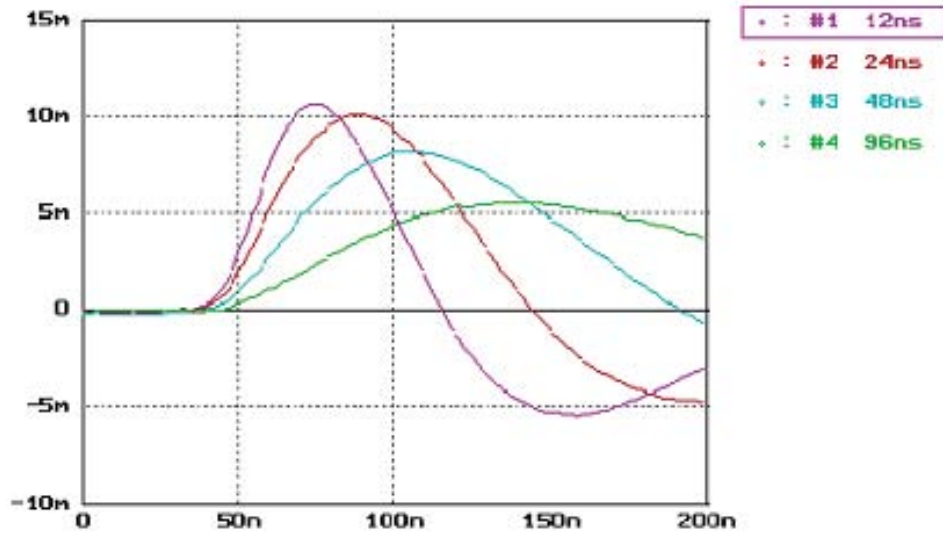


Figure 8: SPE response at various shaping time

4.6. Spectrum measurements

Connecting the SiPM to our chip we can clearly observe peaks for 1 photo-electron, 2 p.e., 3 p.e. and so on as shown in fig. 12.

5. SCHEDULE AND COST

The development of this chip was very short. The first prototype was submitted in June 2004. After test and validation of this prototype, a production of 1000 chips started in November 2004. The production was delivered in January 2005, all chips are now under test and will be available for the CALICE collaboration in April 2005.

The overall cost of this production is around 25 K (or 20 K\$), the biggest part is for silicon dies and 4 K for packages.

6. CONCLUSION

A series of 1000 chips with 18 channels each has been produced in less than one year. It is a very versatile chip with variable gain preamplifier (from 0.7 to 10 V/pc) and with variable shaping time shaper (from 12 to 180 ns).

In calibration mode, the fast shaping clearly separates single photo-electron peaks. In physics mode, the dynamic range of 11bits (1mV to 2V) fulfils the SiPM requirements and remains compatible with the ECAL readout.

An 8-bit DAC provides 5V excursion of change in high voltage value and allows to adjust the SiPM gain.

References

- [1] M. Danilov, these proceedings.
- [2] F. Sefkow, these proceedings.
- [3] E. Garutti, these proceedings.
- [4] www.austriamicrosystems.com

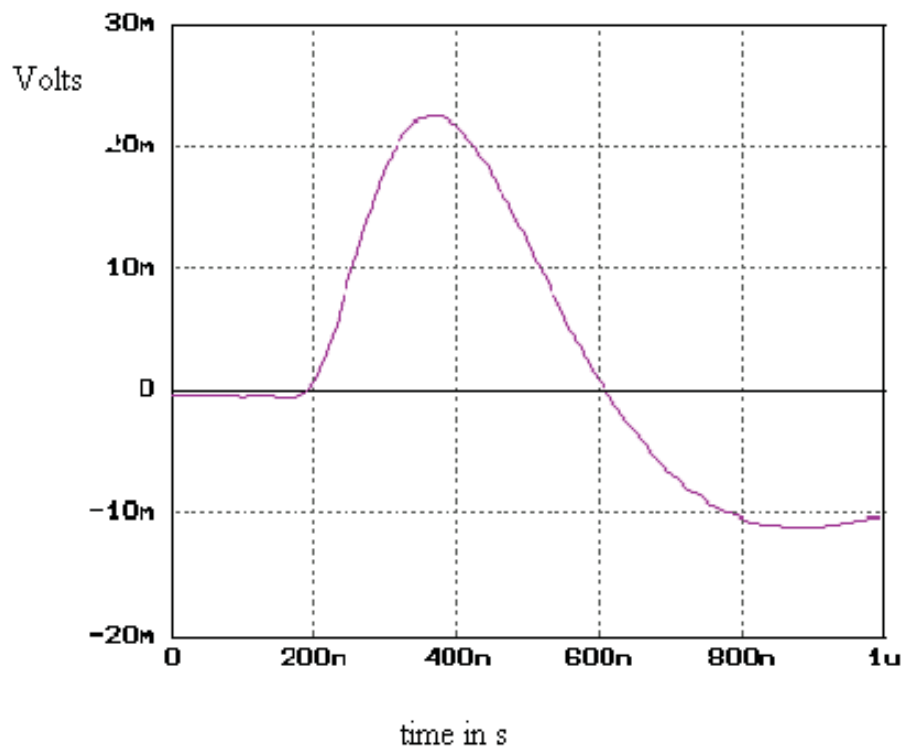


Figure 9: MIP response in physics mode conditions

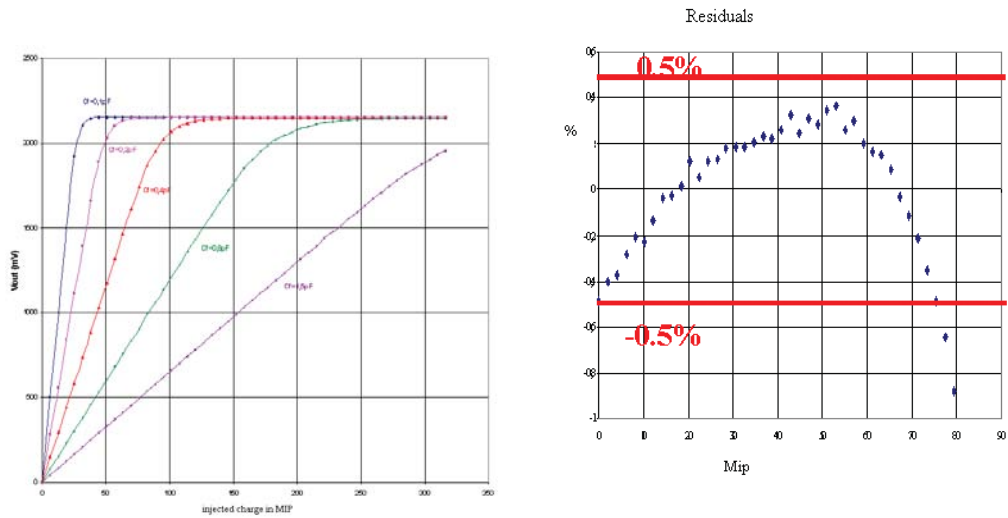


Figure 10: linearity versus MIP injection for various preamplifier gains and residuals for gain 0.4pF

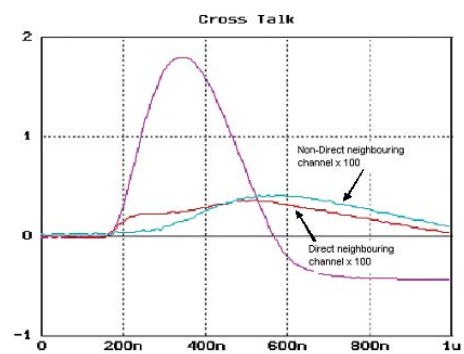


Figure 11: Cross-talk measurement in physics mode conditions

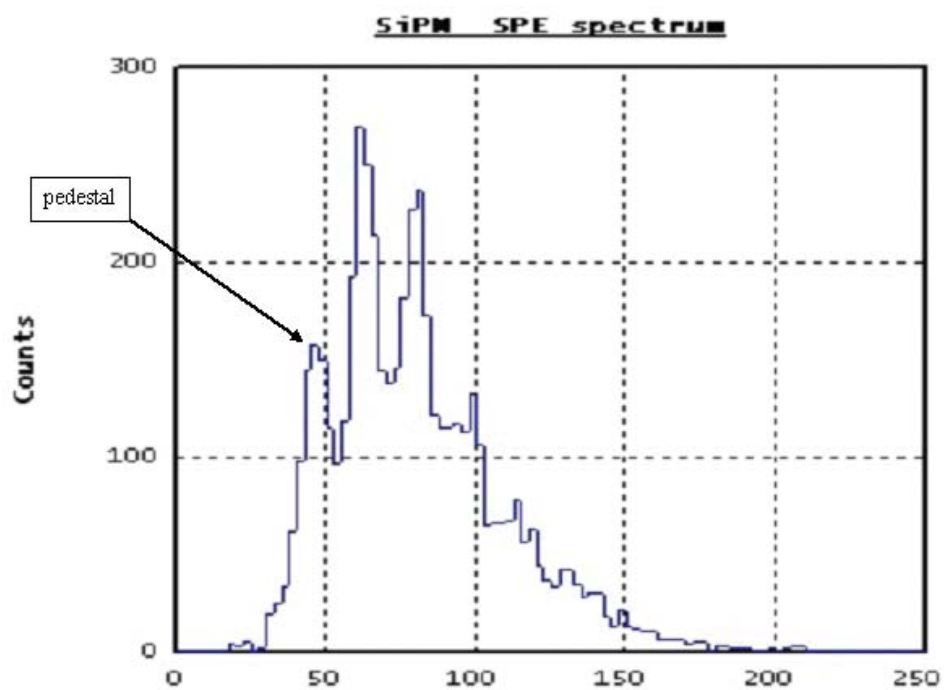


Figure 12: SPE spectrum measurement in physics mode conditions