A 16-channel Silicon Strips Readout Chip in 180nm CMOS technology

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A highly integrated readout scheme for Silicon trackers making use of Deep Sub-Micron CMOS electronics (DSM) and analog sampling techniques is presented. In the context of the International Linear Collider (ILC) tracking detectors developments, a 16-channel readout chip for Silicon strips detector has been designed in 180nm CMOS technology, each channel comprising a low noise amplifier, a pulse shaper, a sample and hold and a comparator operated at low power. Test results are presented.

1. INTRODUCTION

In any detector concept foreseen at the ILC, a front-end readout system for tracking Silicon detectors has to manage millions of channels. Consequently, the amount of material and power per channel has to be carefully optimised keeping noise and readout speed within the constraints of the experiment. It is therefore essential to look for the best integrated technologies available that allow to minimize the amount of material added to the detector, such as connexion capacitances in terms of connectors, hybrid circuits, kaptons, and lead as well to a manageable amount of dissipated power. These technologies allow also to implement efficient data extraction and signal processing techniques such as analog sampling and on-chip digitization.

For designs that covers of the order of 100 square meters and millions of channels, the multiplexing of several tasks such as analog to digital conversion and zero suppression are mandatory. The full context of this work is described in the document available from the Website: http://www.linearcollider.ca/lcws05/h/Savoy.pdf

2. FRONT-END PROCESSING

The foreseen front-end processing is sketched in Figure 1.

The Front-end signal processing chips amplify, filter, sample and digitize the input charge. For the Silicon strips charge readout two different shaping times are foreseen, typically 0.5 to 2 μ s, and 2 to 6 μ s. Besides this, a faster shaping time may be needed to measure the position along the strips. This method is presently under investigations in terms of pulse propagation velocity across the detector, and signal rise-time at the strip termination.

More precisely, in the envisioned scheme, a low noise charge integrator stores the input charge in a 400fF capacitor, giving a gain of the order of 10mV/MIP at this level, assuming 24,000 electrons are deposited in a 300 μ m thickness Silicon detector. The resulting voltage step from the preamplifier's output is filtered by a CR-RC stage whose peaking time can be tuned between 2 and 6 μ s, depending on the strip length, for accurate charge measurements and beam-crossing identification.

The Front-end electronics is designed to keep the intrinsic detector performance. Consequently, sampling the analog pulses and digitizing with sufficient frequency and amplitude accuracy has been chosen as the best data extraction technique. Digital signal processing techniques running these data should derive the best position information from the Silicon strips detectors.

Using centroid algorithms on several adjacent strips, these charge measurements would allow to extract the transverse position with an accuracy of 5-10 μ m. A faster pulse-shaper (50-100ns) would be implemented for timing measurements, in a front-end chip version dedicated to both transverse and longitudinal position along the strip, one detector layer only being equipped with this high resolution timing electronics, in addition to charge.

Simulations have shown that pulse sampled Silicon detectors are intrinsically able to provide a timing precision along the strip of the order of one nanosecond, since the pulse rise-time component due to electrons is no longer than a few nanoseconds. (Figure 2). This precision is actually strongly depending on the achieved detector's signal to noise ratio and the number of samples, and gives better results than leading edge or even constant fraction threshold in the same conditions.

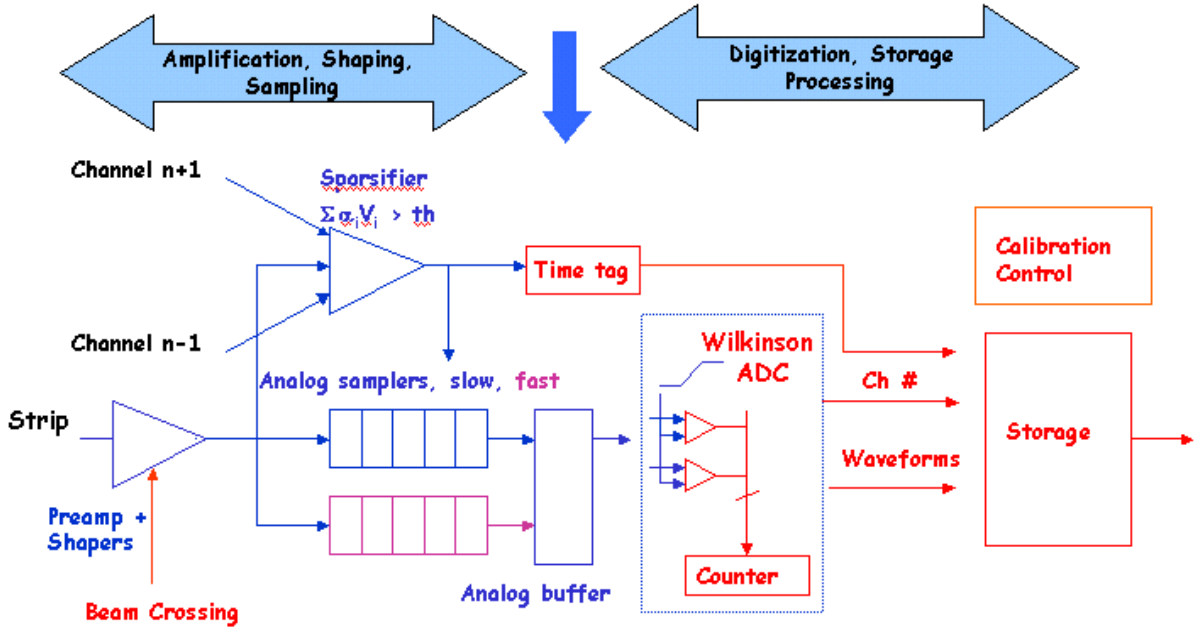

Figure 1: Front-end processing

Therefore, two analog samplers clocked every 10 and 100ns, would generate subsequent samples of the shapers outputs, to be stored in a 2D analog buffer. A depth of a few units is foreseen in both dimensions, first used to store the signal samples, second dimension used to implement a multi-event buffer in order to cope with the strips occupancy as it is presently predicted by physics simulations to be of the order of a few per cents.

In order to store only charge signals above a given threshold, an analog sum of three neighbouring channels has to be compared to a voltage level, taken at the output of the slow shapers where most of the noise is removed, for each channel. This sparsification decision freezes the analog samplers, and selects an available set of two buffers for the next pulse to come.

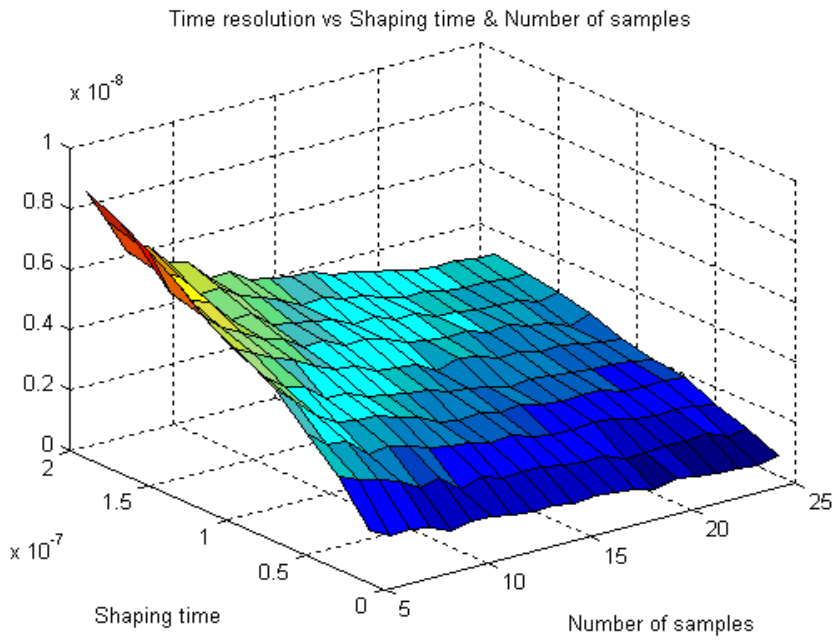

Figure 2. Simulated time resolution as a function of the shaping time and number of samples, at 25 Signal to Noise ratio.

This process runs for the total duration of an ILC train, of the order of one millisecond. At the end of the train, digitization can take place. In order to minimize power, a ramp ADC is foreseen, allowing to convert in parallel as many channels as process gradients through the chip allow, the cost in power per channel being one comparator stage. Such an analog to digital operation may take a few microseconds in total, depending on the number of bits of the conversion, negligible compared to the total cycling time of the ILC machine.

3. TEST CHIP

A test chip has been designed in a 180nm CMOS technology by United Microelectronics Corporation (Taiwan) available at multiproject cost through Europractice (Leuven, Belgium). It includes 16-channels comprising a low-noise preamplifier, a pulse shaper, a sample and hold, a voltage buffer and a comparator. A single test channel allows to check all blocks reachable through six I/O pads. All stages have bias controls allowing to adjust the biaising point to a given value.

3.1 PROCESS

A single test channel allows to check all blocks reachable through six I/O pads. All stages have bias controls allowing to adjust the biasing point to a given value. Ten chips have been tested, the spreads on preamplifier gains and power are shown Figure 2 and 3. The process spreads are of the order of 3%, showing that the technology is well under control. Only one transistor was founded faulty, on the ten chips tested.

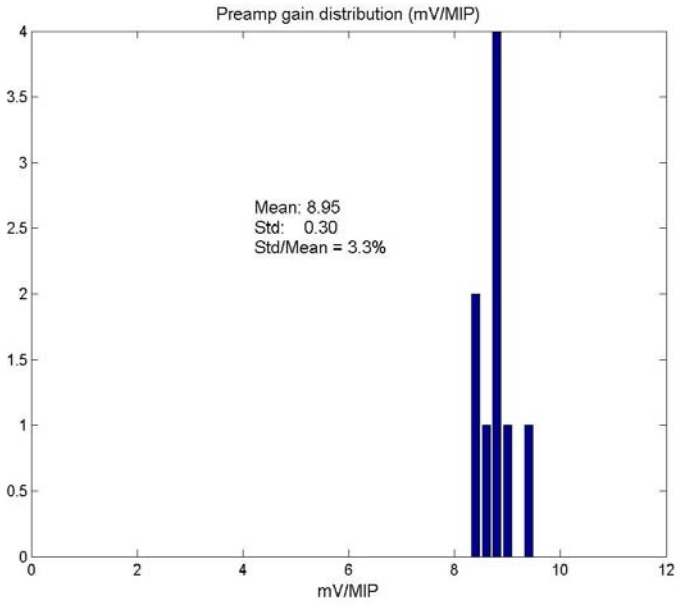

Figure 2. Process spreads: Preamplifier Gains

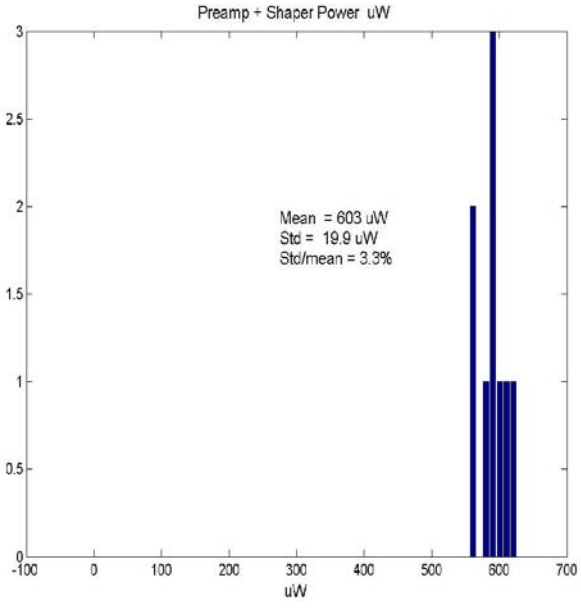

Figure 3. Process spreads: Power

3.2 IMPLEMENTATION AND RESULTS

The low-noise preamplifier (Figure 4) is a folded cascode stage with a PMOS input transistor biased under 40 μ A, in weak inversion, the inversion coefficient being 0.06. The corresponding transconductance is 0.69mA. Simulated thermal noise spectral density for this transistor is 4nV/$\sqrt{Hz}$, using both BSIM3v3 noise models based on channel conductance and stored charge. The simulated open loop gain is 70dB, including the other noise contributions, the simulated noise from this stage being 485 + 16.5e-/pF.

The drain is tied to ground at half the supply voltage, setting the DC point around -0.5V. The 400fF feedback capacitor can be reset (or discharged with a given time constant) using a NMOS transistor controlled through an external voltage. The voltage gain of this stage is therefore 8mV/MIP.

The pulse shaper (Figure 5) is an active CR-RC network using the same folded cascode structure as above, buffered with a source follower in order to drive the 600 fF sample and hold capacitor. Two analog controls allow to tune the peaking time in the microsecond range. The simulated noise is 285 + 8.9 e-/pF at this level.

Gain and Dynamic range

The measured gain of 8mV/MIP is in agreement with the simulations. Dynamic range is 70 MIPS for the amplifier and 50 MIPS for the shaper, instead of 100 MIPS and 60 MIPS as simulated. In addition, the deviation from linearity from the preamplifier is 1.5% instead of 0.5% simulated, and 5% for the shaper, for low amplitudes values. These two discrepancies are understood as non-linear behaviours of the cascode stages operating in weak inversion where the models may not be as accurate as in the high current biaising operations.

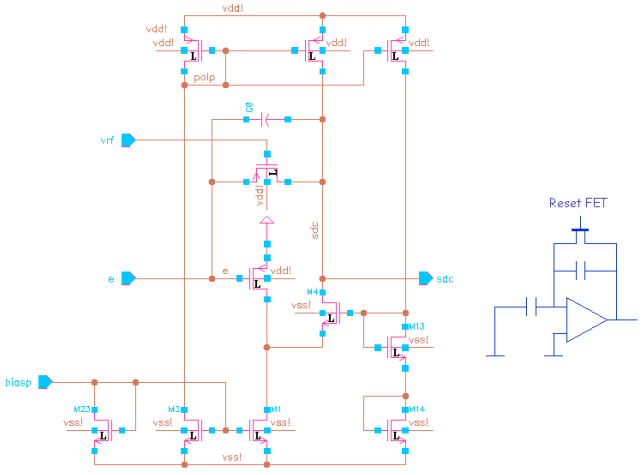

Figure 4: Preamplifier schematics and block-diagram

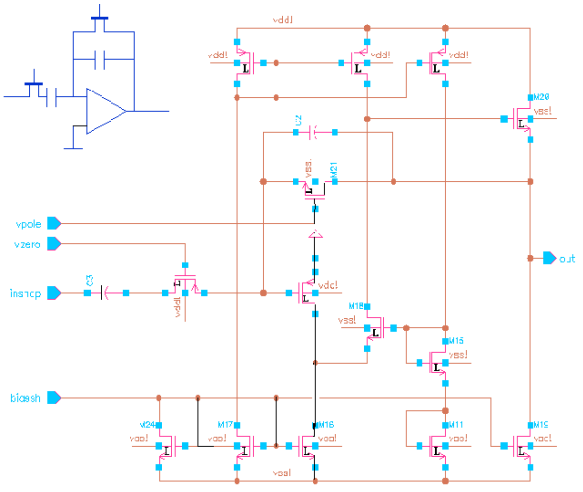

Figure 5: Shaper schematics and block-diagram

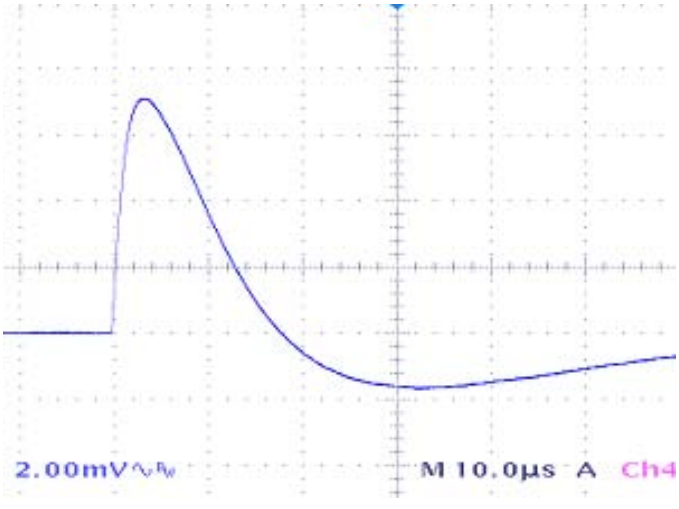

Figure 6. Pulse Shaper response.

Noise

At 60 μW input stage power, 30pF detector capacitance, 3 μs shaping time, the various contributions to the detector and front-end electronics noise are summarized in Table 1.

The pulse shaper response is shown Figure 6 . The electronics noise comes mainly from the low-noise preamplifier input stage (Figure 8). The measured noise is 498 + 16.5e-/pF, as simulated. The measured noise from the shaper is 375 +10.1 e-/pF, instead of 285 + 8.9 e-/pF simulated, due to a small bump in the frequency response around 6 MHz as shown in Figure 8, that can be easily removed in a future version. Tests using a chip on board implementation have reduced this noise contribution by 530 e- from the 650 + 10.1 e-/pF initial measurements.

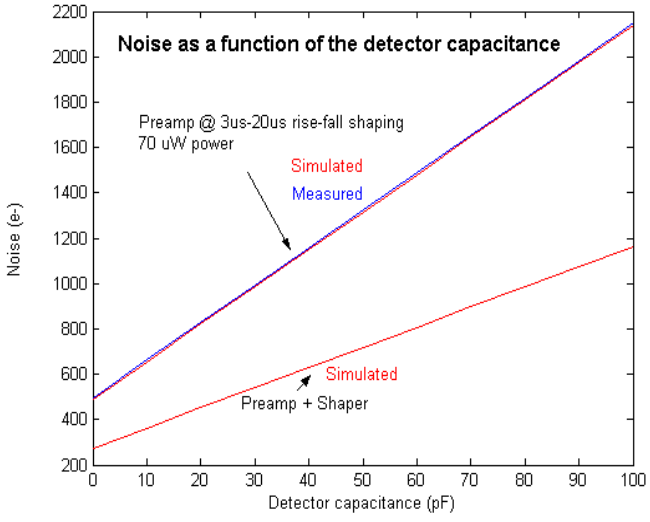

Figure 7 . Preamplifier Noise as a function of the detector capacitance.

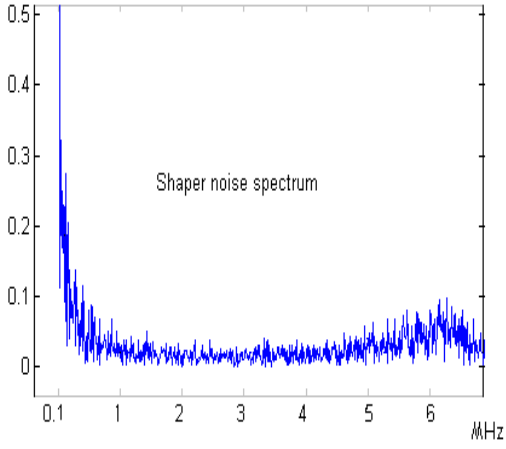

Figure 8. Output noise measured spectral density

At 70 μ W input stage power, 30pF detector capacitance, 3 μ s shaping time, the various contributions to the detector and front-end electronics noise are summarized in Table 1

Table I: Foreseen detector noise contributions at 30 pF detector capacitance and 3 μ s shaping time.

Source	Value	Noise
Electronics	g_m=0.69mA/V	690 e-
Detector leak	10 nA	588 e-
Biasing resistors	10 MΩ	423 e-
Total		1000 e-

According to the noise models from the manufacturer, no 1/f noise should show-up in 180nm CMOS technology, even at 10 μ s shaping time. If this were the case, Silicon-Germanium technology could be an effective alternative both for low frequency noise reduction and speed performance having in view the timing measurements.

The 70 μ W power dissipated in the preamplifier is due mainly to the input transistor biasing, in order to obtain a sufficient gain. It dictates the noise performance of the stage. In case of lower noise requirements, particularly for long strips, an increase of power could be envisaged, leading for instance to lower noise slopes below 8e-/pF.

3.3 POWER

In order to take advantage of the ILC machine timing, all electronic stages running during the collisions only could be switched off for the readout stage. Therefore, a factor 100-200 can be saved at this level. This process has been simulated to be effective with the present front-end electronics provided the integration capacitor is reset before power-off and after power-on.

An open question is to know whether a small fraction of the static current should be kept during the sleeping stage, or if the charges stored after the reset of the feedback capacitance are able to maintain the biasings for 2 ms, when all supply currents are switched off. This scheme is effective in simulations, and needs to be tested in a next chip version.

4. CONCLUSION AND FUTURE WORK

These results regarding the integration of a front-end electronics for Silicon detectors in Deep Sub-Micron CMOS technology will be pursued by tests with an actual Silicon detector equipped with bare chips detector and MIP signals on a test bench, and compared with other front-end chips off the shelf. A 128-channels version that include fast and slow shapers, the sparsifier stage, analog samplers and a full ADC, digital section including possibly digital filtering and lossless data compression, power switching, is under design in CMOS 130nm technology and will take benefits from this prototyping work.

Acknowledgments

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