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Performance of a Fast Binary Readout CMOS Active Pixel Sensor Chip Designed for Charged Particle Detection

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Abstract—We report on the performance of the MIMOSA8 (HiMAPS1) chip. The chip is a 128×32 pixels array where 24 columns have discriminated binary outputs and eight columns analog test outputs. Offset correction techniques are used extensively in this chip to overcome process related mismatches. The array is divided in four blocks of pixels with different conversion factors and is controlled by a serially programmable sequencer. MIMOSA8 is a representative of the CMOS sensors development option considered as a promising candidate for the Vertex Detector of the future International Linear Collider (ILC). The readout technique, implemented on the chip, combines high spatial resolution capabilities with high processing readout speed. Data acquisition, providing control of the chip and signal buffering and linked to a VME system, was made on the eight analog outputs. Analog data, without and with a ^{55}Fe X-ray source, were acquired and processed using off-line analysis software. From the reconstruction of pixel clusters, built around a central pixel, we deduce that the charge spread is limited to the closest 25 pixels and almost all the available charge is collected. The position of the total charge collection peak (and subsequently the charge-to-voltage conversion factor) stays unaffected when the clock frequency is increased even up to 150 MHz (13.6 μs readout time per frame). The discriminators, placed in the readout chain, have proved to be fully functional. Beam tests have been made with high energy electrons at DESY (Germany) to study detection efficiency. The results prove that MIMOSA8 is the first and fastest successful monolithic active pixel sensor with on-chip signal discrimination for detection of MIPs.

Index Terms—Active pixel sensor, charged particle detector, CMOS sensor, discriminator, MAPS, vertex detector.

I. INTRODUCTION

DEVELOPMENTS in future high energy physics will include the construction of an e+e- international linear collider (ILC) [1]. This machine together with adequate detectors

will allow precision, model independent measurements at sufficiently high energy and luminosity. Higgs and fundamental interaction studies may be done with this machine, with a reduced background compared to the LHC experiments [2]. Thus, this machine should be a priority for the next decades of particle physics research.

Precision vertex measurements will be mandatory for the detectors of the ILC. This makes the design of vertex detectors a challenge in terms of number of pixels, high readout speed, spatial resolution, and power dissipation.

The future vertex detector should offer a better spatial resolution than present day vertex detectors based on Hybrid Pixel Detectors, and should be faster than charge-coupled diodes (CCDs). The aim of the monolithic active pixel sensor (MAPS) development program is to obtain spatial resolution roughly equal to 1–2 μm , with a readout time for each frame below 20 μs . This will involve very small pixels (20 μm pitch for the first layer) and thinning the silicon substrate to reduce multiple scattering.

MAPS have the competitive edge over CCDs for radiation tolerance, mainly because they are based on random access of each pixel avoiding charge transfer. The electric charge is converted into an electric signal *in situ* on the photodiode of each pixel, all of them containing an amplifying element. MAPS technology is a serious candidate for the first and second detection layers of the future vertex detector of the ILC.

II. DESIGN AND ARCHITECTURE OF THE MIMOSA8 CHIP

The MIMOSA8¹ (or HiMAPS1²) device (Fig. 1) characterized here is a monolithic chip comprising a 128×32 pixels array, a serially programmable sequencer and 24 binary outputs. The outputs are discriminated with a common adjustable threshold and time multiplexed. The eight remaining outputs are analog. In a move to meet speed requirements the 32 columns are read in parallel, using an external clock. The chip is divided in subarrays with four types of small pixels that have different conversion factors (S1: 110 $\mu\text{V}/e^-$, S2: 66 $\mu\text{V}/e^-$, S3: 60 $\mu\text{V}/e^-$, S4: 50 $\mu\text{V}/e^-$). The pixel pitch is 25 $\mu\text{m} \times 25 \mu\text{m}$ for all subarrays. The amplifier gain is also the same for S2, S3, and S4. Otherwise the diode sizes are different: 4.1 $\mu\text{m} \times 2.5 \mu\text{m}$ for S1, 1.2 $\mu\text{m} \times 1.2 \mu\text{m}$ for S2, 1.7 $\mu\text{m} \times 1.7$

¹Minimum Ionizing particle MOS Active pixel sensor.

²High-speed Monolithic Active Pixel Sensor

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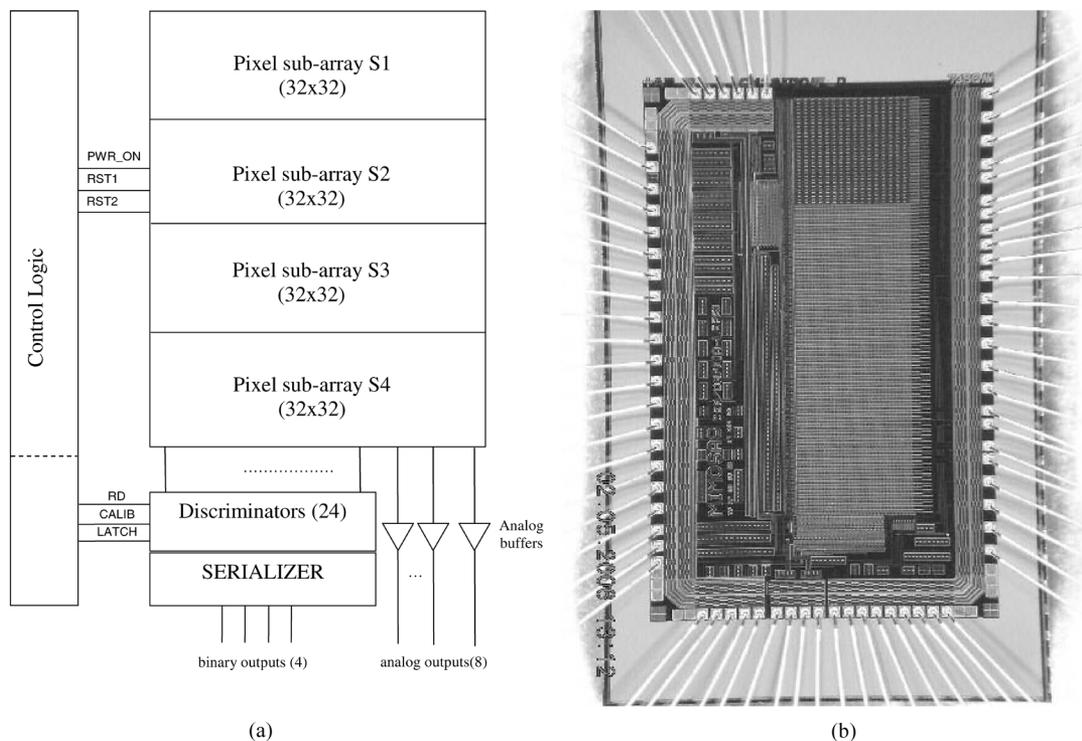


Fig. 1. (a) Block diagram, and (b) photography of the realized prototype chip.

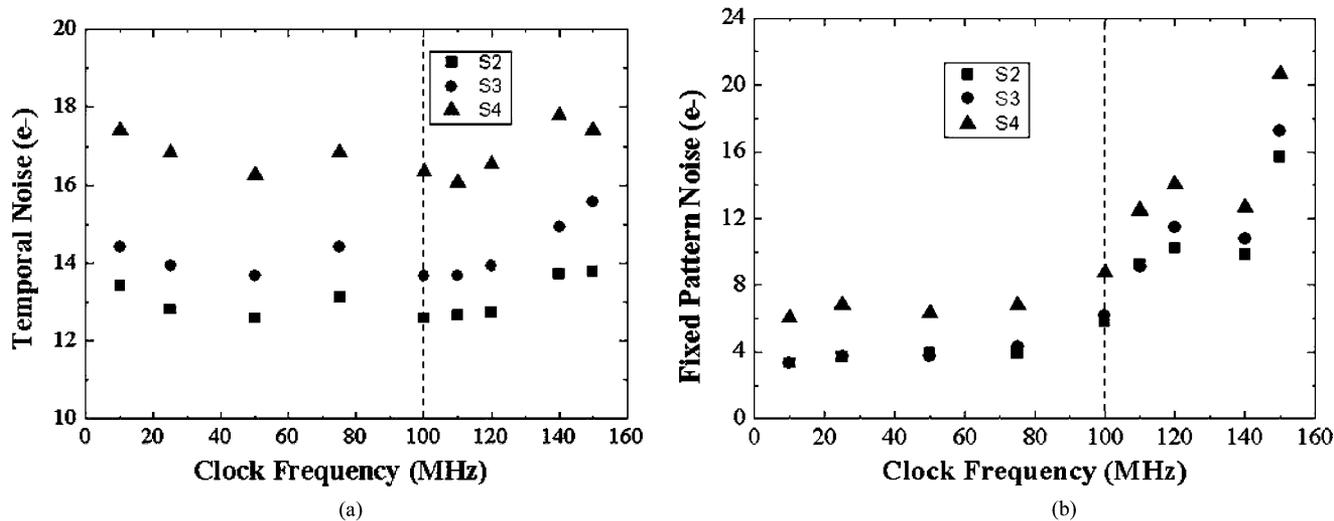


Fig. 2. (a) Temporal noise. (b) FPN versus clock frequency for the three subarrays.

μm for S3, and $2.4 \mu\text{m} \times 2.4 \mu\text{m}$ for S4. Offset correction techniques are used extensively in this chip to overcome process related mismatches. For further details on the architecture of this chip see our previous work [4]. The MIMOSA8 was fabricated with TSMC $0.25 \mu\text{m}$ CMOS digital technology with a thin epitaxial layer. In order to reduce power consumption the power supply of the pixels in a row is only switched on for the row that is being read. The chip is readout in continuous rolling mode, so no external trigger is used.

The new aspects of the pixel have already been described in [4]. To summarize: in pixel voltage amplification has been successfully implemented together with local Correlated

Double Sampling (CDS) based on a concept familiar to CCD designers [5], this being based on one capacitor and a few transistor switches. The CDS suppresses the reset noise and offset nonuniformities of transistors. This scheme proved to be successful up to now and has allowed some good preliminary measurement results [4]. The readout of each row is based on a scheme requiring 16 clock cycles, with a designed optimal clock frequency of 100 MHz. The clocking chronogram is used for both the pixel and the discriminator.

The analog outputs are used to study the pixels individually, and to characterize their pedestal, temporal noise and their charge collection efficiency. The digital outputs have been used

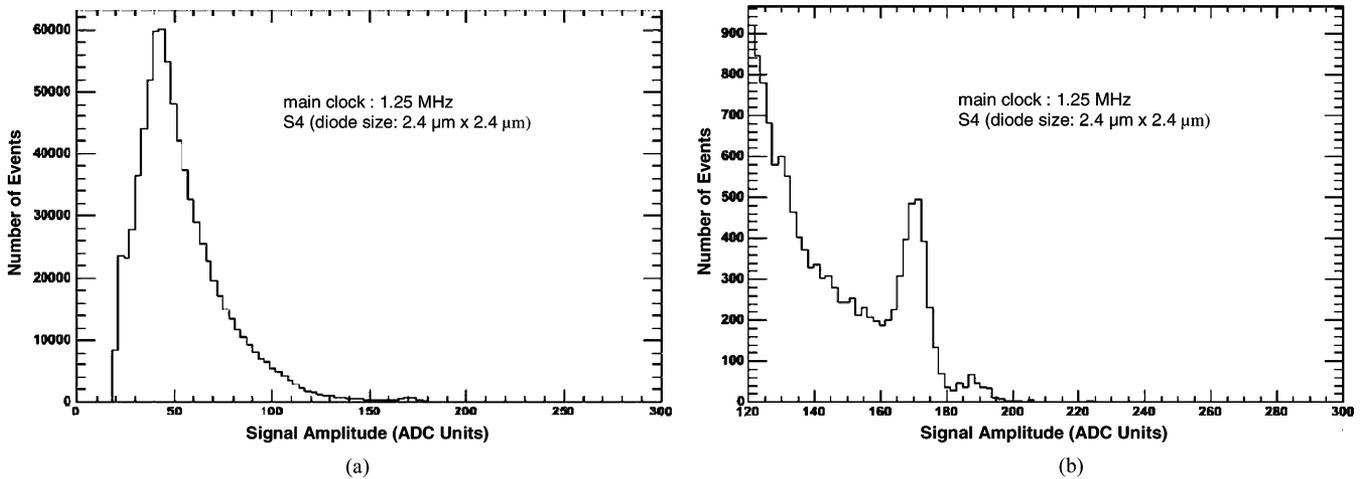


Fig. 3. Histogram of the events recorded on single pixels (no clusters) at a clock frequency of 1.25 MHz with a ^{55}Fe X ray Source. (a) Total spectrum. (b) Truncated spectrum (S4 subarray). The calibration peak is clearly observed in (b).

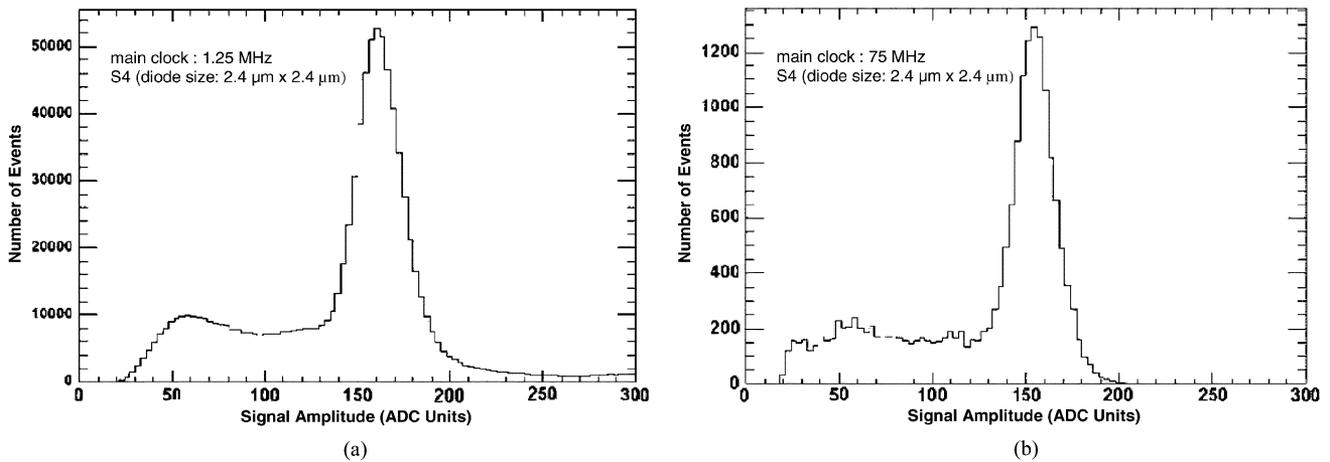


Fig. 4. Total charge collection peak for the largest diode size at different frequencies. (a) 1.25 MHz. (b) 75 MHz. Clusters of 25 pixels have been used.

to characterize the full one-bit digital chain and to evaluate the discrimination efficiency. Up to now, the comparators have been tested thoroughly, these auto-zero circuits being very effective in reducing offset dispersion [6].

The chip is optimized for low power operation. The total power dissipation of the analog part (pixel+discriminator) is given by: $430 \mu\text{W} \times \text{number of columns}$.

III. MEASUREMENT RESULTS

The results of the extended tests done on the pixel array with and without exposure to a ^{55}Fe X ray source (energy peaks: 5.9 and 6.4 keV) are presented here. The acquisition of data was done with a VME system analog-to-digital conversion cards that record the analog outputs of the array. The chip was linked to DAQ by two dedicated boards designed to control the chip and to provide signal buffering for transmission. Data obtained were analyzed off-line using dedicated software. The data were taken and analyses carried out, first without source, to determine pedestals' dispersion [spatial noise or Fixed Pattern Noise

(FPN)] and their distribution on the chip to measure the (temporal) noise level³. In a second step, data from the analog and digital outputs were taken with the source on. The S1 subarray based on an architecture, different from the other arrays, was not characterized here.

Although the chip was optimized to work at 100 MHz clock frequency, it is important to check the functionalities of the chip at lower frequency. For example, very high leakage currents were observed on the diodes of the subarray S1 (which is different from S2, S3, and S4) at a few MHz. For this reason, we started the measurements at low frequencies and increased step-by-step the clock frequency up to the limits of the VME-based data acquisition system.

A. Analog Data on Single Pixels

Fig. 2(a) indicates that the temporal noise remains stable up to 100 MHz clock frequency. The FPN behaves similarly with a sharp increase above 100 MHz Fig. 2(b). This is satisfactory as the chip was optimized for 100 MHz clocking.

³Large number of events was acquired without source, then the rms values (temporal noise) and dispersions of mean values (FPN) are calculated for each pixel.

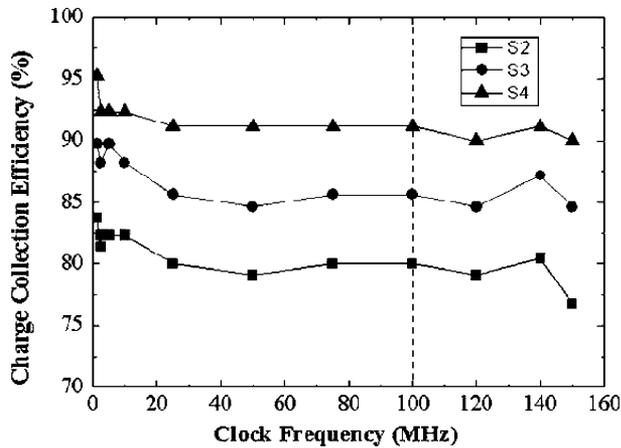


Fig. 5. Percentage of charge collected versus clock frequency for the three subarrays of pixels. Clusters of 25 pixels were used.

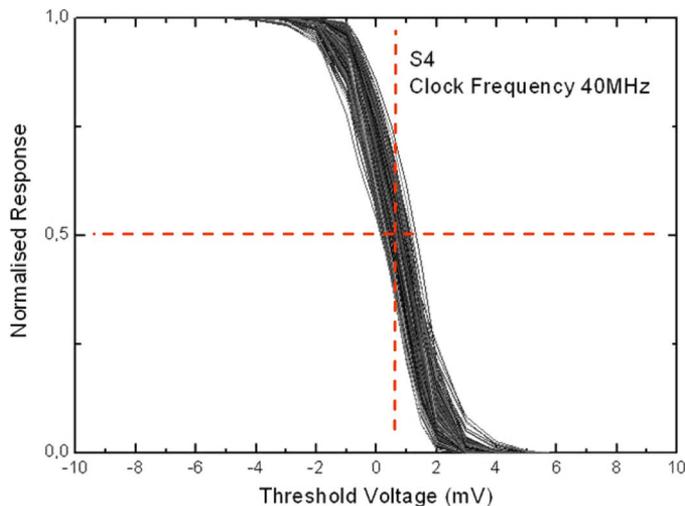


Fig. 6. Number of counts (normalized) versus discriminator threshold voltage. The offset and the temporal noise of the pixel/discriminator chain can be derived. Each curve corresponds to one pixel associated to a column discriminator. The offset dispersion can also be estimated. The clock frequency is 40 MHz.

The eight columns with analog outputs underwent tests with a ^{55}Fe 10 mCi source. Fig. 3 shows the signal corresponding to single pixels. For all spectra, a cut at low energy has been made to reduce the influence of temporal noise. The calibration peak of the source is clearly observed in Fig. 3(b) ($\sim 1600e^- = 170$ ADC Units), but corresponds to relatively rare events, when photons deposit all their energy directly on one diode or very close to it. This is the reason why the calibration peak has a low amplitude. As calibration events are rare, a low clock frequency is needed to obtain a clear peak. The dominant broad peak Fig. 3(a) which appears in the spectrum is due to events generating a charge between several diodes. This is the most probable case. The charge is shared on two or more pixels, inducing events of lower magnitude. The charge is predominantly generated in the epi-layer. The charges generated in the heavily doped bulk are lost.

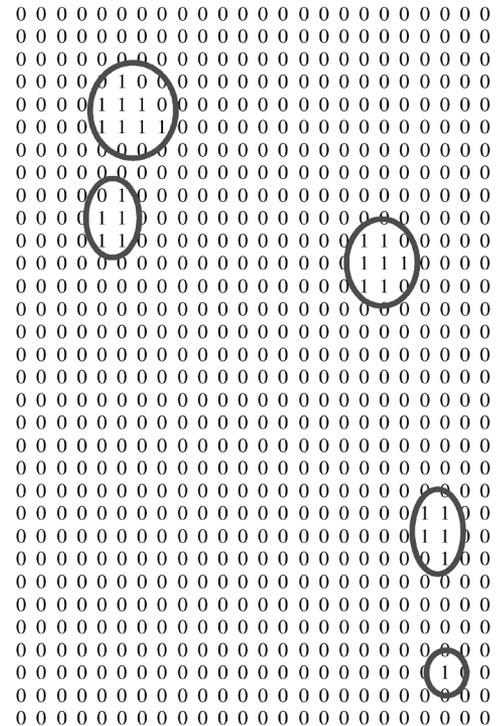


Fig. 7. Example for a subarray of pixels with the digital values of their outputs (1: pixel hit, 0: no hit). This data was recorded with the X ray source on. Clusters of hits distinctly appear. The clock frequency is 7.5 MHz.

B. Clusterization Method: 3×3 Pixels and 5×5 Pixels

In order to study the charge distribution, pixel clusters were analyzed. The software analysis allows studying different cluster sizes (3×3 or 5×5) built around the central pixel. This analysis shows that the charge spread is limited to the closest 25 pixels and almost all the available charge is collected using a lower limit threshold of 5σ on measured signals (the value of σ represents the temporal noise). Fig. 4 shows the *total charge collection peak* for clusters of 5×5 pixels in the S4 subarray. The charge collection efficiency (CCE) is defined here as the ratio of the position of the total charge collection peak to the calibration peak. It varies from 83% for S2 subarray up to 95% for S4 subarray at the same clock frequency of 1.25 MHz (Fig. 5).

The MIMOSA8 design was originally made to ensure functionality at 100 MHz of the main clock frequency. The measured total charge collection peak remains almost unaffected by clock frequencies (Fig. 5) up to 140 MHz for 25 pixels clusters. The decrease of the CCE at high frequencies is due to the limits of the chip and the data acquisition board; while the increase at low frequencies may be attributed to the pixels being hit twice during one integration cycle. There should be subsequently no change in the conversion factor and the charge collection efficiency up to a 140 MHz clock frequency. The CCE varies only with diode sizes (S2, S3, S4). The CCE is higher for bigger diodes, because more charge is collected.

C. Digital Outputs: Comparison With Analog Data

In a second part of the in-lab tests, the one bit digital outputs were tested, in order to assess their functionality. Tests were carried out without and with source.

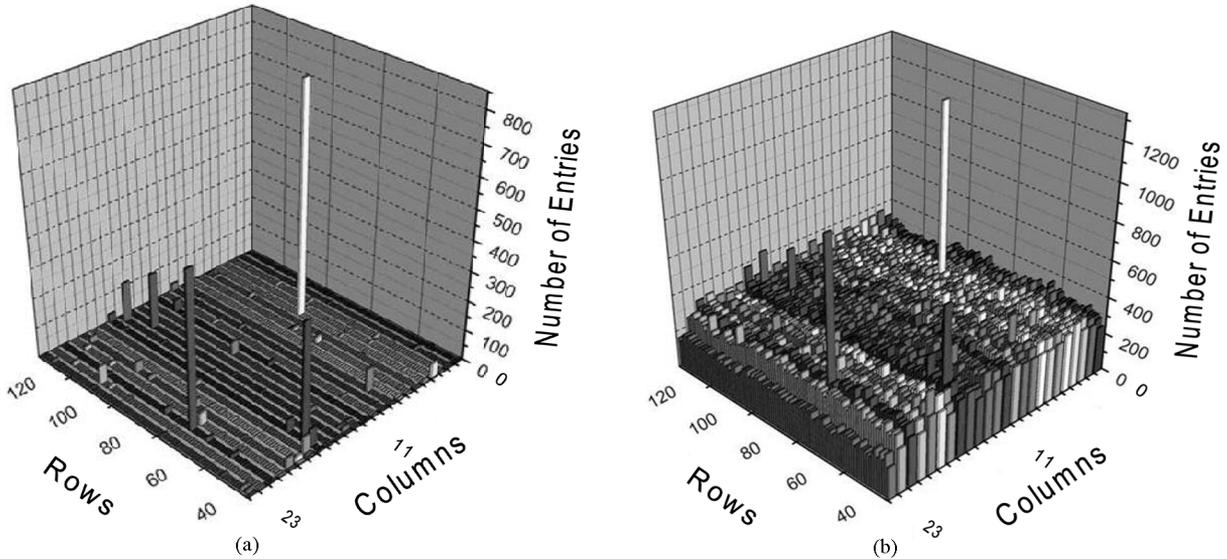


Fig. 8. Histogram (number of hits for each pixel) for the array. (a) Without the source. (b) With the source. The conditions are: clock frequency: 7.5 MHz, effective threshold voltage of the discriminators (after correction of systematic offset) is $\sim 110e^-$. The same number of events was recorded in each case.

First, the residual offset distribution of the test discriminators has been evaluated for different chips. The maximum dispersion between discriminators has a value below $0.3 \text{ mV}_{\text{rms}}$.

Second, the offset distribution of whole readout chain (pixel together with the discriminator) on a single chip was analyzed (Fig. 6). This was done for S2, S3, S4 subarrays. The systematic offset is 1 mV at 40 MHz. Measurements of temporal noise give a value of $0.9 \text{ mV}_{\text{rms}}$ and a fixed pattern noise of $0.3 \text{ mV}_{\text{rms}}$.

Note that the signal height for ^{55}Fe photons is given by $(\sim \text{CVF} \times 1600e^-)$. For example, for S4, the signal height is $(50 \mu\text{V}/e^-) \times 1600e^- = 80 \text{ mV}$.

The analysis of the digital outputs (24 columns) with X-ray exposure leads to an array of 1 s (hits) and 0 s (no hits) as represented in Fig. 7, for a single frame. Note that noise can induce nonphysical hits. Increasing the discriminator common threshold can limit the influence of noise. Cluster of 1 s are present and may be used for hit position determination. In this case discrimination is equivalent to one-bit analog to digital conversion.

In Fig. 8 the threshold was set to a high enough value to cut the spurious hits due to noise. In spite of this in (a), some pixels present much higher pedestals and noise than the others. For a given threshold, a few pixels can exceed the threshold value. However the number of these pixels remains very low. Fig. 8(b) shows that the discrimination is functional for this chip.

D. Minimum Ionizing Particles: Preliminary Beam Tests Results

The response of the MIMOSA8 chip to minimum ionizing particle (MIP) traversing the CMOS sensor was studied using a 5 GeV/c electron beam at DESY (Hamburg, Germany). For these tests, pixel detectors were mounted inside a high precision beam telescope. A small scintillation counter adapted to match the physical dimension of the tested device was delivering a trigger.

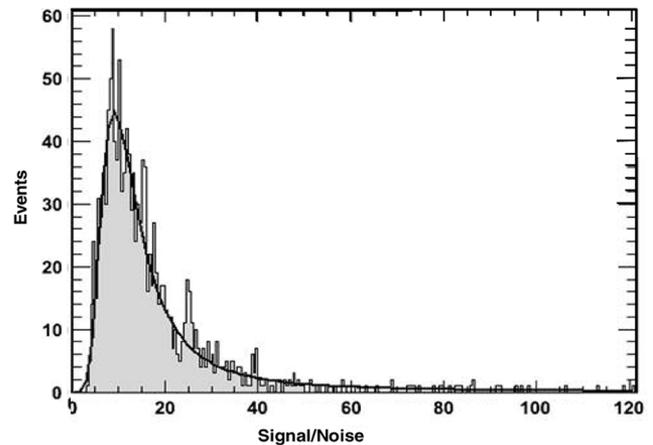


Fig. 9. Seed pixel S/N distribution.

Both analog and binary outputs were tested. The VME based data acquisition system allowed main clock frequencies up to only 40 MHz. Data analysis process was based on C++ and the ROOT framework.

While the use of a high precision telescope (a few $\mu\text{m}/\text{plane}$) allows in principle the measure of the intrinsic spatial resolution, the multiple scattering of 5 GeV/c electrons significantly degrades this resolution. Thus, the tests were limited to the determination of the detection efficiency, defined as the proportion of events which have a reconstructed hit in MIMOSA8 close to the track extrapolation of the telescope.

The individual pixel noise, defined as a fluctuation of the signal (after CDS processing) around its pedestal value, was found to be between 11 and 14 electrons, compatible with laboratory's measurements, for the three tested subarrays. Fig. 9 displays the signal-to-noise ratio (S/N) for the central pixel of a cluster for minimum ionizing particles (seed pixel). This ratio peaks around 10 [Most Probable Value (MPV)] which is a very

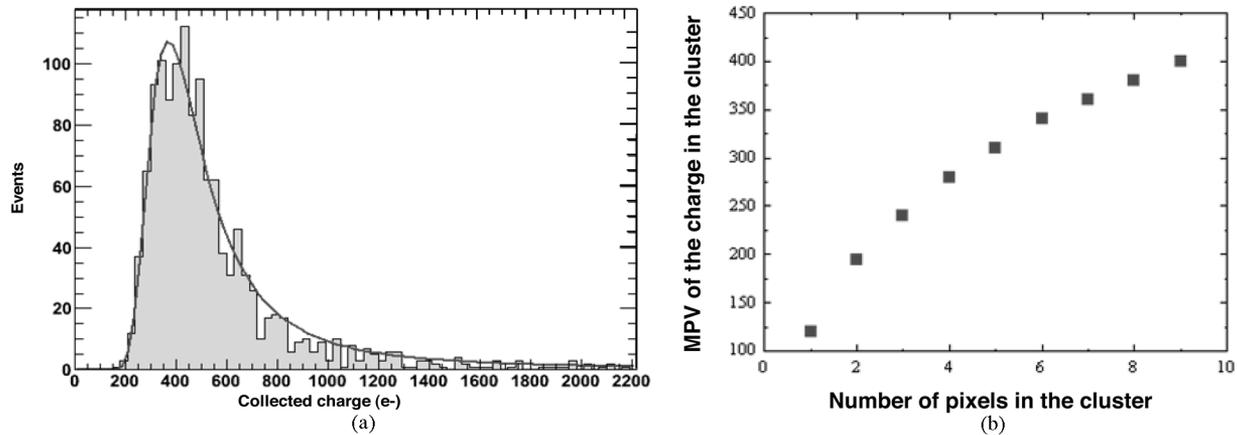


Fig. 10. (a) Distribution of the collected charge (in electrons) for pixel clusters of 9 pixels (MPV = 387.8). (b) Total charge (most probable value) (in electrons) as a function of the number of pixels in the cluster.

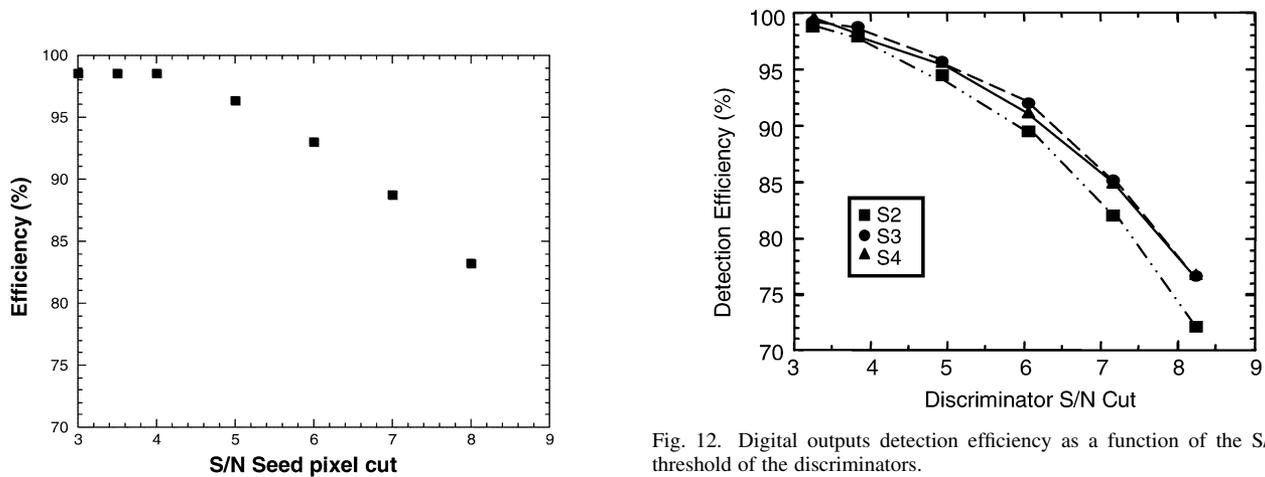


Fig. 11. Analog outputs: detection efficiency plotted versus S/N cut value at the seed pixel.

encouraging result for such a limited thickness of the epitaxial layer ($<6 \mu\text{m}$) in this fabrication process.

Concerning the analog outputs, the seed pixel was identified by requesting an individual signal to noise ratio above three and taking the pixel with the highest signal value within a cluster of neighboring pixels. The variation of the collected charge as a function of the cluster size is plotted in Fig. 10(b). Pixels were successively added to the cluster in decreasing order of their signal amplitudes. It seems that a cluster of nine pixels collects almost all the charge deposited by the particle. Indeed, no significant gain in the collected charge may be made by increasing the size of the cluster, while this increase results in a drastic drop in statistics due to the fact that there are only 8 columns for that analog part.

Very encouraging results have been obtained for the detection efficiency of all subarrays. Present analysis show that the detection efficiency of the S3 subarray attains 98% depending on the S/N cut made on the seed pixel (Fig. 11).

The digital outputs have also been characterized. Fig. 12 shows the detection efficiency versus discriminator S/N real

threshold⁴. From this figure, it is clear that a low discriminator threshold is necessary to keep high detection efficiency ($\sim 99\%$). But the fake hit rate (the probability of the hits caused by noise) increases in that case. A study shows that the value is about 10^{-3} when S/N real threshold is ~ 3.2 and that it decreases below to 5×10^{-5} when the threshold value is bigger than 4.5. [8].

The present beam tests have proved that MIMOSA8 chip has good detection characteristics.

IV. CONCLUSION AND PROSPECTS

The results obtained show that the MIMOSA8 (HiMAPS1) chip is the first successful prototype of a fast CMOS pixel detector suitable for the inner part of the μ Vertex ILC detector. Future designs will be based on its analog and digital architecture. Tolerance to fast neutrons is also under study. These results will allow us to determine how the charge collection efficiency is affected by the displacement damage and how to possibly reduce this sensitivity. In a near future column, analog-to-digital conversion could be implemented in order to optimize spatial resolution by improved computation.

⁴The mean systematic offset value of the discriminators is removed here ($\sim 0.6 \text{ mV}$ from Fig. 6).

MIMOSA8 shows that a big step forward in development of MAPS detectors used in high-energy physics experiments is the integration of a high precision and fast circuitry for column parallel processing of signals, together with in pixel signal amplifying and processing.

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