An ultra-low voltage high gain operational transconductance amplifier for biomedical applications

F. Bautista, S.O. Martınez, G. Dieck, O. Rossetto

An ultra-low voltage high gain operational transconductance amplifier for biomedical applications

Farid Bautista*, Sergio O. Martínez*,Graciano Dieck* and Olivier Rossetto†
*Electrical and Computer Engineering
Instituto Tecnológico y de Estudios Superiores de Monterrey, Monterrey México
Email: {farid, smart, graciano.dieck.assad}@itesm.mx
†Université Joseph Fourier, LPSC, Grenoble France
Email: rossetto@lpsc.in2p3.fr

***Abstract*—A novel differential-input single-output Operational Transconductance Amplifier (OTA) is presented in this paper. The topology proposed consists of an input stage based on a folded cascoded amplifier, and an output stage based on a current source amplifier and a bulk-driven current mirror. The simulations show that the amplifier has a 1.94μW power dissipation, 92dB open-loop DC gain, a unit gain-bandwidth of 390KHz, a low noise between 537Hz to 390KHz and operates at 0.5V rail-to-rail supply voltage. It was designed for a 0.35μm CMOS process. The OTA's performance satisfies the required parameters for its implementation in biomedical portable devices.**

I. INTRODUCTION

THE TRENDS of scaling down the channel length in CMOS technology and emergence of portable devices such as Ambulatory Brain Computer Interface (ABCI) systems, insulin pumps, hearing aids and mobile communications require to develop circuits that work at ultra low voltage power supply. Moreover, low power dissipation is essential in these systems to have longer battery lifetime and is even more critical in wireless and batteryless systems.

Most of the biomedical portable devices monitor patients all day long. Therefore, such devices must have low power dissipation; typical values in novel devices are around 40μW up to 60μW. In addition, the amplification stage in their analog-front-end must have enough gain and low-noise in the base band to amplify the biomedical signal (0.05Hz-500Hz and 5μV-5mV).

Different techniques have been developed for low-voltage operation such as, charge-pump, low V_{TH}, bulk-forward biased, bulk-driven and devices working in weak inversion. However, charge pump technique is not a true low voltage and the fabrication cost with low V_{TH} process is high. Amplifiers with bulk as input and supply voltages down to 0.8V have been reported in [1], [2], [3] and [4]; and recently a bulk-driven amplifier working in subthreshold region with 0.5V power supply has been reported in [5]. In addition, a gate-driven amplifier with 0.5V rail-to-rail, 62dB DC gain and 75μW power dissipation is also proposed in [5].

Differential pairs are commonly used as input stages, in an ultra-low voltage OTAs the tail current must be removed in order to have more voltage headroom [6]. However, a Common Mode Feedback (CMFB) must be added to improve the Common Mode (CM) operation and CM rejection ratio (CMRR). The configurations reported in the literature are based on current source amplifiers (CSA). This paper proposes a novel topology working with $\pm$0.25V supply voltage. The first stage is similar to the folded cascode (FC) OTA and the output stage is a CSA to achieve greater output swing.

II. SUBTHRESHOLD OPERATION

When the V_{GS} in the MOS transistor is less than the threshold voltage (V_T), the device works in subthreshold region or weak inversion region. In subthreshold region, the I_D curve changes from quadratic behavior to exponential behavior. The current I_{DS} in weak inversion region is given by [7]:

$$I_{DS} = I_{DO}\frac{W}{L}e^{V_G/nU_T}(e^{-V_S/U_T} - e^{-V_D/U_T}) \quad (1)$$

where I_{DO} is the characteristic current, n is the slope factor, U_T is the thermal voltage (kT/q), approximately 25mV at room temperature. The above equation is also applicable for p-channel transistors by changing the signs of V_G, V_S and V_D.

By definition, the gate transconductance can be found from equation 1:

$$g_{md} = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{1}{nU_T}I_{DS} \quad (2)$$

The small signal source conductance can be found from equation 1 as:

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{1}{U_T}I_{DO}\frac{W}{L}e^{V_G/nU_T}e^{-V_S/U_T}e^{-V_{DS}/U_T} \quad (3)$$

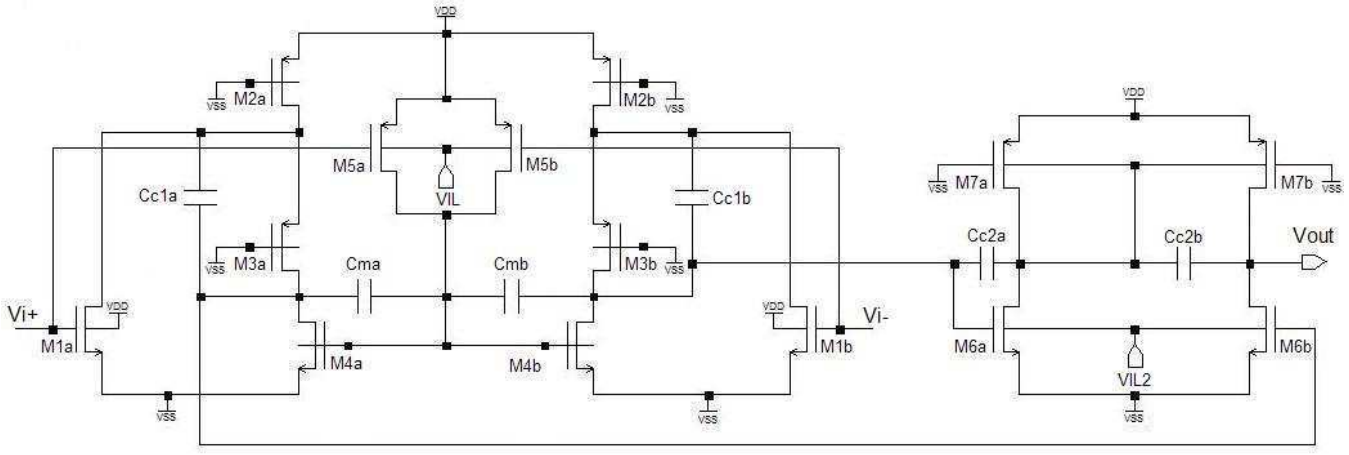

Fig. 1. Differential-input single-output OTA

When V_{DS} is less than $3U_T$ the linearity is poor, on the other hand when $V_{DS} \gg 3U_T$ the conductance is almost constant [8].

III. OTA DESIGN

The proposed OTA consist in two stages. A configuration similar to classical FC was chosen for the first stage and a CSA like for the output stage. The whole circuit is shown in the figure 1.

A. First OTA stage

The main difference between the classical FC configuration and the proposed configuration is that the former has a stack of 4 transistors at its output (figure 2), to obtain a high output resistance. The proposed topology only has a stack of 3 transistors. Assuming that all the devices are working in saturation ($V_{DS_{sat}} \geq 0.1V$), and using 4 transistors at ultra-low voltage supply produce an extremly reduced ouput swing. Hence, to increase the output swing and have relatively higher gains, 3 transistors are stacked. Nevertheless, an extra stage is needed to obtain better ouput swing.

A differential NMOS pair is used as input ($M1_a$ and $M1_b$), the bulks of the transistors are forward biased (tied to V_{DD}) to reduce the V_{TH} and increase the inversion level [5]. In order to maintain the input transistors on, the required $V_{cm,in}$ is $V_{DD}/2$. The $V_{cm,o}$ is set to $V_{DD}/2$ in order to have maximum output swing.

Transistors M3a and M3b constitute two symmetric common gate amplifiers (CGA). The current sources M_{2a} and M_{2b} provide the current bias to the CGA and also are the current sources for differential input. Both CGAs have active current sources composed by M_{4a} and M_{4b}. Bulks of M_2 to M_4 are connected to the gate in order to reduce the V_{TH}.

Considering that I_{tail} has been removed from the design in order to provide voltage headroom, devices M_{5a}, M_{5b} and capacitors C_{c1a}, C_{c1b} are added to perform CM operation and achieve good CMRR. In addition, the output common level ($V_{cm,o}$) is fixed through M_5 bulks.

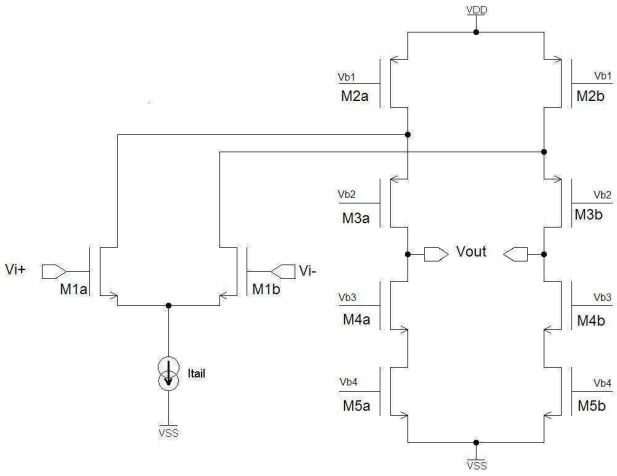

Fig. 2. Classical Folded Cascode OTA configuration

The DC gain of this stage is given by:

$$A_{v_1} = \frac{g_{m1}(g_{ds3} + g_{m3} + g_{mb3})}{g_{ds3}(g_{ds1} + g_{ds2}) + g_{ds4}(g_{ds3} + g_{m3} + g_{mb3})} \quad (4)$$

By decreasing the current in the CGA, the output resistance increases, enhancing the gain of this stage, A_{v_1}. However, the unit gain-bandwidth (GBW) is reduced. The simulation shows a $49.6dB$ gain for the first stage.

The input referred thermal and flicker noise obtained for this stage is:

$$\overline{V}^2_{n_{in}} = 2\overline{V}^2_{n_1} + 2\Big(\frac{g_{m2}}{g_{m1}}\Big)^2\overline{V}^2_{n_2} + 2\Big(\frac{g_{m4}}{g_{m1}}\Big)^2\overline{V}^2_{n_4} \quad (5)$$

and

$$\overline{V}_{n_i}^2 = \frac{8kT}{3g_{mi}} + \frac{KF}{C_{ox}^2 W_i L_i f} \tag{6}$$

where $k = 1.38 \times 10^{-23} J/K$ is the Boltzman constant, T is the temperature, KF is the flicker noise process dependent constant, C_{ox} is the oxide capacitance, f is the frequency, W is the channel width and L is the channel length. The first expression of the equation 6 represents the thermal noise while the second term corresponds to the flicker noise.

In the design g_{m1} is set larger than g_{m2} and g_{m4}, in order to reduce the total input referred noise. Only the noise of the first stage is computed, since the gain is high enough to overcome the equivalent noise of the output stage.

B. Output OTA stage design

A second stage is in cascade with the first stage and is used to achieve higher gains while maximizing the output swing.

For single output, devices M_{7a} and M_{7b} are used to make the conversion from differential to single output. Bulks of both devices are tied together performing a bulk driven mirror. Gates of both transistors are connected to V_{SS} to keep them on. The bulk of the devices M_6 fixes the output common mode operation to $V_{DD}/2$. Figure 3 shows the diagram of the bulk-driven mirror (BDCM) working at subthreshold region.

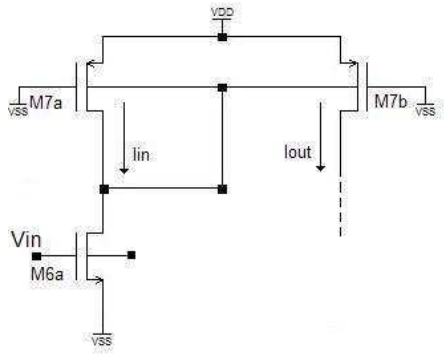

Fig. 3. Bulk-Driven Current Mirror

I_{OUT} is obtained knowing that $V_{GB7a} = V_{GB7b}$, then:

$$I_{OUT} = \frac{I_{IN}(W/L)_{7b}(e^{V_{SB7b}/U_T} - e^{V_{DB7b}/U_T})}{(W/L)_{7a}(e^{V_{SB7a}/U_T} - 1)} \tag{7}$$

If the aspect ratios of the transistors M_7 are the same, equation 7 becomes:

$$I_{OUT} = \frac{I_{IN}(e^{V_{SB7}/U_T} - e^{V_{DB7b}/U_T})}{(e^{V_{SB7}/U_T} - 1)} \tag{8}$$

Also, it is easy to see that if V_{DB} is positive I_{OUT} is slightly greater than I_{IN}.

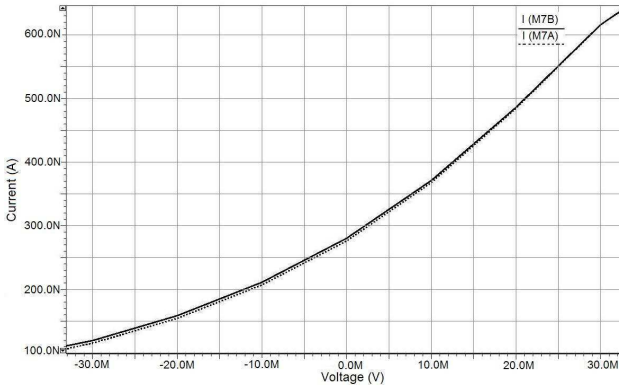

Fig. 4. Comparison between I_{OUT} and I_{IN}

Figure 4 shows the behavior of the BDCM when a sweep of V_{IN} changes the input current.

The gain expression of this stage is given by:

$$A_{v_2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} \left(1 + \frac{g_{mb7}}{g_{ds6} + g_{ds7} + g_{mb7}}\right) \tag{9}$$

the obtained numerical value of this stage was 42.4dB. The whole amplifier gain is 92dB.

IV. SIMULATION

For the simulation of the proposed OTA, BSIM3 models of 0.35μm CMOS process were used. The simulation was done under typical conditions, the circuit was fed with a source of $\pm 0.25V$ and loaded with a resistance and a capacitance of $5M\Omega$ and $2pF$. The transistor's aspect ratios and the capacitor's values are summarized in table I.

TABLE I
TRANSISTORS ASPECT RATIOS AND CAPACITORS VALUES

First Stage			**Output Stage**		
Transistor	Length	Width	Transistor	Length	Width
M_1	500μm	.7μm	M_6	600μm	1.4μm
M_2	450μm	.7μm	M_7	300μm	1.4μm
M_3	250μm	.7μm			
M_4	75μm	.7μm			
M_5	22.2μm	1.4μm			
Capacitors					
Cm	1P	C_{c2}	5P		
C_{c1}	20P				

The OTA has an open-loop DC gain of 92dB, a GBW of 390.1KHz, a PM of 57^o (figure 5) and dissipate 1.94μW. The circuit has better CMRR at low frequencies (see table II).

TABLE II
SUMMARIZED RESULTS

Parameter	**Proposed**	[5]	[6]
Open-loop DC gain	$92dB$	$72dB$	$55dB$
Gain Band Width	$390.1KHz$	$15MHz$	$8.72MHz$
Phase Margin	57^o	60^o	61^o
CMRR @$10Hz$	$48dB$	$85dB$@$5KHz$	$61.9dB$
CMRR @$100Hz$	$45dB$	N/A	N/A
Input ref. Noise @$10KHz$	42 $nV/\sqrt{Hz}$	$120nV/\sqrt{Hz}$	N/A
Input ref. Noise @$4KHz$	$50.4nV/\sqrt{Hz}$	N/A	N/A
Offset	$2.6mV$	$2mV$	N/A
Power Consumption	$1.94\mu W$	$100\mu W$	$77\mu W$

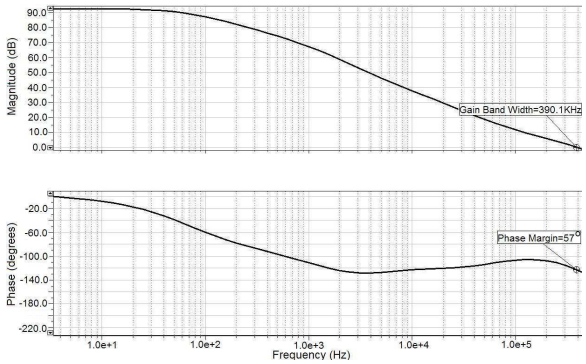

Fig. 5. Open loop frequency response of the OTA

The noise behavior is shown in figure 6, where the flicker noise decreases from $583nV/\sqrt{Hz}$@$1Hz$ to $60nV/\sqrt{Hz}$@$537Hz$. This later frequency is approximately the noise frequency corner.

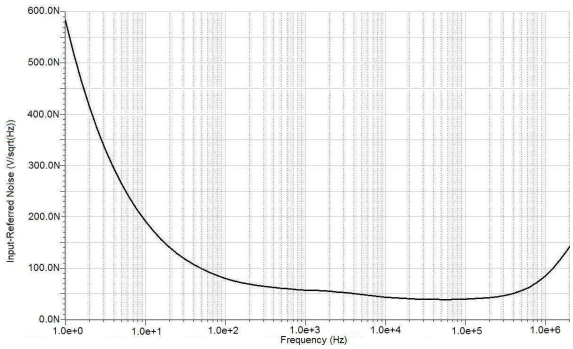

Fig. 6. Input referred noise of the OTA

V. DISCUSSION

Comparing the simulation results with previous reported work [5] [6], our proposed design has larger open-loop DC gain and dissipate less power ($1.94\mu W$). The input-referred noise is lees than the reported in [5]. The circuit present the smallest GBW. However, since several biomedical signals have frequencies much less than $390.1KHz$, we were not concerned in achieve a high GBW.

The proposed OTA has the advantage of high DC gain and low-noise while dissipating low-power.

The overall results are summarized in table II.

VI. CONCLUSIONS

A differential-input single-output OTA that operates with $\pm 0.25V$ rail-to-rail has been proposed in this paper. The OTA achieves high gain ($92dB$), low noise in the $538Hz$–$390.1KHz$ frequency band ($\leq 60nV/\sqrt{Hz}$) and a CMRR of $48dB$@$10Hz$. The CMRR can be improved by adding a CM network like the one proposed in [5].

The OTA's performance satisfies the required parameters for its implementation in biomedical portable devices.

REFERENCES

[1] J. Rosenfeld M. Kozak and E. G. Friedman, *"A bulk-driven CMOS OTA with 68 dB DC gain"*, in Proceedings of the 2004 11th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2004., 13-15 Dec. 2004., Pages:5-8.

[2] Y. Haga, H. Zare-Hoseini, L. Berkovi, I. Kale, *"Design of a 0.8 Volt fully differential CMOS OTA using the bulk-driven technique"*, in IEEE International Symposium on Circuits and Systems, ISCAS 2005., 23-26 May 2005., Pages:220-223 Vol. 1.

[3] L. H. de Carvalho Ferreira, T. C Pimenta, *"An ultra low-voltage ultra low power rail-to-rail CMOS OTA Miller"*, in The 2004 IEEE Asia-Pacific Conference on Circuits and Systems, 2004. Proceedings., Vol. 2, 6-9 Dec. 2004 Pages:953-956.

[4] C. Tai; J. Lai; R. Chen, *"Using Bulk-driven Technology Operate in Sub-threshold Region to Design a Low Voltage and Low Current Operational Amplifier"*, in 2006 IEEE Tenth International Symposium onConsumer Electronics, ISCE '06., 2006. Pages:1-5.

[5] S. Chatterjee,Y. Tsividis,P. Kinget, *"0.5-V analog circuit techniques and their application in OTA and filter design"*, in IEEE Journal of Solid-State Circuits, Vol. 40, Issue 12, Dec. 2005 Pages:2373-2387.

[6] M. Abdulai, P. Kinget, *"A 0.5 V fully differential gate-input operational transconductance amplifier with intrinsic common-mode rejection"*, in Proceedings. 2006 IEEE International Symposium on Circuits and Systems, ISCAS 2006., 21-24 May 2006., Pages:2837-2840.

[7] E. Vittoz, J. Fellrath, *"CMOS analog integrated circuits based on weak inversion operations"*, in Journal of Solid-State Circuits, IEEE Vol. 12, Issue 3, Jun 1977 Pages:224-231.

[8] X. He, K. Pun, C. Choy, C. Chan, *"A 0.5V fully differential OTA with local common feedback"*, in Proceedings. 2006 IEEE International Symposium on Circuits and Systems, ISCAS 2006., 21-24 May 2006 Pages:1559-1562.