Skiroc : a Front-end Chip to Read Out the Imaging Silicon-Tungsten Calorimeter for ILC

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Abstract

Integration and low-power consumption of the read-out ASIC for the International Linear Collider (ILC) 82-million-channel W-Si calorimeter must reach an unprecedented level as it will be embedded inside the detector. Uniformity and dynamic range performance has to reach the accuracy to achieve calorimetric measurement. A first step towards this goal has been a 10,000-channel physics prototype of 18*18 cm which is currently in test beam in CERN.

A new version of a full integrated read out chip (SKIROC) has been designed to equip the technologic prototype to be built for 2009. Based on the running physics prototype ASIC (FLC_PHY3), it embeds most of the required features expected for the final detector.

The dynamic range has been improved from 500 to 2000 MIP. An auto-trigger capability has been added allowing built-in zero suppress. The number of channel has been doubled reaching 36 to fit smaller silicon pads and the low-noise charge preamplifier now accepts both AC and DC coupled detectors. After an exhaustive description, the measurement results of that new front-end chip will be presented. The results on the technological R&D concurrently conducted on the ultra-thin PCB hosting both the front-end electronic and the silicon detectors will also be described.

• I - INTRODUCTION

Integration and low-power consumption of the read-out ASIC for the International Linear Collider (ILC) 82-million-channel W-Si calorimeter must reach an unprecedented level as it will be embedded inside the detector. Uniformity and dynamic range performance has to reach the accuracy to achieve calorimetric measurement. A first step towards this goal has been a 10,000-channel physics prototype of 18*18 cm which is currently in test beam in Fermilab.

A new front-end chip called SKIROC – standing for *Silikon Kalorimeter Read-Out Chip* – has been designed to read-out the upcoming generation of Si-W calorimeter featuring ILC requirements. The analogue core of SKIROC is based on the front-end electronic designed for that physics prototype. It has been enhanced in many ways using an intermediate prototype called ILC_PHY4. The Maximum input charge has been extended from 500 to 2000 MIP. The number of channel has been doubled – reaching 36 - to fit a pad size reduction in the silicon detector design conducted concurrently. A stand alone working capability comes along with the full power pulsing feature. That means SKIROC does not need any external component such as decoupling capacitance or bias resistor involving a huge room saving. The wake up sequence duration of the power pulsing is around 2μs to ensure a lower than 1% duty cycle in an ILC-like beam structure [1], involving more than two order of magnitude of power saving.
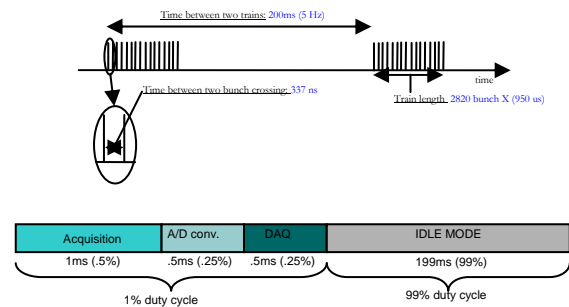

Fig. 1 – ILC beam structure and electronic sequence

Beyond the analogue core improvement, many features have been implemented in SKIROC. A channel by channel auto-trigger capability has been added allowing a built-in zero suppression. A multi-channel ADC is embedded. The trigger and gain selection threshold is set by an internal dual DAC. Voltage references used in the analogue core use a bandgap reference [2]. A digital core driving all the analogue features and the digital communication with the DAQ has been designed and is implemented in a FPGA to get debugged and improved before being embedded in the next version.

This abstract will described the SKIROC chip and present results of different elementary block used to design SKIROC, including the ILC_PHY4 chip – the SKIROC starting point.

II – SKIROC DESCRIPTION

SKIROC is a 36-channel front-end chip designed to read-out silicon PIN diodes for calorimetry application. It has been

designed in a general framework ensuring consistent back-end of different front-end ASIC for several calorimeters (HaRDROC to read out the digital RPC HCAL prototype and SPIROC to read out the SiPM and Sci tiles HCAL prototype are the two others chip existing on that framework)

Its main characteristics are the following:

- AMS SiGe 0.35μm technology
- 20mm² (4mm × 5mm) area
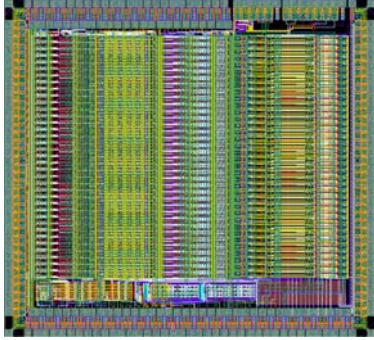- 3.3V power supply
- Package: CQFP240

Fig. 2 – SKIROC layout

Each channel is made of a variable-gain low-noise charge preamplifier followed by both a dual shaper – one with a gain 1 and the other with a gain 10 - to filter the charge measurement and a trigger chain composed of a high gain fast shaper and a discriminator. The measured charge is stored in a 5-depth SCA that can be read either in an analogue way or can be connected to a multi-channel 12 bit Wilkinson ADC. Thresholds are set with a 10-bit DAC for trigger level and for automatic gain selection level. A bandgap ensures the stability versus supply voltage and temperature for all the requested reference in the analogue core.
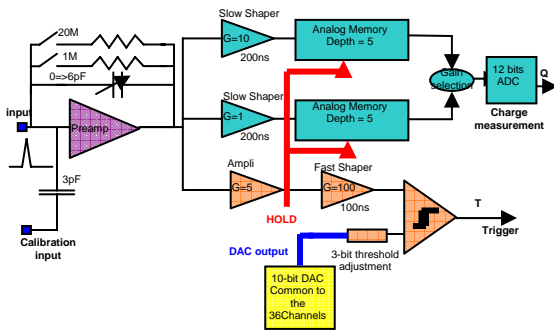

Fig 3 – One channel block diagram

The digital signals requested for digital and analogue block communications are outputted using a dynamic multiplexing to reduce the pin count while emulating the digital core in a FPGA.

III – BLOCKS MEASUREMENTS

The blocks used to design SKIROC has been fully characterized before being used in the ASIC. At the moment this abstract is written, results on SKIROC are being processed and final results will be presented during the conference.

The analogue core of SKIROC is mainly inspired from ILC_PHY4 front-end chip prototype. Extensive measurements have been conducted on ILC_PHY4 to validate the stand-alone working capability without any decoupling capacitance or bias resistor. Results below (Fig 4) show that the performances in term of linearity are compatible with calorimetry measurement.
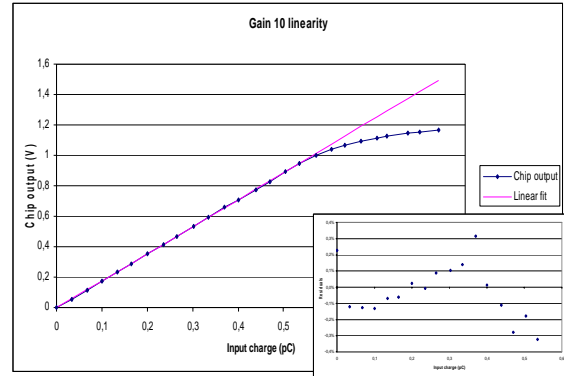

Fig 4 – Linearity and residual of ILC_PHY4

The equivalent noise charge of the preamplifier is measured around 2000 electrons. After shaping, the simulated MIP to noise ratio is 16 for the trigger line and 11 for the charge measurement. Crosstalk is around the per mil level.

The bandgap characterization shows a 10ppm/°C drift ensuring the stability of the pedestal with temperature. The stability of the voltage reference with power supply is ensured for supply included within 2.8V to 3.8V for a nominal value of 3.3V.
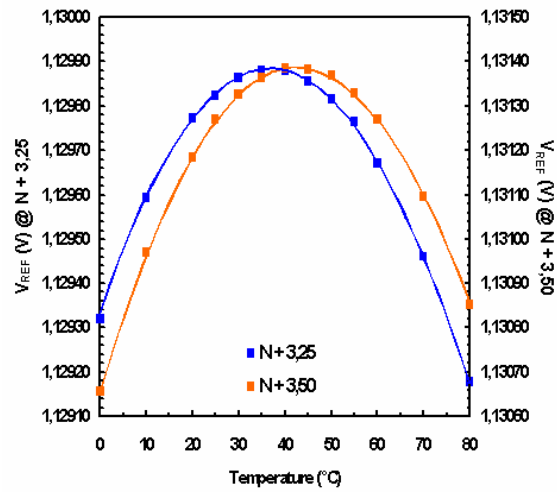

Fig 5 – Bandgap stability measurement

The DAC performances measured on HaRDROC show linearity in the per-mil range and an output voltage swing of 2V covering the whole useable threshold range.
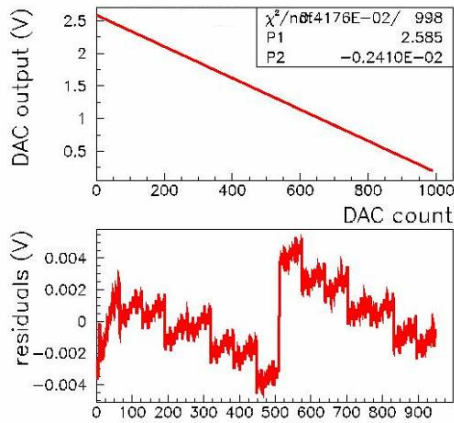

Fig 6 – Dual DAC linearity measurement

The 12-bit 36-channel ADC is a Wilkinson using a full differential structure. The simulated non-linearity is shown in Fig 7 and fill the requirements for a calorimetry measurement.
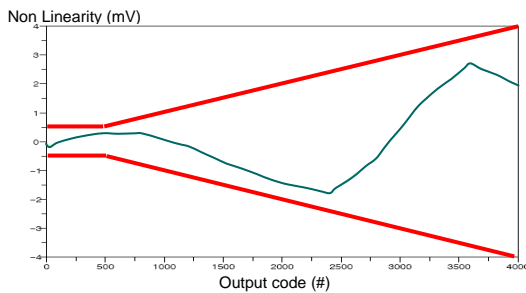

Fig 7 – Wilkinson ADC non linearity

Several points on these blocks have been improved in SKIROC and the coming measurements should validate a fully functional self-triggered front-end chip.

IV – CONCLUSION

The SKIROC chips will be used to equip the 40,000-channel ECAL foreseen for 2009 that will validate the technological choices for the 82-million-channel final detector. Many of the final detector requested features have been embedded and the performance has been greatly improved compared to the physics prototype front-end chip. The production of that ASIC is foreseen in summer 2008 to be able to take data in 2009, before the engineering design report of the final detector planned for 2010 by the ILC Worldwide Study Bureau.

V – REFERENCES

[1] TESLA Technical design report

http://tesla.desy.de/new_pages/TDR_CD/start.htm

[2] Acknowldgement to Fabrice Voisin – Bandgap reference – IN2P3 Microelectronic school. Designer of the bandgap used in SKIROC