A Charge-Sensitive Amplifier Associated with APD or PMT for Positron Emission Tomography Scanners

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Abstract - We present a Charge-Sensitive Amplifier (CSA) to be coupled with a 511-KeV 2-photon detector for positron emission tomography scanners. The circuit has been designed to be associated with an Avalanche Photodiode (APD) or Photo-Multiplier Tube (PMT) with large capacitance. It is a two-stage structure. The input stage consists of a folded-cascode fully-differential part and a common-mode feedback (CMFB) circuit. The output stage employs complementary source followers. The amplifier has been designed in a 0.35µm BiCMOS process with optimization of noise and speed performances to meet specific constraints. Its main characteristics evaluated by post-layout simulations are: 70-dB DC gain, 4.6-GHz GBW, 20-ns peaking time for pulsed stimulus, 3900-electron equivalent input noise charge (ENC), 135-mW power consumption at 3.5 V supply.

I. INTRODUCTION

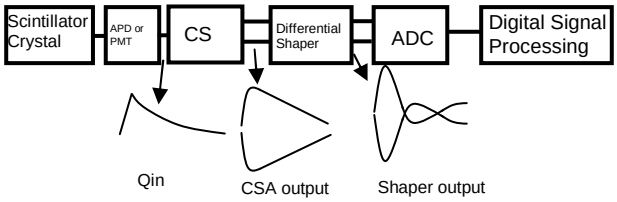
Positron Emission Tomography (PET) scanners have been recognized as very powerful and sensitive instruments for biomedical purposes such as brain studies, cardiac imaging, early cancer diagnosis and therapy. They operate by indirect detection of radioisotope's positron emission, which annihilates with an electron to produce a pair of 511-KeV (gamma) photons emitting in opposite direction. Each escaped photon may hit a scintillator to generate a pulsed light that can be detected using a photomultiplier tube (PMT) or an avalanche photodiode (APD). Via sensitive and rapid detection of the 511-KeV photon pair, the positron annihilation event can be localized on a straight line of coincidence (line of response, or LOR).

PET scanners should make use of low-noise and rapid electronics associated with PMT or APD. The associated electronics may include successive charge-sensitive amplification, analog filtering, A-to-D conversion and digital signal processing, as shown in Fig 1a.

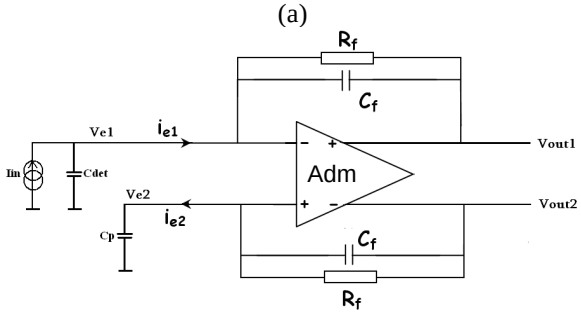
For developing such systems, there has been demand for custom design of detector-associated electronics to meet specific requirements, especially on speed and sensitivity performances. One challenge of the design task is the detector-coupled charge-sensitive amplifier, which is the first stage of the associated electronics.

The performance requirements for the amplifier include: about 5-GHz gain-bandwidth product (GBW), minimum detectable charge of 4000 electrons, 40dB dynamic range. On the other hand, it should be mentioned that the detector capacitance is large: 10pF for the PMT and 50pF for the APD respectively.

We present in this paper the design of an amplifier for this application. The proposed circuit is based on a fully differential amplifier (Fig. 1b), which allows input adaptation to either PMT or APD (having reversed output), and output adaptation to the following differential-mode shaper stage. Its symmetrical structure is also advantageous for reduction of electromagnetic noise.



(a)



(b)

Fig. 1a) Architecture of the detector-associated electronics; b) charge-sensitive amplifier using a fully differential amplifier

II. Circuit description

The charge-sensitive amplifier consists of two stages. The input stage is a fully differential structure including a common-mode feedback (CMFB) block. The output stage is a source-follower performing impedance adaptation.

A. Input stage

The input stage for differential operation is a symmetrical structure. Its differential operation can be described using a half circuit because of its symmetrical structure. The half circuit is shown in Fig. 2.

This half circuit is a folded-cascode amplifier employing an input *p-type* MOSFET (M1) and an *npn* transistor (Q7). The input MOSFET with very low leakage gate current has minimized noise effect of the related shot-noise current source. The use of bipolar component in the cascode structure allows improvements of gain and frequency performances. It also occupies a much smaller surface area compared to a large-size MOSFET.

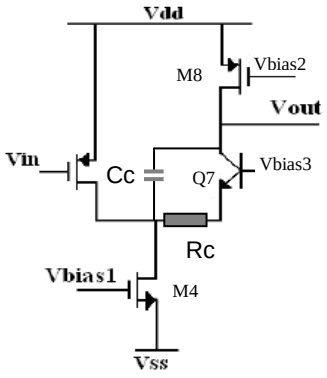


Fig. 2. Half circuit of the amplifier for differential operation

As the photodetector to be coupled has large capacitance, large-size MOSFETs are employed, especially for the input transistor M1 (W/L = 5000µm/0.35µm). By setting a bias current up to 10mA for M1, its transconductance g_m may reach 100mA/V to enhance gain and gain-bandwidth product (GBW), and to reduce its channel thermal noise.

The required gain for the amplifier is about 70dB. It can be achieved using M8 as active charge with a bias current of 0.35mA. This simple active charge allows improved output dynamic swings, which is an aspect to be considered as the supply voltage is only 3.5V for the circuit.

The DC gain of the half circuit is given by:

$$A_0 = -\frac{g_{m1} g_{m7} r_{ds1-4}}{g_{ds8}\left(1 + g_{m7} r_{ds1-4}\right)} \qquad (1)$$

where $r_{ds1-4} = r_{ds1} // r_{ds4}$ is only a few hundred ohms because of large sizes and large bias currents. However, thanks to large transconductance of Q7, $g_{m7} r_{ds1-4} >> 1$ and the gain can approximately be estimated by:

$$A_0 \approx -\frac{g_{m1}}{g_{ds8}} \qquad (2)$$

The bandwidth is determined by the time constant of the output node, given by:

$$f_c = \frac{g_{ds8}}{2\pi C_{out}} \qquad (3)$$

To preserve bandwidth while ensuring close-loop stability, a feedforward compensation technique [3] is implemented by adding passive components R_c and C_c. Proper choice of the added components allows second-pole cancelation by a negative zero. R_c is chosen to satisfy the following condition:

$$g_{ds1} \le \frac{1}{R_c} \le g_{m7} \qquad (4)$$

and C_c is optimized for a good phase margin.

The fully differential part of the input stage (not including the feedforward compensation network) is shown in Fig. 3a. An additional transistor M5 sets the bias currents of the input pair (M1, M2). Its gate bias not only controls I_{ds1} and I_{ds2}, but also affects the bias currents of the differential output branches (i.e. branch of M9, Q6 and that of M8, Q7 respectively). Thus it can be connected to the output of the CMFB circuit to adjust the common-mode output bias voltage $V_{out,cm}$ (= (V_{out1} + V_{out2})/2).

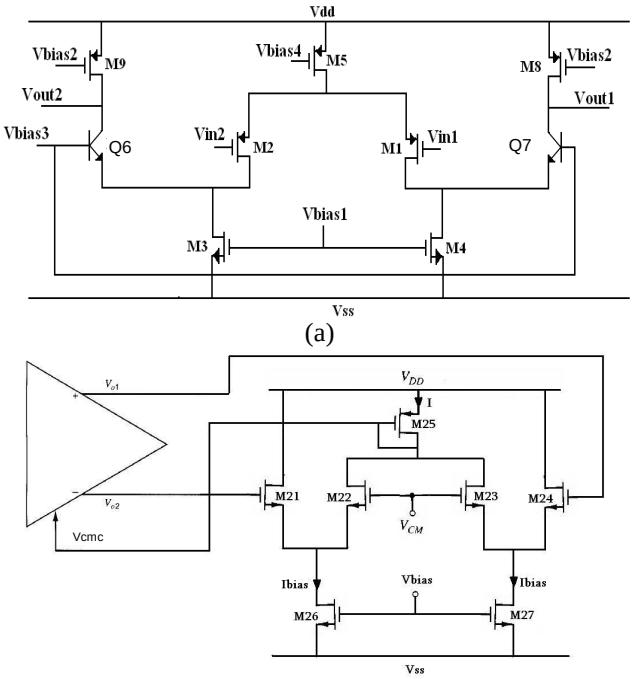


Fig. 3. Input stage consisting of a fully differential part (a) and a CMFB circuit (b)

The CMFB circuit with connections to the fully differential part is presented in Fig. 3b. It is similar to the one proposed by [5]. The common-mode output bias voltage of the differential part $V_{out,cm}$ is sensed by a transistor pair (M21, M24). An increase of $V_{out,cm}$ will raise the sum of their drain currents (I_{ds21} + I_{ds24}). Assuming constant bias currents for M26 and M27, the rise of (I_{ds21} + I_{ds24}) will lead to the decrease of the sum of another pair's drain currents (I_{ds22} + I_{ds23}), which is equal to the drain current of M25 $I_{ds\ 25}$. The resulting reduction of the gate-source voltage $|V_{gs25}|$ is feedback to M5 of the differential part, allowing final lowering of $V_{out,cm}$. Thanks to this feedback control, a very low common-mode gain of the input stage (e.g. $A_{cm} << 1$) can be achieved.

It should be noted that the node at the drain of M25 has a related non-dominant pole expressed as:

$$p_{nd} = \frac{g_{m25}}{C_{gs5} + C_{gs25}} \qquad (5)$$

It may cause instability when choosing too low bias current for M25. To avoid this problem, the minimum current ratio I_{ds25}/I_{ds5} should be about 0.5.

B. Source-follower output stage

The output stage of the amplifier consists of two source followers driven respectively by the differential outputs of the input stage. In order to optimize output swings, the source follower driven by V_{out2} is composed of n-type transistors, while the other source follower for V_{out1} employs p-type components (shown in Fig. 4). It is noted that the input signal of the amplifier is always a positive one. This means that the non-inverting output of the input stage V_{out2} has a upward swing range from $V_{out,cm}$ to (V_{dd} − $V_{ds9,sat}$) while its inverting output V_{out1} has a downward swing from $V_{out,cm}$ to ($V_{ds4,sat}$ + $V_{ce7,sat}$). The proposed complementary source followers as output stage operate for these swing ranges.

However, there is some loss of symmetry for the differential outputs of the amplifier; in particular the output bias voltages may be significantly different. This disadvantage will not raise serious problems for the application case, because the amplifier coupling with the following shaper stage is capacitive. Other dissymmetrical problems such as gain differences may be minimized through careful design.

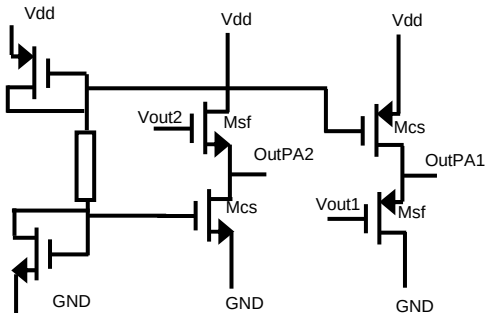


Fig. 4. Output stage consisting of two complementary source followers

C. Frequency and pulsed stimulus response of the amplifier

As the following output stage is a source-follower circuit with a gain close to unity, the GBW of the amplifier is approximately given by:

$$GBW \approx |A_0| f_c = \frac{g_{m1}}{2\pi C_{out}} \tag{6}$$

For a pulsed charge stimulus, the rise time of the amplifier's response is determined by the time constant:

$$\tau_{csa} = \frac{C_d}{2\pi \cdot GBW \cdot C_f} \tag{7}$$

where C_d is the detector capacitance, and C_f is the feedback capacitor of the amplifier. C_f should properly be chosen. On the one hand, according to the above expression, it should be increased to reduce the time constant, but on the other hand, it should be small enough to minimize effect of the input-related pole on the stability.

III. Noise analysis

The equivalent circuit of the CSA half circuit for noise analysis is shown on Fig. 5. Noise sources from the detector and its biasing network do not appear in Fig. 5 and are not considered here (Detailed analysis of such noise sources can be found in [6] and [7]).

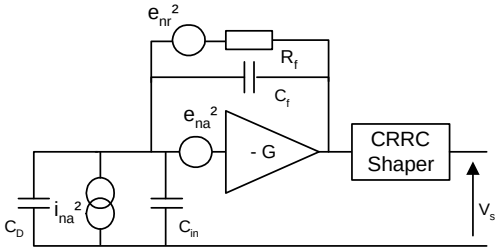


Fig. 5. Equivalent circuit for noise calculation

The parallel and serial input referred noise sources of the CSA are denoted respectively as i_{na}^2 and e_{na}^2. A voltage noise source, denoted as e_{nr}^2, is inserted to take into account the thermal noise of the feedback resistor R_f. C_D is the detector capacitance and C_{in} is the input transistor gate capacitance.

The parallel input noise i_{na}^2 corresponds to the shot noise generated by the input transistor's gate leakage current. For CMOS technology, this input current is negligible and so its related noise can be neglected.

The feedback resistor's thermal noise e_{nr}^2 is given by:

$$\frac{d\left\langle e_{nr}^2 \right\rangle}{df} = 4kTR_f \tag{8}$$

where k is the Boltzmann constant and T the temperature in Kelvin.

The bandwidth of this white noise source is limited by the time constant of the feedback network ($\tau_f = R_f C_f$) and by the peaking time τ_s of the CRRC shaper. The contribution of this noise evaluated at the shaper output is:

$$v_{nr}^2 = \frac{kT}{C_f}\frac{\tau_s}{(\tau_f + \tau_s)} \approx \frac{kT}{C_f}\frac{\tau_s}{\tau_f} \tag{9}$$

Since the peaking time τ_s is much lower than the feedback network characteristic constant time τ_f, the resistor feedback thermal noise contribution at the shaper output can be neglected.

The serial noise e_{na}^2 is mainly contributed by the noise from the input transistor.

Its power spectral density is given by:

$$\frac{d\left\langle e_{na}^2\right\rangle}{df} = \frac{8}{3}\frac{kT}{g_{m1}} + \frac{K_f}{C_{ox}^2 WLf} \qquad (10)$$

where g_{m1} is the transconductance of transistor M1, C_{ox} is the gate oxide capacitance per area, K_f is the process dependant flicker noise parameter.

The first term in (10) takes into account the thermal noise of the M1 channel.

The second term in (10) describes the flicker noise resulting mainly from the charge trapping in the transistor channel.

The serial noise is firstly amplified by the CSA and then filtered by the CRRC shaper. Its contribution at the shaper output is given by [8]:

$$v_{na}^2 \approx \left(\frac{C_{in}+C_d}{C_f}\right)^2 \left(1.57\frac{2kT}{3\pi\tau_s g_{m1}} + \frac{K_f}{2C_{ox}^2 WL}\right) \qquad (11)$$

The equivalent input noise charge (ENC) is given by:

$$ENC_{na} \approx (C_{in}+C_d)e\sqrt{1.57\frac{2kT}{3\pi\tau_s g_{m1}} + \frac{K_f}{2C_{ox}^2 WL}} \qquad (12)$$

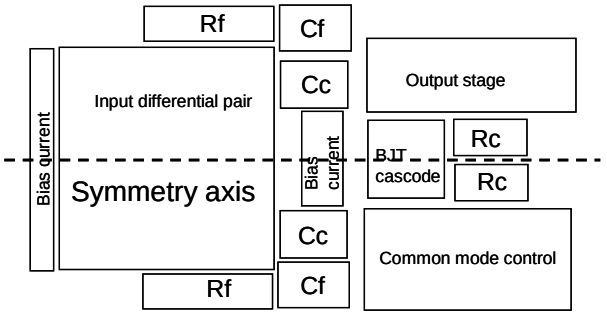
where *e* is the Neper number.

Because of the short peaking time of the shaper, ENC is dominated by the input transistor's thermal noise contribution.

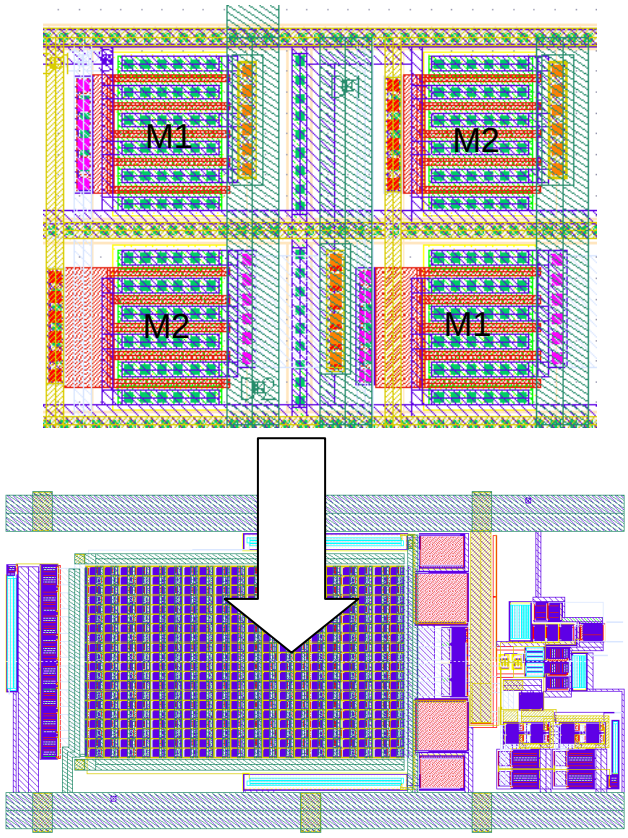
Equation (12) shows that a low noise CSA design should implements input transistors with large transconductance while maintaining their input capacitance much lower than the detector capacitance. Such a tradeoff implies the implementation of large input transistor with minimum gate length L (0.35µm) to achieve high W/L ratio (for large g_m) with the minimum WL product (for reducing the input capacitance).

IV. CHARACTERISTICS

The proposed amplifier has been designed in a 0.35µm BiCMOS process (AMS). The floor plan of the layout is shown in Fig. 6a. Layout of the high-gain input stage is generated with application of symmetry and common-centroid techniques. For the large-size input differential pair (M1, M2), its layout is an array of 10x10 common-centroid cells in parallel connections (Fig. 6b).



(a)



(b)

Fig 6. a) Floor plan of the amplifier layout; b) Layout showing an array of 10x10 common-centroid cells, which is the large-size input differential transistor pair (M1, M2)

Post-layout simulations have been performed to evaluate the characteristics of the designed amplifier.

Fig. 7 shows the frequency response of the amplifier. The estimated GBW is 4.6GHz with a phase margin of 79°. The phase evolution with increasing the frequency is not monotonic, because practical implementation of feedforward compensation has difficulties in precise zero-pole cancelation. It is however necessary to minimize phase oscillation for stability consideration. This can be done by adjusting the values of the compensation components (R_c and C_c).

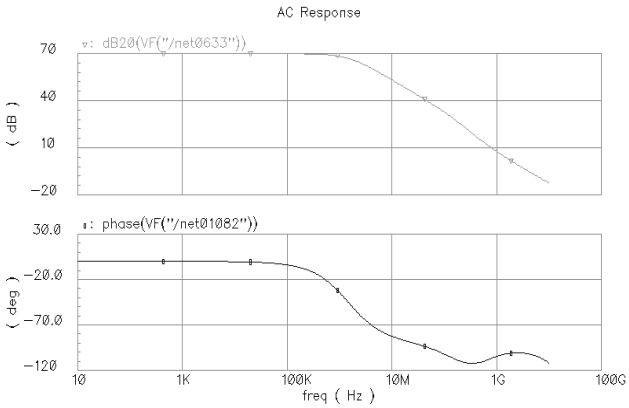


Fig 7. Frequency response of the amplifier

Fig. 8a presents simulated pulsed response of the amplifier. The stimulus is a 1-V, 5-ns step-function voltage source with 50-pF detector capacitance in parallel. Via 0.7-

pF capacitive coupling, the pulsed stimulus is applied to the amplifier input. The corresponding peak-to-peak differential output voltage is slightly over 1V with a peaking time of 25ns. Fig. 8b shows simulated response to an APD-like output signal: the stimulus has a rise time of 5ns and an exponential decay time of 40ns. In this case, the peak-to-peak differential output voltage is 0.9V and the peaking time is 103 ns.

Post-layout simulations with extracted parasitic parameters show significant noise performance degradation at 150µV_{RMS} (ENC ~ 3900 electrons) compared to 130µV_{RMS} by schematic simulations. This increase of noise is mainly due to serial resistance of the poly-Si gate of the input transistor pair. This extracted resistance is about 70Ω compared to the g_{m1}^{-1} (~ 10Ω).

Table 1 summarizes the characteristics of the amplifier, obtained by post-layout simulations. The fabrication of the circuit is underway. We expect to undertake the testing work as soon as it is fabricated.

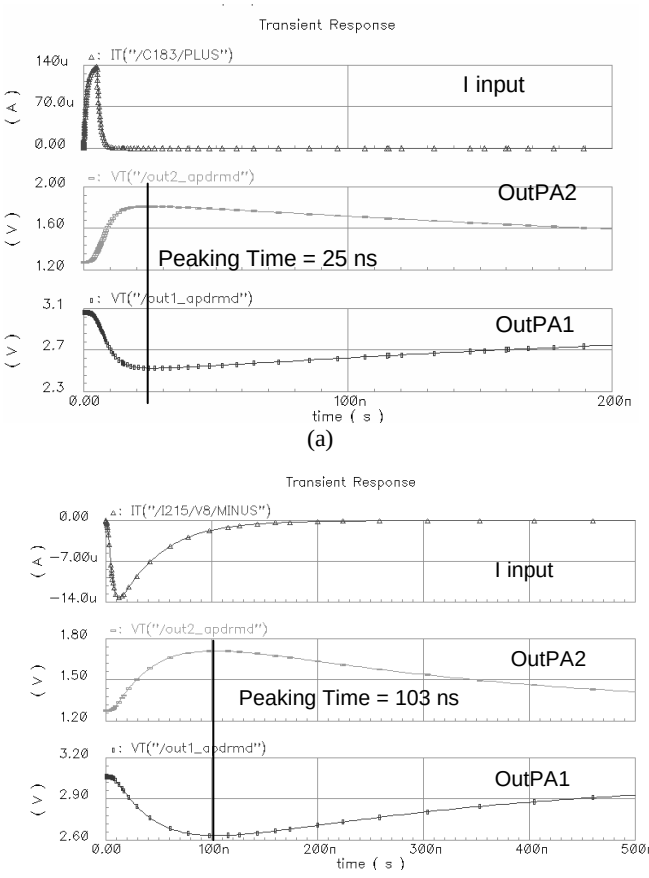


Fig. 8. Temporal response of the amplifier to pulsed stimulus (a) and APD-like input signal

Area	0.195 mm^2
Supply voltage	3.5V
Power supply	135 mW
DC gain	70 dB
GBW	4.6 GHz
R_c	100 ohms
C_c	2pF
Phase Margin	79 Deg
R_f	300 kΩ
C_f	1pF
Equivalent input noise charge (by schematic simulations)	3530 electrons
Equivalent input noise charge (by post-layout simulations)	3900 electrons
OutPA1 dynamic swings	1.2V to 1.8V
OutPA2 dynamic swings	3.1V to 2.54V
Maximum integrated charge	700 fC
Dynamic range	39 dB
Peaking Time (pulsed stimulus)	25 ns
Peaking Time (APD-like stimulus)	103 ns

Table 1. Main characteristics of the amplifier, obtained by post-layout simulations

V. CONCLUSION

We have designed a charge-sensitive amplifier for development of PET scanners. Its speed and noise performances are optimized for this application. By post-layout simulations, we have evaluated its main characteristics: 70-dB gain, 4.6-GHz GBW, 20-ns peaking time for pulsed stimulus, 3900-electron noise (ENC), and 135-mW power dissipation at 3.5-V supply.

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