Acquisition chain for CTF3 pick-ups read-out

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Abstract: since 2005, LAPP got involved in the development of new electronics system of intensity and deviations acquisition for the CTF3 (CLIC Test Facility 3) collaboration.
The aim of this system is to perform the analog to digital conversion of inductive pick-ups signals the closer as possible to the beam in order to reduce the cost of the expensive existing acquisition (analog signals cables and digitizers in VME crates).
The system includes the full chain from preamplification to data processing: analog preamplification module, analog transmission, digitalization board, network and data process/display software.
From 2006 to 2009, 50 chains have been installed in several beam lines of the accelerator.
This document describes the chosen technical solutions.

Summary:

1- Pick-ups and Analog module.

In TL2/CLEX, the signals from pick-ups -BPIs and BPMs- are acquired using the Digital Front-End boards (DFE), developed by LAPP. BPMs have been developed at CERN [1] and BPIs have been developed at LNF-INFN [2].
Thanks to compatibility between analog modules (from CERN and LAPP), it has been decided to pre-amplify several BPM provided by Upsalla with LAPP analog modules in TBTS lines.
The most important difference between the two pick-ups is the electrode planes orientation: BPM and BPI have 45° tilted electrodes planes.
In CTF3, beam pulses duration is about 140ns and repetition rate is maximum 5Hz.

1-1 Pick-ups and signals: beam and calibration.

Both pick-ups are composed by four electrodes. Electrode is an inductive part: the electrode represents the primary of a transformer and the ***n*** turns winding around the core represent the secondary (***1:n***).
Due to current intensity and bandwidth adjustment, different resistances are connected in parallel inside the pick-ups. So, they have different output impedances and different current gains.

The electrode output current is converted in voltage using a load.
The transfer impedance between the current beam and one of the 4 converted voltages has been defined as follows:

$$Zt = {Vs}/{Ib} = {Rl}/{4n}$$

Vs the voltage due to current transformation and ***Ib*** the beam current.
Rl the load resistance and ***n*** the number of turns at the secondary (the transformer primary is 1 turn). It is a useful characteristic using a centered beam.

Only regarding the electrode current ***I***,

$$Vs = I.{Rl}/{n}$$

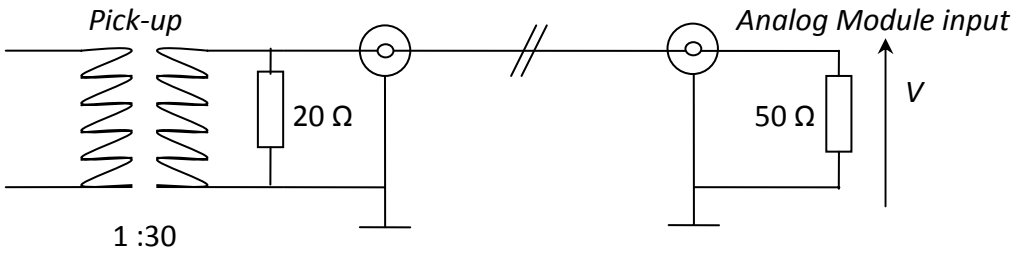
The transmission lines are 50Ω and so the final current to voltage conversion is achieved using a 50Ω resistor at the input of the analog preamplifier.

Calibration: a primary winding allows the calibration of the pick-up, replacing the electrode for the current induction.

a) Beam monitoring principles: intensity and deviations.

Both pick-ups (BPM/BPI) are built with 4 electrodes which drain the images of the beam current.
The space distribution of this coming back current depends on the beam deviation from the center of the pick-up: a deviation towards an electrode introduces a higher electrode current.
As the electrodes responses are linear when beam is quite centered, for a constant beam current, the sum of the signals from the 4 electrodes is constant whatever the deviation.
So, the sum of currents represents the intensity.
Differences between opposed electrodes currents correspond to the deviation from the "electric" center of the pick-up.

b) BPI: number of turns 30, output parallel resistor 20Ω.



The current is converted into voltage on a load about ***50//20≈14Ω***.

$$Zt \approx 14/120 \approx 0{,}117\Omega$$

The bandwidth of the pick-up electrodes is 400kHz – 100MHz.
For the foreseen maximum deviations *(+/- 15mm horizontal & +/-10mm vertical)* and for a maximum beam current about ***35A***, the estimated voltage at the 4 inputs is:

0,94V<Vs<7,06V

Whatever the deviation (still the pick-up response is linear), the sum of the four electrodes voltages, for a 35A beam current, is about:

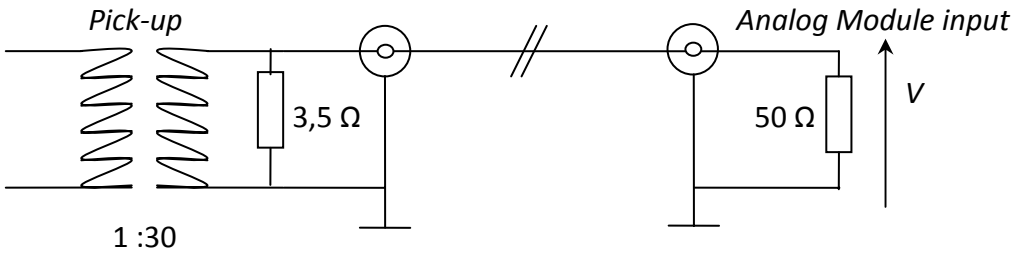
ΣVs=16V

Only regarding one electrode current ***I***, $Vs \approx I.{}^{14}\!/_{30} = I.0{,}467$

Calibration: the number of primary turns is 2 and the line is 50Ω, so for an injected ***Ical*** calibration current, the voltage will be:

$$Vs = 2.Ical.{}^{Rl}\!/_{n} = Ical.0{,}933$$

c) BPM: number of turns 30, output parallel resistor 3,5Ω.



The current is converted into voltage on a load about ***50//3,5≈3,27Ω***.

$$Zt \approx 3{,}5/120 \approx 0{,}027\Omega$$

The bandwidth is different for sum of deviations, maximum bandwidth is 150 Hz – 300 MHz.
Whatever the deviation (still the pick-up response is linear), the sum of the four electrodes voltages, for a 35A beam current, is about:

ΣVs≈4V

Only regarding one electrode current ***I***, $Vs \approx I.{}^{3{,}27}\!/_{30} = I.0{,}109$

Calibration: the number of primary turn is 1 and the line is 50Ω, so for an injected ***Ical*** calibration current, the voltage will be:

$$Vs = Ical.{}^{Rl}\!/_{n} = Ical.0{,}109$$

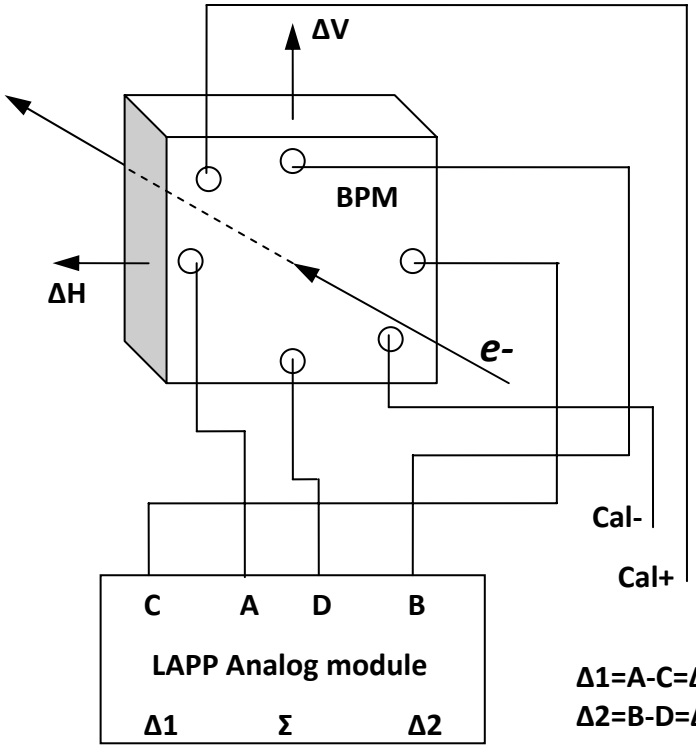
1-2 Analog module and pick-ups connections. (cf. annex 1 & 2)

A pre-amplifier converts electrodes currents into voltages using 50Ω input loads. Dynamic range of input signals have to be adapted the to the acquisition system dynamic.
The analog module developed by LAPP is inspired by the CERN analog module used to pre-amplify the BPM pick-ups located in other places of the accelerator as linac.
An important specification was to develop a full compatible BPM/BPI analog module.
The analog module processes horizontal, vertical deviations and beam intensity.
It is supplied and controlled (gains, calibrations, attenuators) using a standard CERN/LAPP 12 conductors cable. It provides the calibration current to the pick-up.
Analog modules are distributed on the different lines from TL1 to CLEX.
In TL1 and Combiner Ring, the signals from the analog modules are transmitted to VME crates ADCs which are located in the gallery upstairs. These transmissions require long N type cables with low attenuation.
Concerning the pick-ups located from TL2 to CLEX, signals are acquired using LAPP Digital Front-End boards which are located in crates all around the accelerator.

a) Intensity and deviations: sum and differences. Connections between pick-ups and analog modules.

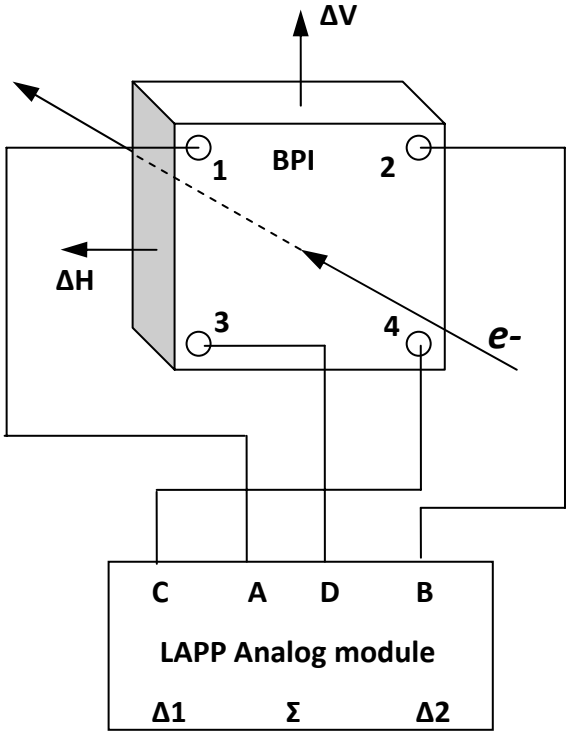
The module processes a sum Σ of the 4 input voltages which corresponds to the beam intensity. It processes two differences Δ1 & Δ2 which contain the deviations information. As the BPI pick-up has electrodes planes 45° tilted, the acquired data will have to be digitally processed to obtain real deviations.
By definition, standard horizontal and vertical signals should have the same sign than the sum if the beam deviates by the left and by the top.
As the signals are negative by construction, the sum pulse should be a negative pulse and by definition ΔV and ΔH should be negative for a left and top beam deviation.
The A, B, C and D names for analog modules inputs and modules outputs names have been chosen arbitrarily.

BPM cabling:



Δ1=A-C=ΔH
Δ2=B-D=ΔV

BPI cabling:



Δ1=A-C=V1-V4
Δ2=B-D=V2-V3

b) <u>Analog module features: attenuators, gains, compensations and calibrations</u>:

The *attenuator, gain and calibration* options are selectable from a control console in the "*specialist requirements*" application (cf. section 4).

Analog module power supplies: ***+6V; -6V; Ground.***
These power supplies and controls are provided by its corresponding Digital Front-End board using a 12 conductors cable (see chapter 3-2 for references and cabling).

After the 50Ω current to voltage conversion, the analog module performs two differences and one sum with the 4 input voltages. A gain is applied on differences and on sum before switching these signals on two selectable output types: three 50Ω single ended SMA outputs or one RJ45 100Ω differential outputs.
Total analog chain voltage gains, from 50Ω conversion to differential 100Ω output depends on the place in the accelerator and on the type of pick-up used.

The differences are named ***Δ1= A-C*** and ***Δ2=B-D***. The sum is ***Σ=A+B+C+D***.
In these notations, the analog gains do not appear.

BPM pick-up with analog preamplifier module.
RF SMA-SMA cables.

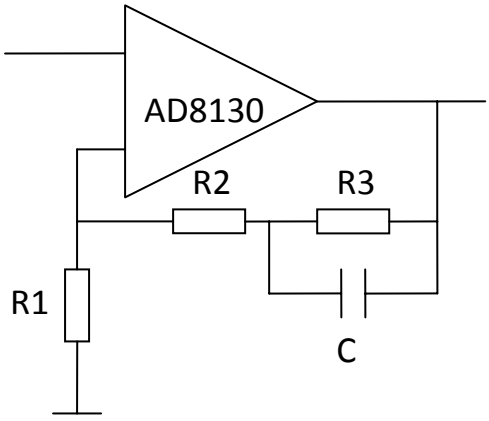
Attenuators, gains:

As the current in Combiner Ring is higher than in the lines before and BPI transfer impedance is higher than BPM too, an input attenuator stage has been implemented. It is ON/OFF switchable using ***0-3,3V*** logic levels. It is ***OFF*** for a high logic level.
The attenuator is a symmetric 50Ω T type.
The ON attenuation is ***-22dB***. Its state at rest is attenuation ***ON*** to prevent unconnection problems.

Two dynamic ranges can be selected: ***High gain*** and ***Low gain***.
The high/low gain ratio is a factor ***10*** in Combiner Ring and ***4*** for TL2 to the end of the lines. ***High gain*** is selectable using a high logic level ***3,3V***.
Low logic levels are ***0V*** (ground).

Compensation stages:

Due to pick-up low cut-off frequency, the signals are drooped after the rise edges. The solution to avoid these deformations is to implement a zero compensation in the input stage by the use of a capacitor in its feed-back:



There are several sets of values, depending on the place of the pre-amplifier in the machine (gain) and depending on the type of the pick-up (low cut-off frequency):

TL1; BPI: Sum: R1=R2=200Ω, R3=22kΩ, C=2nF.
Differences: R1=R2=200Ω, R3=22kΩ, C=1,5nF.

CR, TL2; BPI: Sum: R1=100Ω, R2=300Ω, R3=22kΩ, C=10nF.
Differences: R1=100Ω, R2=300Ω, R3=22kΩ, C=6,8nF.

TL2; BPM: Sum: R1=560Ω, R2=560Ω, no filter.
Differences: R1=560Ω, R2=560Ω, R3=5,6kΩ, C=47nF.

TBTS; BPM: Sum: R1=100Ω, R2=560Ω, no filter.
Differences: R1=100Ω, R2=560Ω, R3=5,6kΩ, C=47nF.

The input amplifier used to perform sum and differences is the Analog Devices AD8130 (or AD8129 for gains>5) because of its high CMRR. CMRR is an important specification because it limits directly the precision of the measurement.

Calibrations:

The analog module allows to direct calibration current pulses from one input to one of the two outputs using RF 50Ω adapted relays. Two calibration selection signals are provided to the module and named ***CAL+*** (upper left electrode) and ***CAL-*** (lower right electrode).
These signals are complemented (low level active) because they drive open collector transistors in series with relays.
Calibration current pulses are produced by a generator located in the upstairs gallery. They are directed to a distribution board in the crate. This distribution board directs the current pulse to the corresponding analog module.

2- Digital Front-end board.

The digital front-end board is designed to be the closer as possible to the pick-up/analog pre-amplifier to limit the analog signal cable lengths.
The aim is a cable cost reduction thanks to a local digitalization and a data transmission on a specific network. The development of a specific board for this acquisition also allows the reduction of the cost by channel.

2-1 Sampling part – architecture.
(cf. annex 1)

Due to desired high sampling rates and high dynamics (500Msps-12bits), and because the acquisition is not a free running digitalization but a fixed number of samples window, we opted for the use of an analog memory and then a down-rated frequency sampling.
The ***12 bits*** analog memory is free-running with a sampling rate of ***512MHz*** (a sample every ~1.95 ns). A timing signal is received and processed by the FPGA and allows to freeze the analog memory samples.
Then, a ***14bits-800kHz*** ADC digitizes the memory samples. The data is collected by the FPGA and sent on the network thanks to the ***SPECS*** boards.

- ***Analog memory (SAM):*** [3]

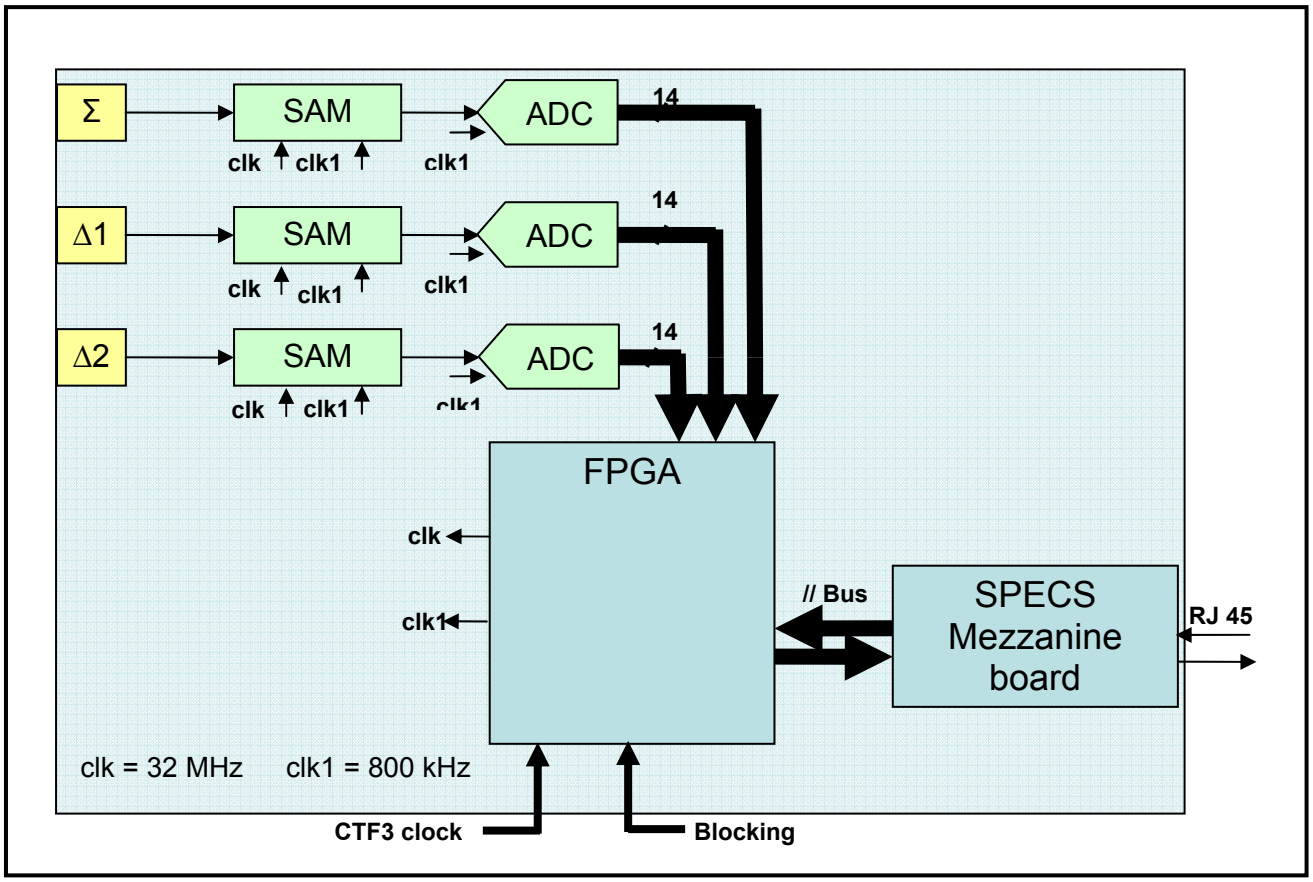
The SAM is an ASIC developed by CEA in Saclay. It's a 16x16 rad-hard analog memory, so a ***256*** samples memory.
There are 2 differential input channels per chip, so there are 2 chips for 3 analog channels. The writing clock is running at a frequency of 32 MHz and is internally multiplied by 16 to obtain a sampling frequency of 512 MHz.
The sampled data represents a time "window" of ***256*1/512.E6=500ns***.
AD8138 differential amplifiers allow the differential reception of analog signals and a common mode voltage shift.
SAM's differential analog input range is ***0,5V - 2V*** and the common mode voltage is ***1,25V***. To obtain this common mode voltage, we use the ADC voltage reference output.
To be noticed: the SAM's output resistance is 500Ω; so it is to be taken into account for the next stage input impedance.

- ***ADC:***

After analog memories read-out, the cells are sampled by a ***14bits-800kHz*** ADC ***LTC1419A***. ***AD8138*** differential amplifiers adapt the levels to the ADC input range: ***-2.5V / +2.5V*** with a gain of 3.
There is a half phase shift between the SAM read clock signal and the ADC sampling clock signal to have data as stabilized as possible.Then, data is stored in the FPGA and sent to the control computer thanks to the SPECS mezzanine board.

- ***FPGA:***

  An ***Actel ProAsicplus APA300*** is used to control all the board. Inputs and output levels are 3,3V and core level is 2,5V. It receives timing signal from the machine and processes it before sending it to the SAM.
  It allows to tune the delay and so to fit the pulse in the reading window.
  A 32 MHz is distributed to the SAM as a write clock.
  The sampling 800 kHz ADC sampling clock is generated by the FPGA and is also distributed to the SAMs to make them work synchronously.
  Data from ADCs is stored in three internal 256x16 RAM memories. They are transferred to the control room when the SPECS mezzanine receives the read signal from the SPECS master board. The data is sent at 1,11MHz on the network.
  This clock is also tuned inside the FPGA.
  See annex 4 for FPGA acquisition sequence.



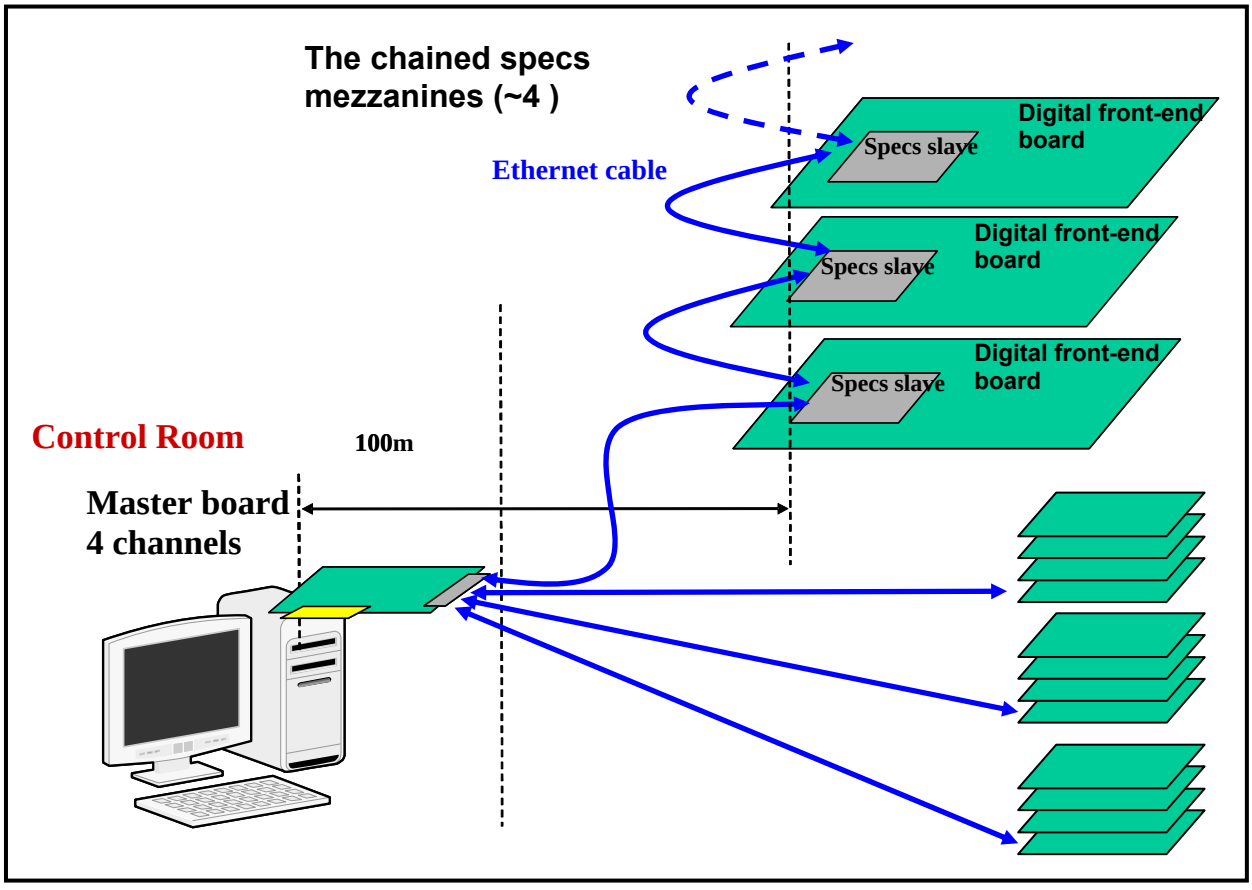
2-2 Controls – power supplies.

DFE provides power supplies to its corresponding analog module (+6V, -6V, ground) and controls using a 12 pins burndy connector on front-panel (see 3-2-a for pin-out). The controls are performed by two open collector transistors for Cal+ and Cal- and two 0-3,3V drivers for attenuator and gain switching.
An arbitrary output signal is also available via a lemo socket on front panel to control the calibration pulse switching on the distribution board.

2-3 SPECS network.

The SPECS network has been developed by LAL (Laboratoire de l'accélérateur linéaire) for LHCb [4] [5]. It is a Rad-Hard network system. The SPECS network is based on 1 mezzanine fixed on the DFE, working as a slave and a PCI card in a computer far away from the beam and working as a master.
This system is used to control the boards from the control room and to get back data after sampling.

As it is possible to chain mezzanines together on the same master port, we use only one network cable by crate. We foresaw to chain a maximum of 4 boards because the high cable length can limit the transmission in some case (up to 100m).
A master PCI board can concentrate up to 4 mezzanine networks.
Each mezzanine board of a chain owns its own address.



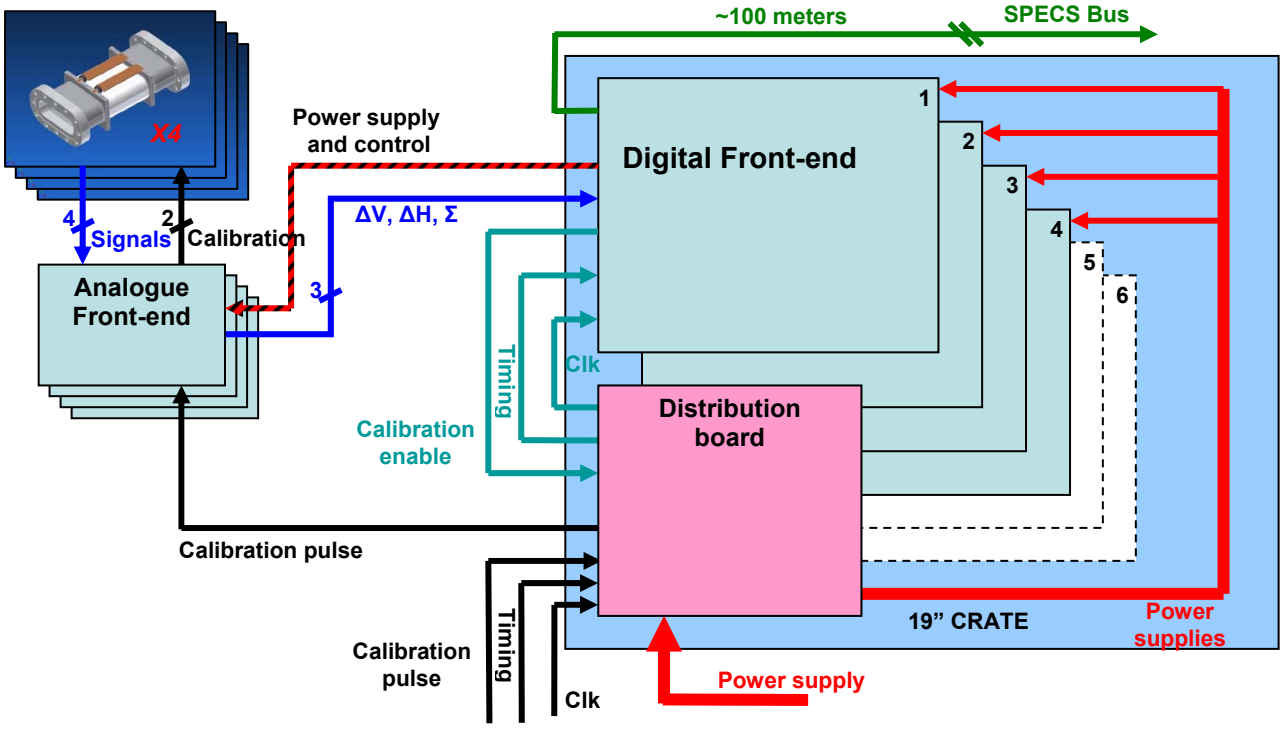
SPECS protocol, is a 10 Mbit/s serial link designed for the configuration of remote electronics elements. SPECS is a single master multi-slave bus, designed to allow a simple, fast and cheap means of communication between electronics systems.
The serial packet is 16bits long: 14 ADC data bits + 2 mask bits. Each slave sends 3 *256*16=12288bits ≈ 1,5ko every 200ms, so a ~7,5ko/s rate.
The maximum data rate between slave and master boards is 1Mo/s.

3- Crate architecture and timing distribution.

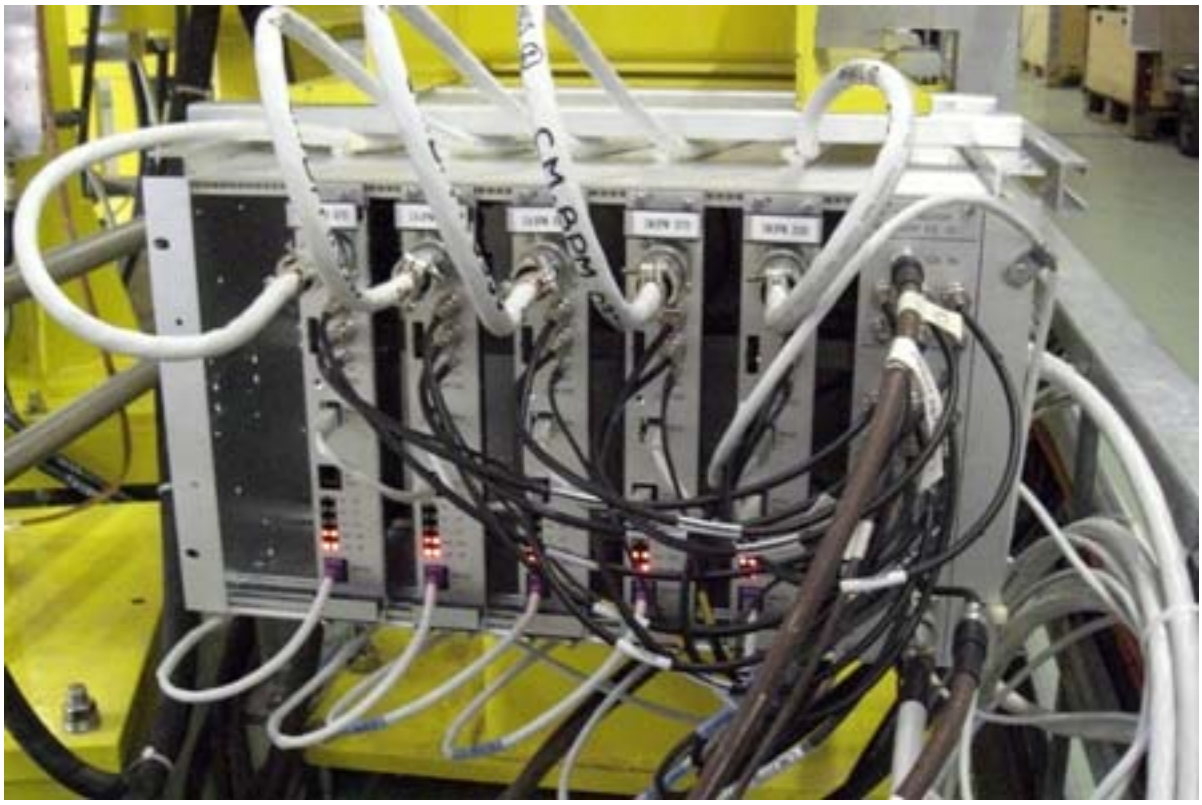
3-1 Acquisition architecture.

As the pick-ups are distributed on the lines, crates have been also distributed to acquire signals. The reasonable limit that we fixed on the number of DFE to be chained in a crate was 4.

So, pick-up digitizers are grouped by 4 in the crates. DFEs need power supplies, timing control (pulse synchronized on the beam) and machine clock. They also control the calibration switching.
The distribution board receives the power supplies, the timing pulse, the machine clock and the calibration pulse from the upstairs gallery. It distributes the signals to the DFEs and analog modules (calibration pulses).
A DFE provides the power supplies to its dedicated analog module and receives the 3 signals, sum and differences (see section 3 for pin-out).



As the aim of the system is to digitize the signals the closer as possible to the beam, the parts are subjected to radiations. The levels are not known and are impossible to foresee.
So the most part of components have been selected regarding their radiation hardness with qualification references or traditional use in radiation environment.



Uranus crate in CLEX with 5 chained DFE boards and one distribution board.

3-2 Distribution Board.

Distribution board performs the following functions:

- Reception, adaptation and distribution of the machine clock.
- Reception, adaptation and distribution of the machine timing.
- Reception and distribution of the power supplies.
- Reception and distribution of the calibration current pulse.

Clock and timing signals are received on 50Ω cables coming from the gallery. They are distributed from distribution board front panel to DFE front panels using BNC cables. For each signal, the board allows one 50Ω adapted input and six 50Ω adapted outputs.
The power supplies are received on the front panel using 12 conductors cables from the gallery and are distributed in the crate using cables with 3 pins molex connectors.
Calibration current pulse is generated in the gallery by a pulsed current generator triggered on the machine timing.
All these signals are transmitted to the crates in the accelerator.

- ***Machine clock distribution:***

Machine clock is a 96MHz sine signal, 50Ω adapted.
It is buffered before distribution to the DFE boards.
An attenuator can be set to the right value to fit the signal dynamic to the DFE input range. As the DFE input stage is a comparator stage, it allows to transform a sine signal with variable amplitude (in a limited range) in a 3,3V pulsed clock.

DFE standard input level is ***0dBm***.
In CLEX, reception levels are about 0dBm due to attenuation on cables, so attenuator is not used (0dB).

- ***Machine timing distribution:***

Machine timing is a variable low frequency pulsed signal, 50Ω adapted.
Typically, the frequency is about ***1Hz***, the pulse length is about ***1µs*** and the rising edge about 2ns.
It is buffered before distribution to the DFE boards. DFE input levels are 0-3,3V.
An attenuator can be set to the right value to fit the signal dynamic to the distribution components.

In CLEX, reception levels are about ***0-18V***, so a ***15dB*** attenuator is implemented at the distribution board input.

- ***Power supplies distribution:***

Power supplies are received from the gallery on a 12 conductor cable. Voltages are +6V, -6V and ground. Several conductors are used for each voltage to reduce the resistance on long cables and so limit the voltage drop (see 3-2 b for pin-out and references).
It is to be noticed that cables type coming from the gallery are the same for Combiner Ring analog modules and distribution boards but remains incompatible.
Due to unavoidable voltage drops on long cables, it is mandatory to trim power supplies levels in the gallery to obtain the right levels in the crate. The use of voltage regulators in the different systems allows a coarse adjusting.

Power consumptions:

Analog modules:
+6V: 0,7A; -6V: 0,4A; so 6,6W for a maximum consumption
(attenuators ON and calibration ON).
Digital Front-End:
+6V: 1A; so 6W.
Distribution:
+6V: 0,3A; so 1,8W.

For a maximum 6 DFE crate with 6 analog modules and one distribution board:
+6V: 10A; -6V: 2,4A; so a 75W maximum consumption.

Note: a crate can contain 6 DFE boards + 1 distribution board with several network cables.

- ***Calibration current pulse distribution:***

The current pulses are transmitted on 50Ω BNC cables to the distribution board front panel of each crate. Pick-ups, analog modules and distribution board connectors are SMA, so a BNC to SMA adapter is necessary at the reception.
The distribution board allows one input and six distributed outputs.
As the signal is a 2A current pulse, the distribution is performed using RF relays.
They are switched ON using a control DC signal performed by its corresponding DFE board. It is transmitted by the use of lemo cables from DFEs front panels to distribution board front panel.
It is to be noticed that the commutation of several relays at the same time divide the distributed current to the pick-ups. So, regarding adaptation consideration, it is recommended to switch only one relay by one.

3-3 Cables, pin-outs.

a) Analog module cables:

- ***power supplies and controls:***

This cable provides power supplies and controls from DFE front panel to the analog module. 12 conductors, shielded, CERN reference: 04.21.52.124.4.

Analog module cable end: burndy cable connector, 12 sockets, burndy reference UTO61412S21T, CERN reference 09.31.05.236.3.
DFE cable end: burndy cable connector, 12 pins, burndy reference UTO61412P21T, CERN reference 09.31.05.232.7.

Analog module front panel connector: 12 pins, burndy reference UTO01412P21T, CERN reference 09.31.05.132.0.
DFE front panel connector: 12 sockets, burndy reference UTO01412S21T, CERN reference 09.31.05.136.6.

Pin-out: several conductors can be used for the same signal.

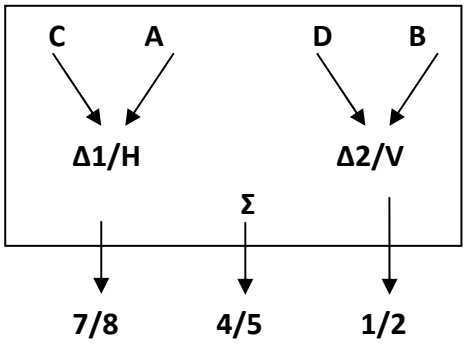
Burndy pin number	Pin ref. on analog module and wire color.	Signal
1	P1 red	+6V
2	P1 red	+6V
3	P1 red	+6V
4	P2 blue	-6V
5	P2 blue	-6V
6	P6 orange	Analog gain selection
7	Gnd black	Ground
8	P3 yellow	Cal+ complemented
9	Gnd black	Ground
10	P4 brown	Cal- complemented
11	P5 violet	Attenuator selection
12	Gnd black	Ground

- ***Pick-ups to analog modules cables:***

Calibration current pulse is transmitted from distribution board to analog module using a RG58 50Ω cable with SMA connectors. The lengths of the 4 cables corresponding to the 4 electrodes signals have to be adjusted to be the same in order to limit delays between acquired signals (~1mm).

Output signals can be read on a single ended output: SMA sockets.
A jumper can be placed in the analog module to select the output type of transmission.
The transmission between analog module and DFE is performed with three differential twisted pairs, using a cat.6 network Kerpen S/FTP cable. It allows the use of RJ45 connectors.
Three combinations are possible: BPM read-out with LAPP analog module & DFE; BPI read-out with LAPP analog module & DFE; BPM read-out with CERN analog module & DFE.

Cabling:



RJ45 pin numbers

In the case of BPI preamplified by a LAPP analog module and digitized by a DFE:

Pin 1: Δ2+; Pin 2: Δ2-
Pin 4: Σ-; Pin 5: Σ+
Pin 7: Δ1+; Pin 8: Δ1-

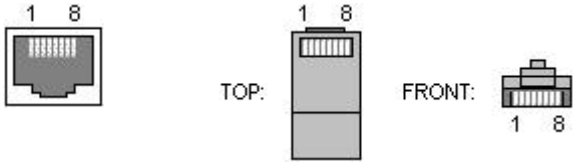
In the case of BPM preamplified by a LAPP analog module and digitized by a DFE:

Pin 1: V+; Pin 2: V-
Pin 4: Σ-; Pin 5: Σ+
Pin 7: H+; Pin 2: H-

In the case of a BPM preamplified by a CERN analog module and digitized by a DFE:

Pin 1: H+; Pin 2: H-
Pin 4: Σ-; Pin 5: Σ+
Pin 7: V+; Pin 2: V-

RJ45 pin-out : Cat.6



b) Distribution board cables:

- ***power supplies:***

The distribution board receives the power supplies from the gallery using the same cable type than the analog module: 12 conductors, shielded, CERN reference: 04.21.52.124.4.

Power supplies cable end: burndy cable connector, 12 sockets, burndy reference UTO61412S21T, CERN reference 09.31.05.236.3.
Distribution board front panel connector: 12 pins, burndy reference UTO01412P21T, CERN reference 09.31.05.132.0.

+6V: pin number 1,2,3,4,5.
-6V: pin number 6,7,8,9.
Ground: 10,11,12.

- ***Other cables:***

Clock distribution and timing distribution between distribution board and DFE are BNC-BNC RG58 cables (50cm).

Calibration enable cables between DFE and distribution are lemo single ended cables.

Calibration current pulse input/outputs are SMA connectors. This signal is received in a BNC pin connector type, so it is necessary to transform it with the use of a BNC socket to SMA pin adapter.

Network chain is performed with 15cm standard RJ45 network cables.

4- Soft implementation [6] [7] [8] [9].

Fesa client

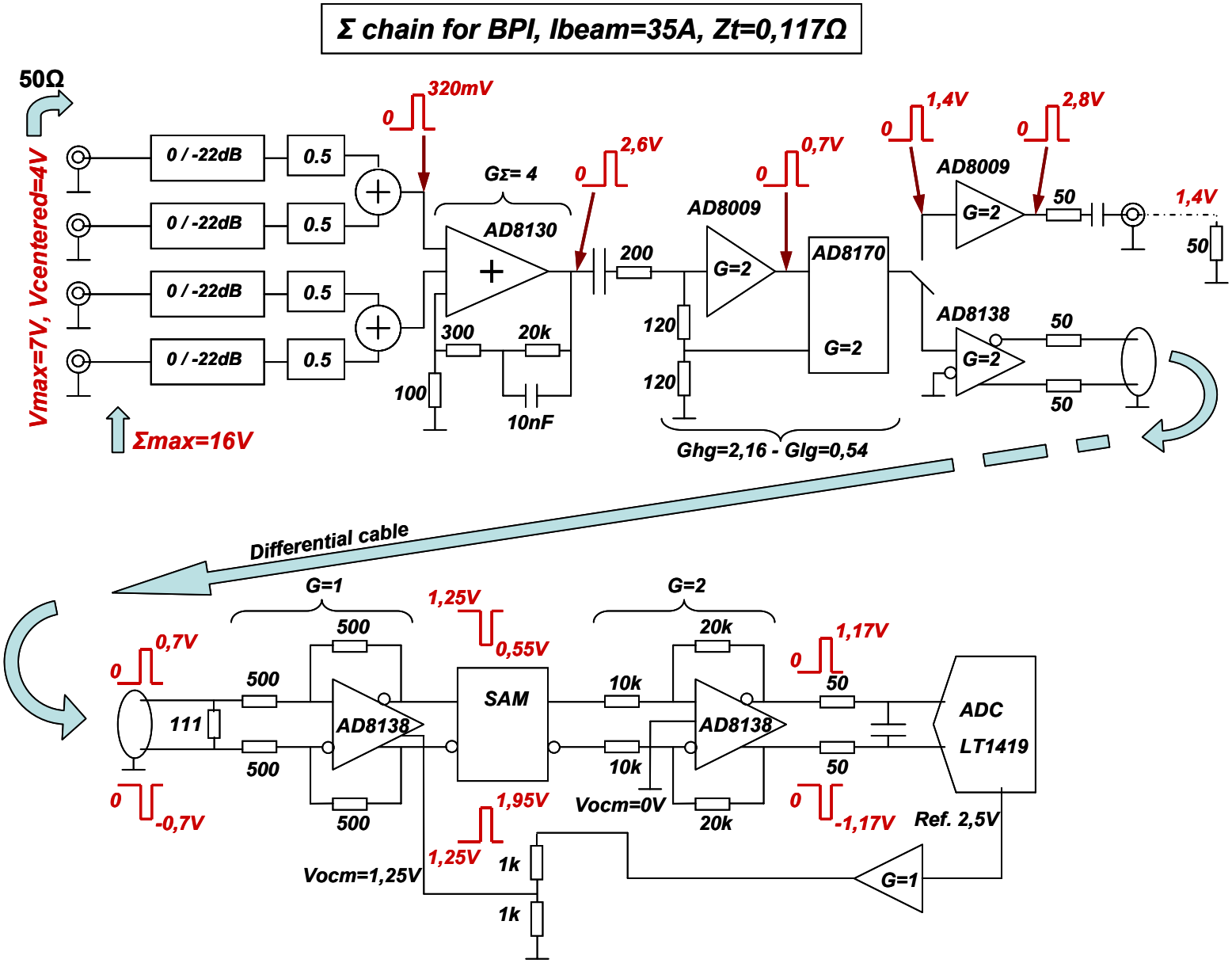
After digitalization, the acquired data is retrieved, normalized according to the BPM type and transferred to the OASIS application server by *FesaShared_M* software.
A library has been developed to communicate with the front-ends, via the SPECS parallel bus. This library is based on the PCI9030 library and driver. In addition to the data retrieval, the communication link is also used to configure the front-ends.
To implement the OASIS interface, two classes, *LappBPMScope* and *LappBPMChannel*, have been developed using the FESA framework.
They manage respectively the front-ends and the channels along with their properties. Both classes are deployed in a FESA server that processes the requests from the OASIS application server. The timing pulse used to trigger the DFEs is also linked to a FESA real-time action. This action updates the acquired values in the *LappBPMChannel* and notifies the FESA server.

The gateway is a standard rack-mountable PC running Scientific Linux CERN 4.
The motherboard has 3 PCI slots. One PCI slot is reserved for the timing receiver and the other two are used for the SPECS Master cards.

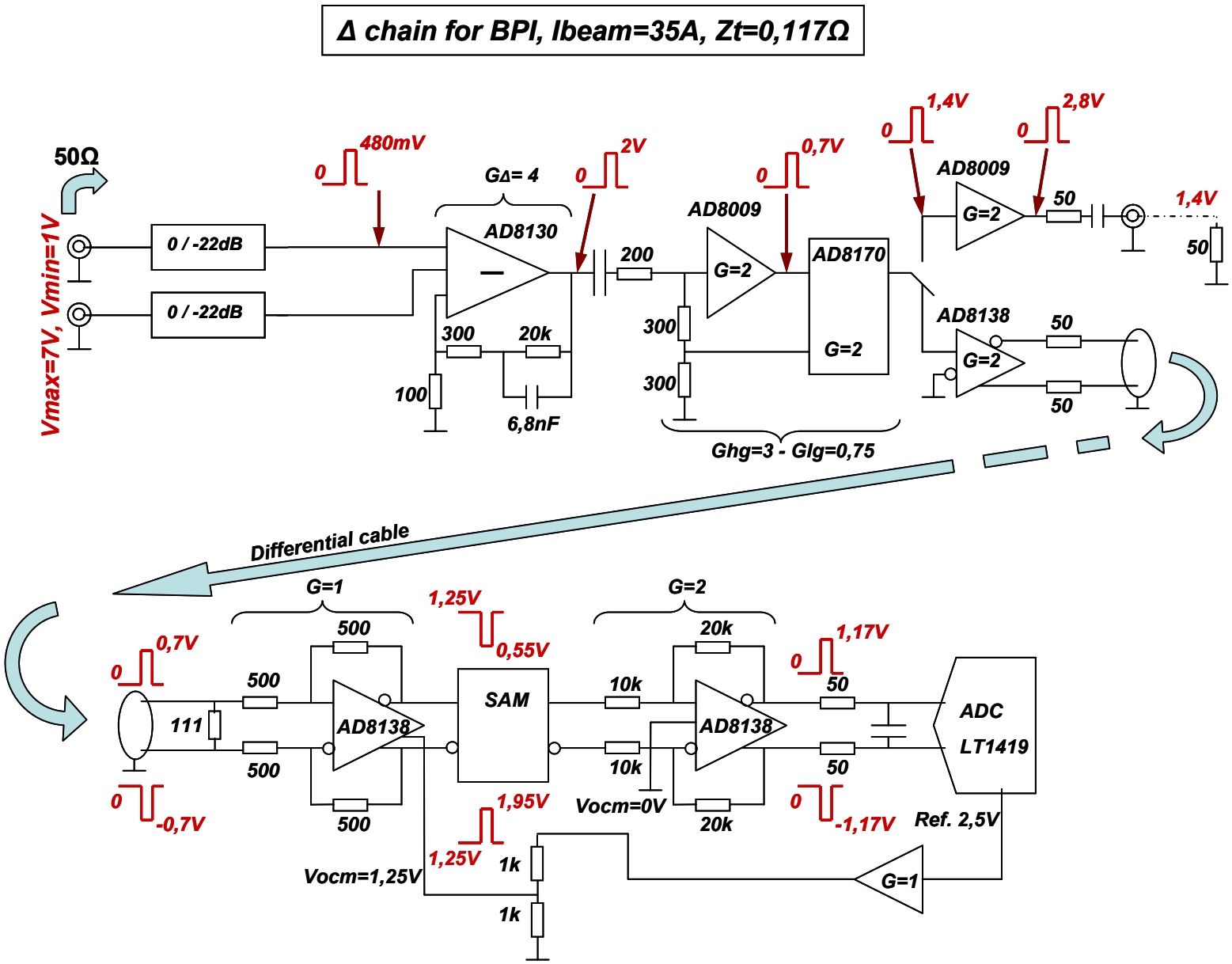
LappBpmSpecialist

Bases on japc and oasis-client java libraries, this software has been developed for BPM calibration procedure. This application allows to configure electronic font-end and can be used for maintenance operations.

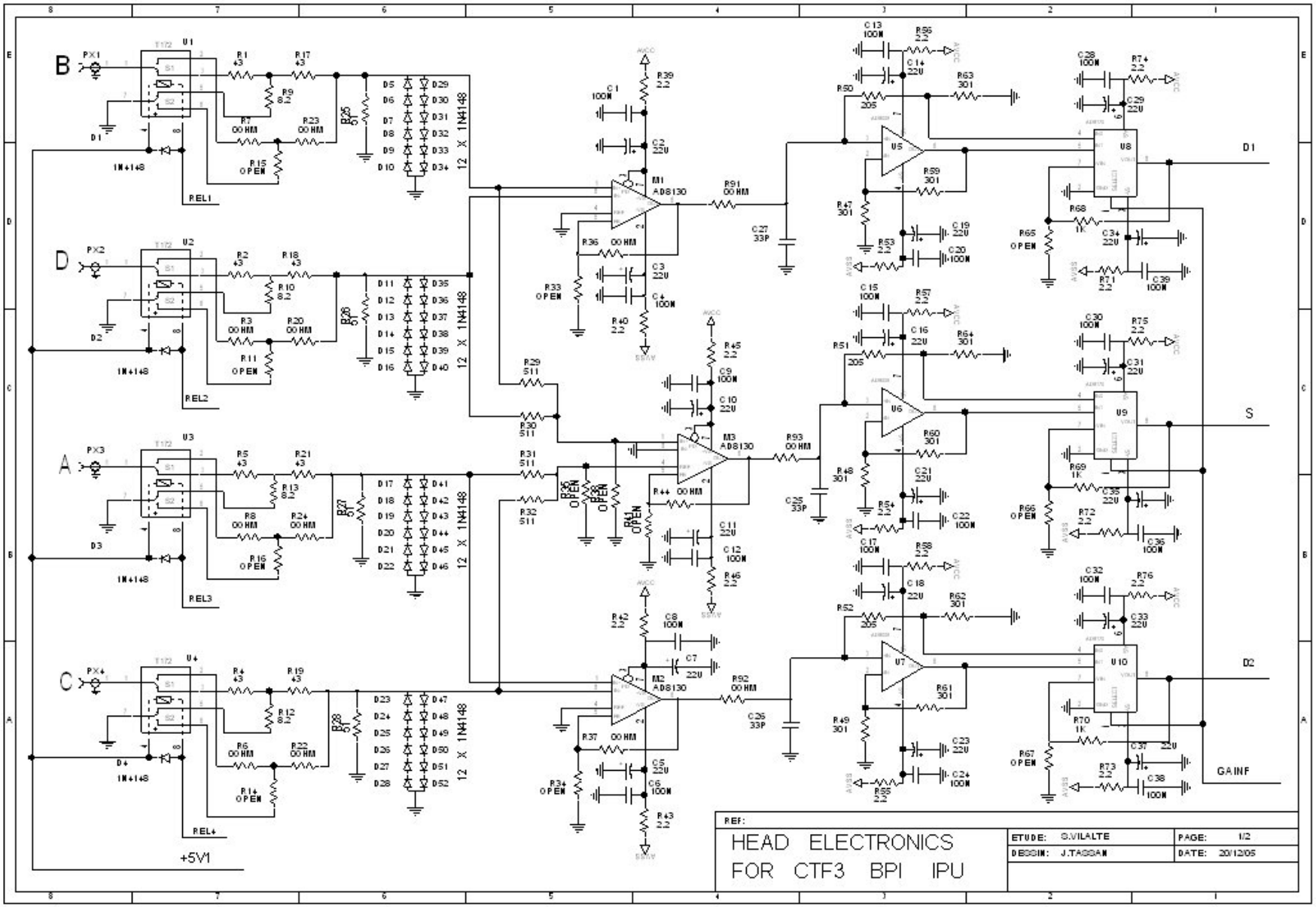
Annex 1: Σ synoptic full chain architecture and levels.



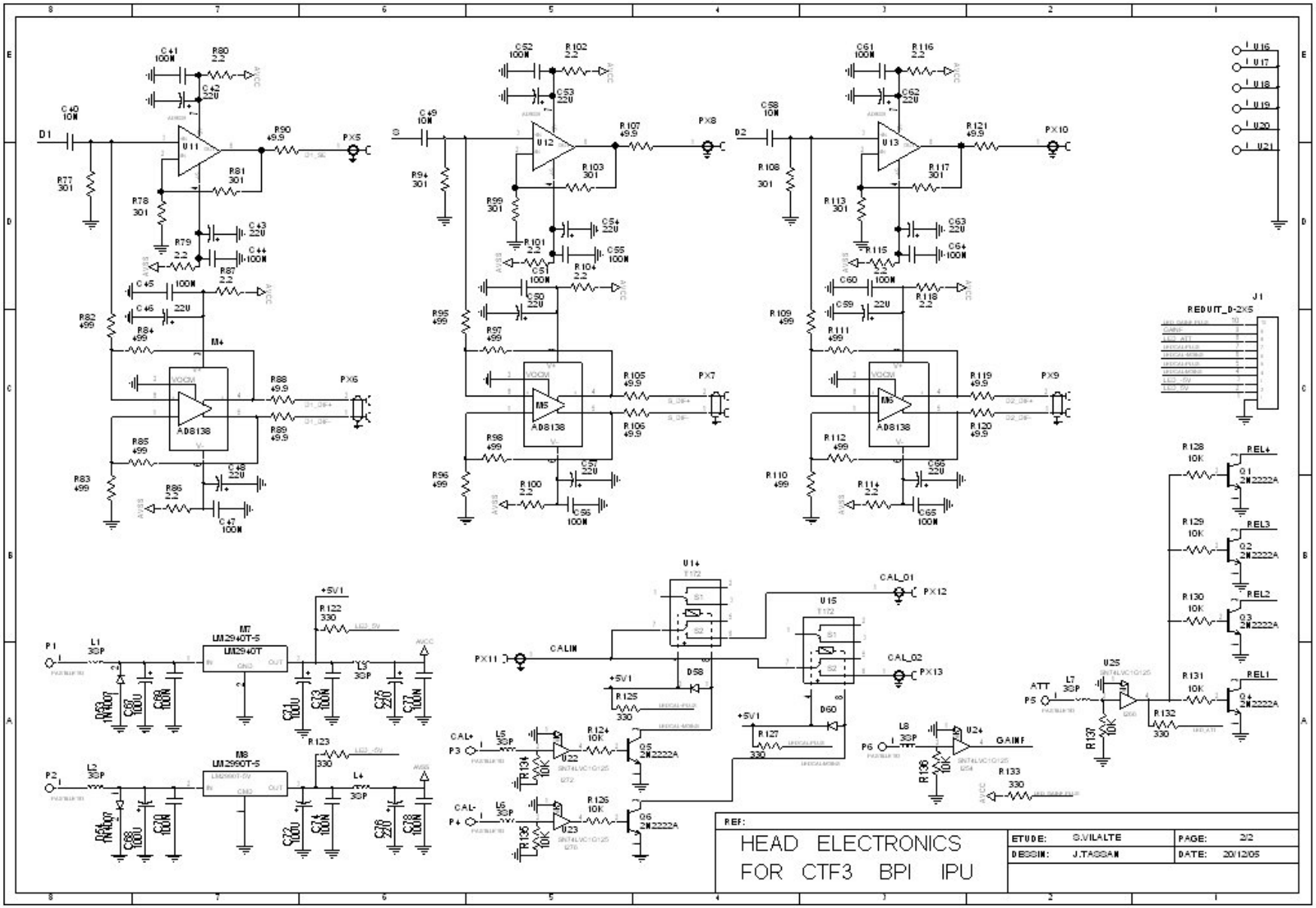
Annex 1: Σ synoptic full chain architecture and levels.



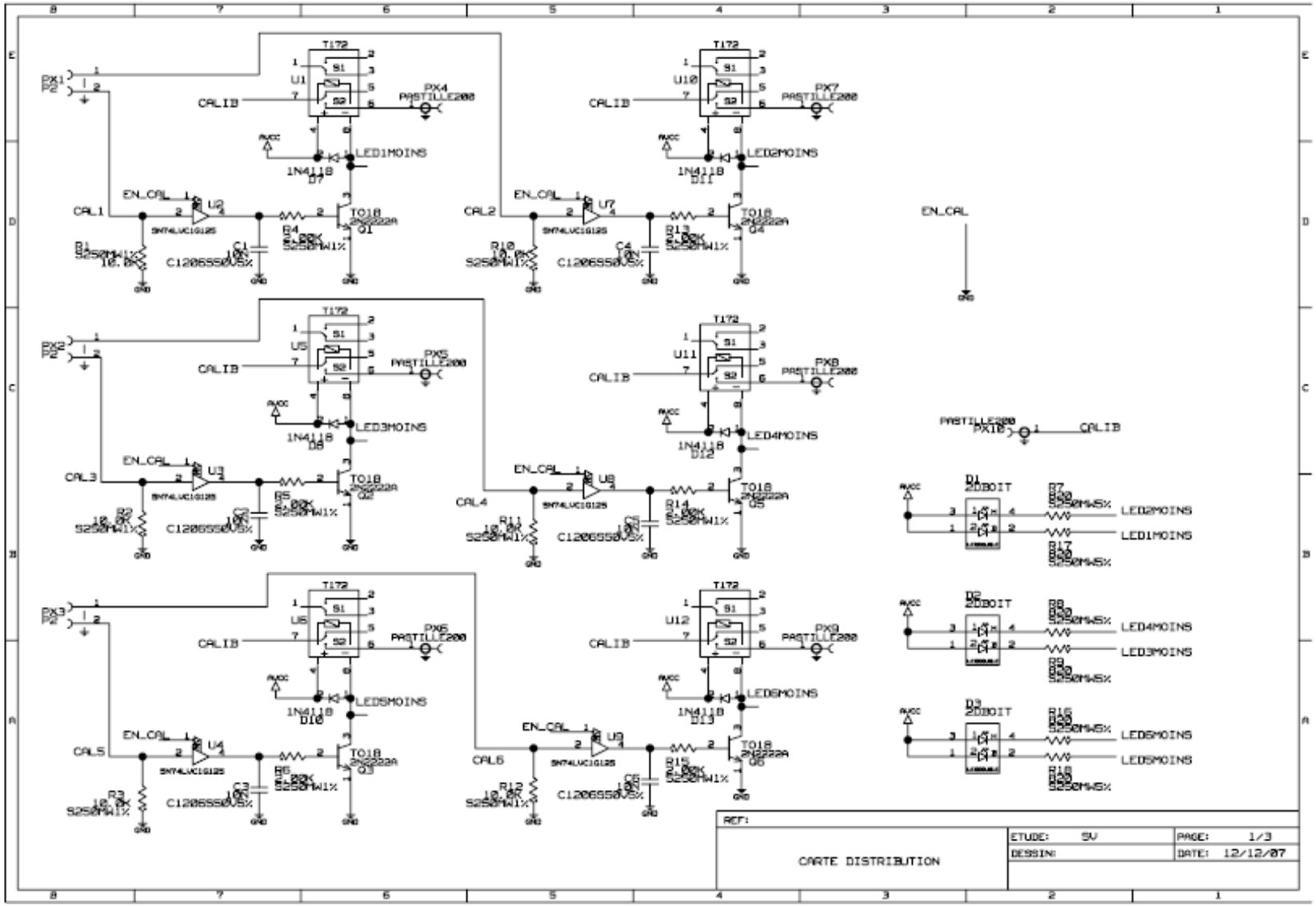
Annex 2: Analog module schematics 1/2.



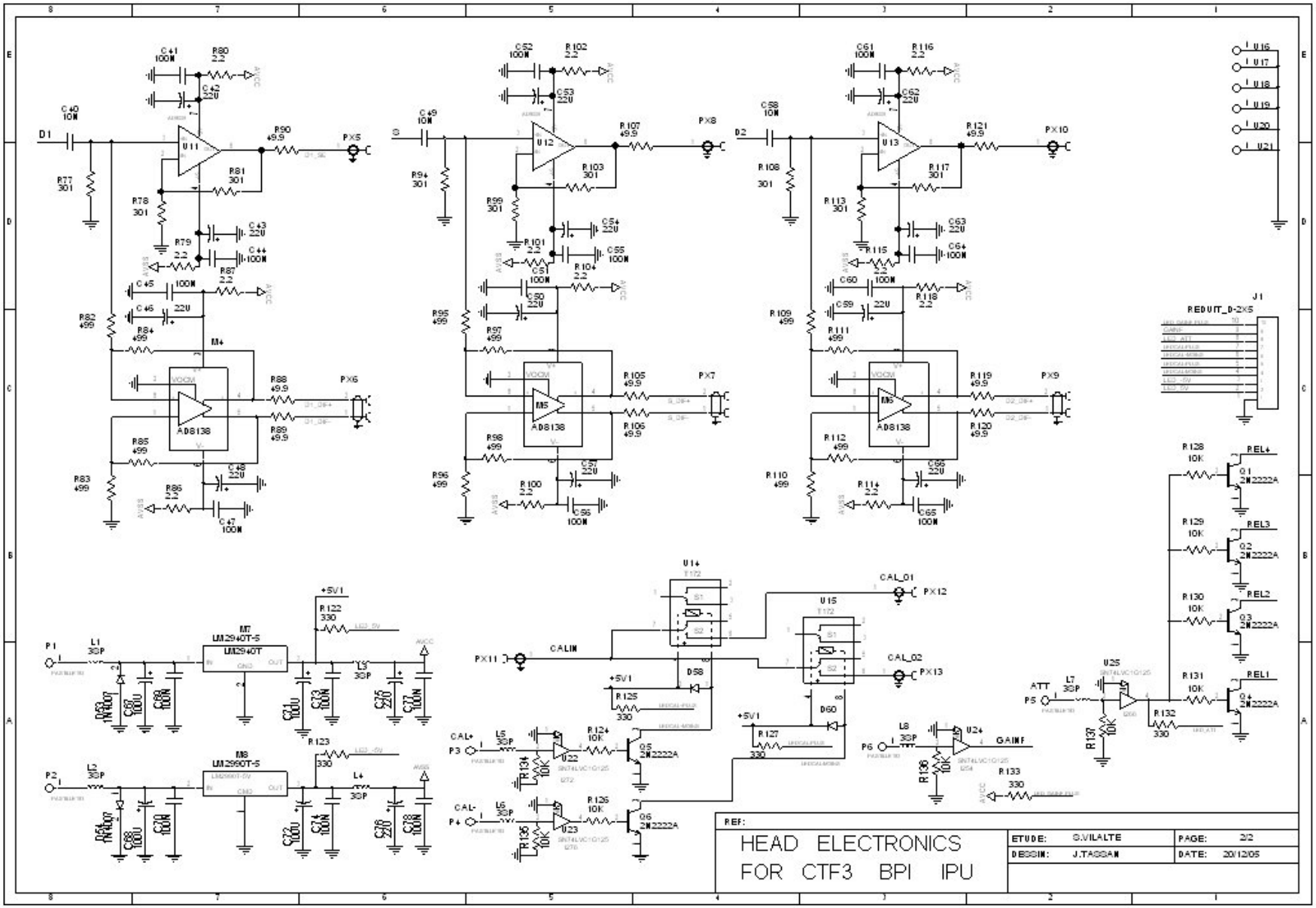
Annex 2: Analog module schematics 2/2.



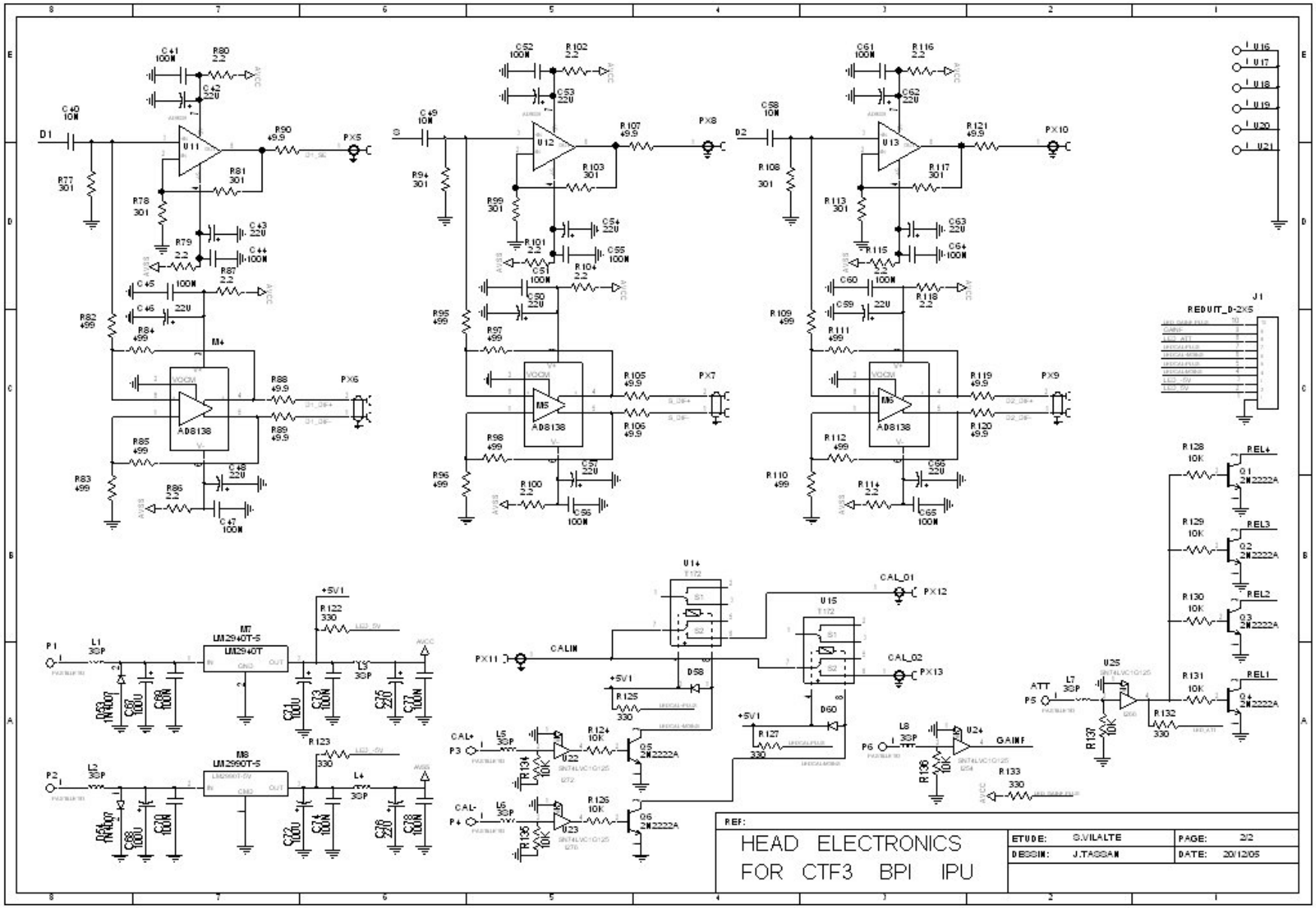
Annex 3: Distribution board schematics 1/3.



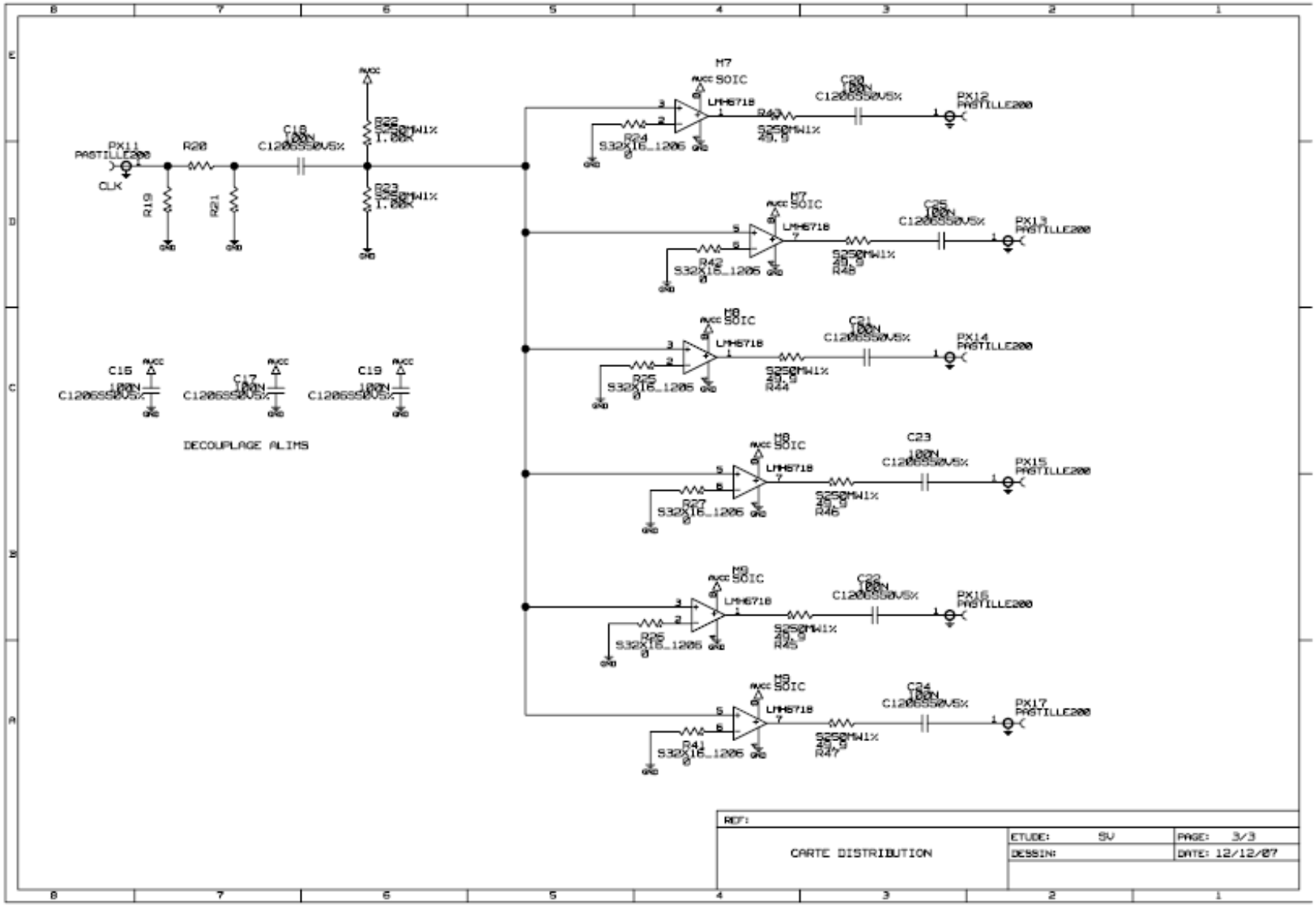
Annex 3: Distribution board schematics 2/3.



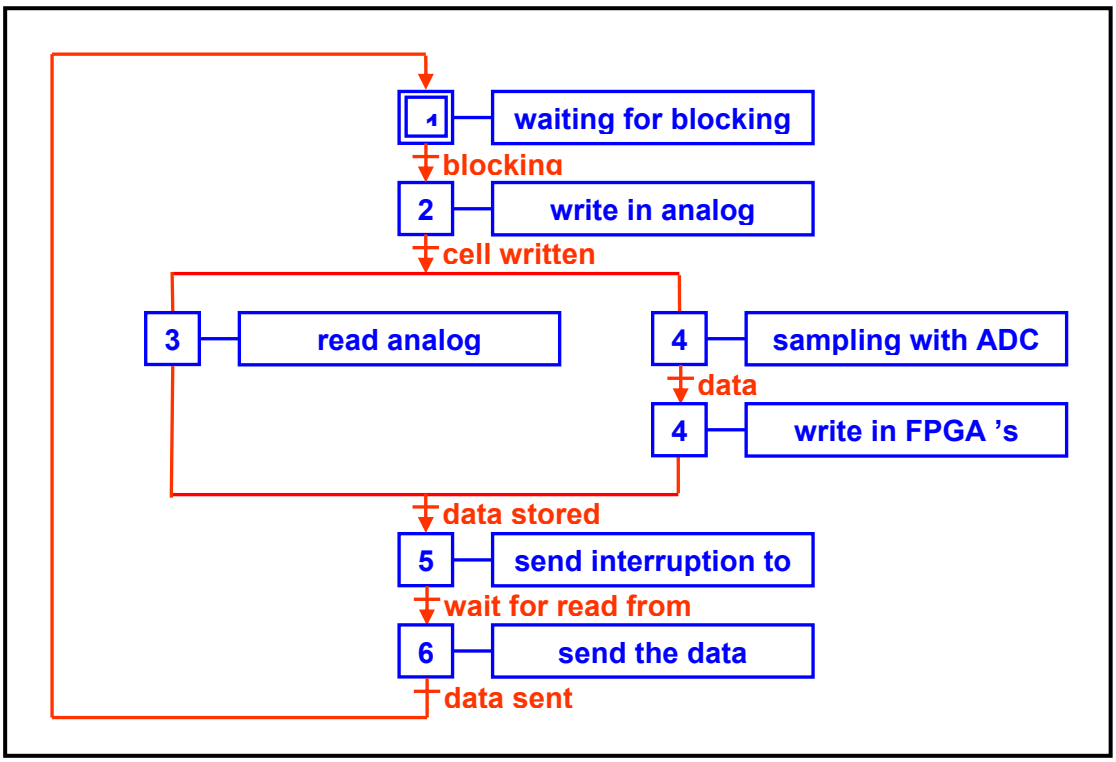
Annex 3: Distribution board schematics 3/3.



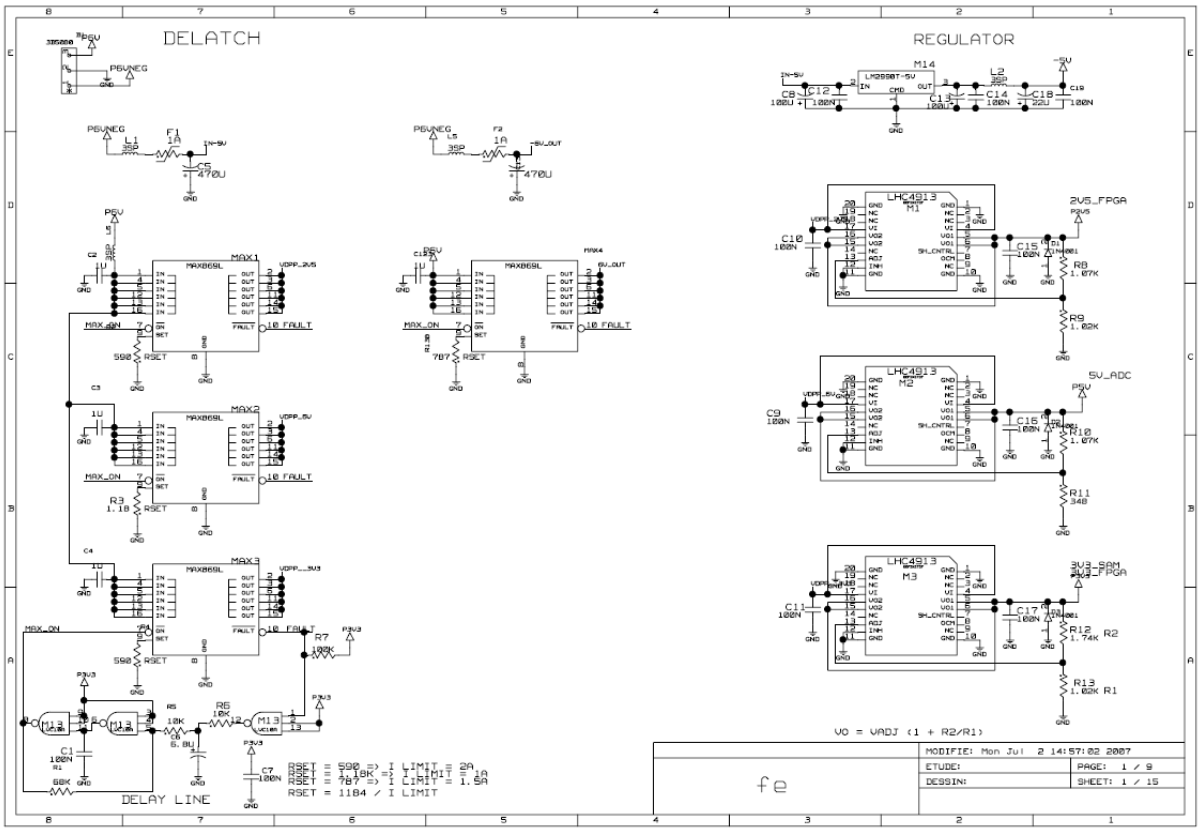
Annex 3: Distribution board schematics 3/3.

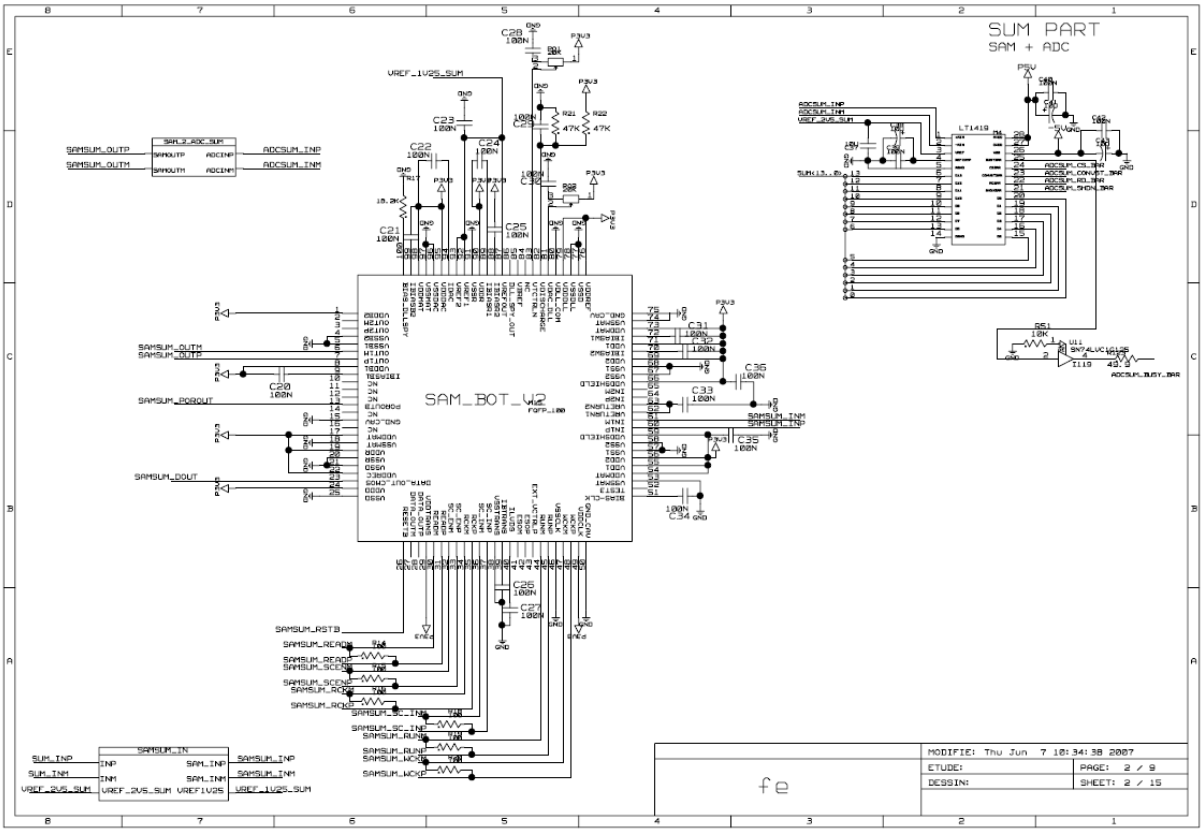


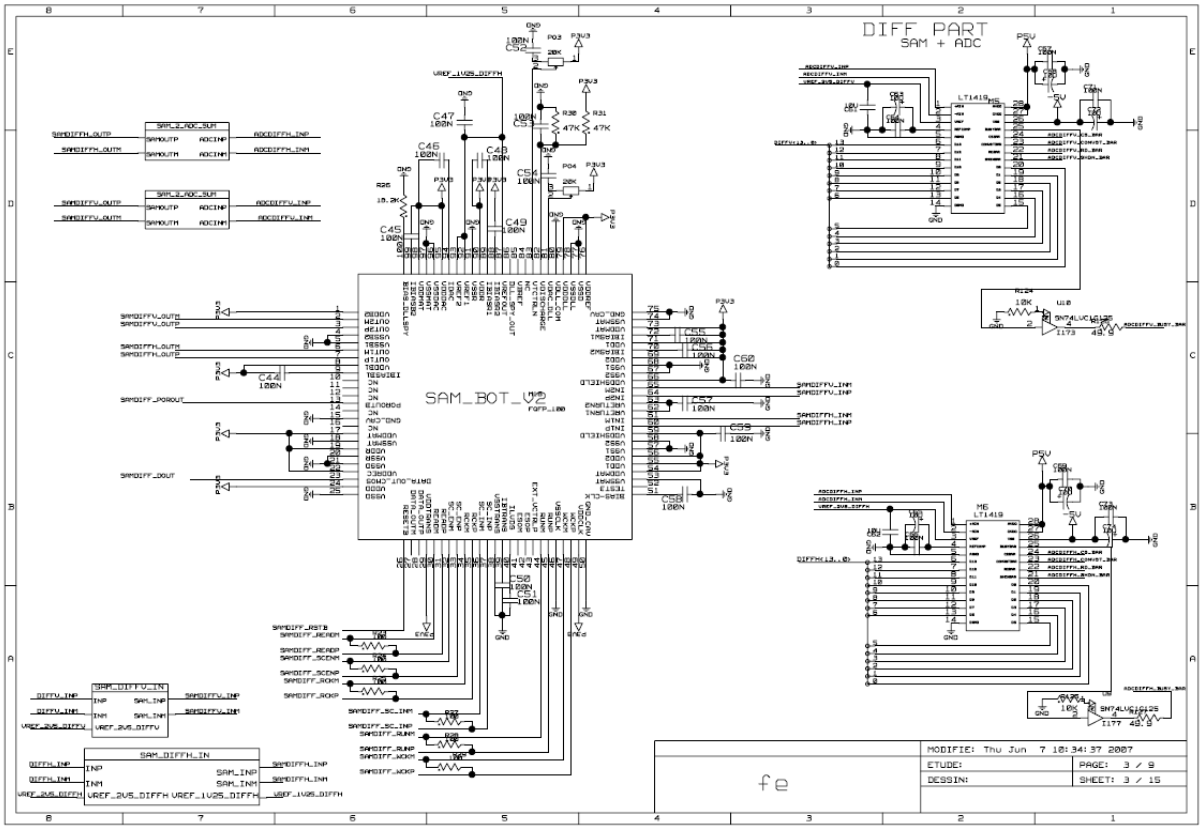
Annex 4: DFE FPGA acquisition sequence.



Annex 5: DFE schematics.



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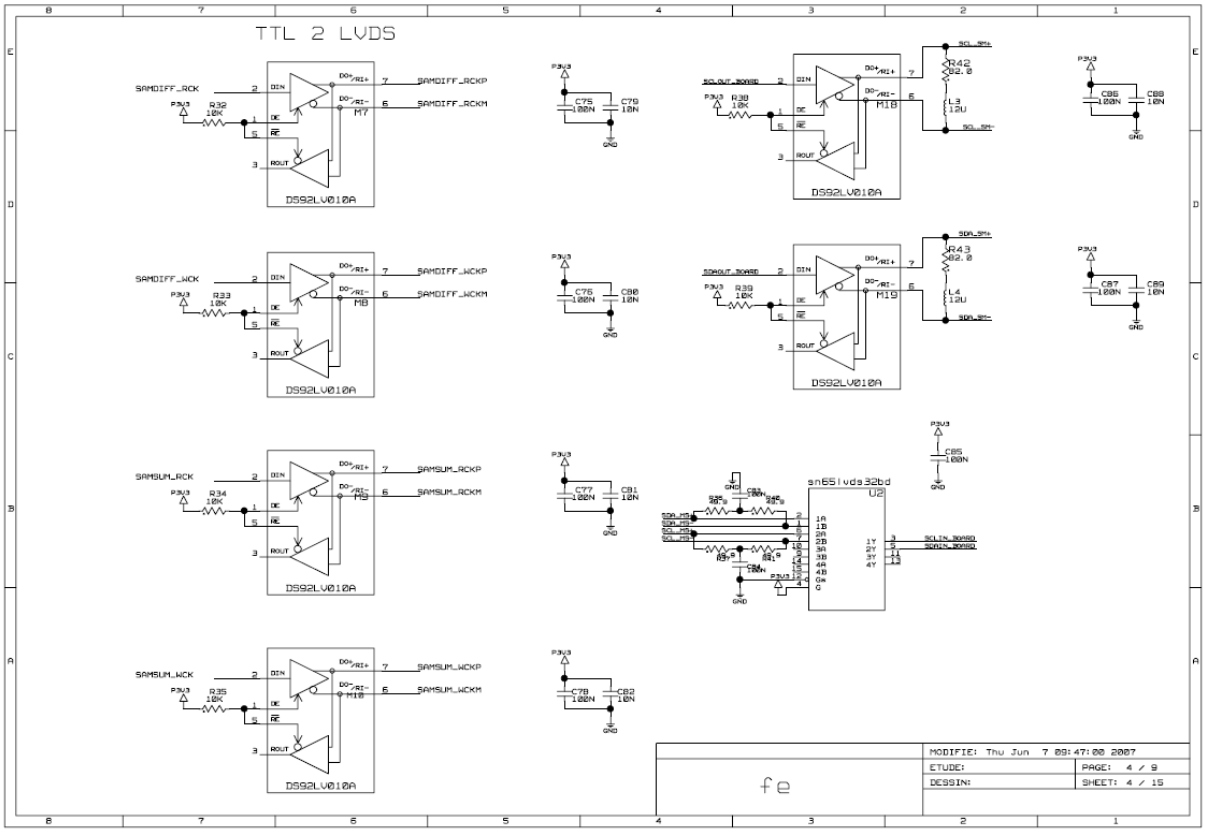
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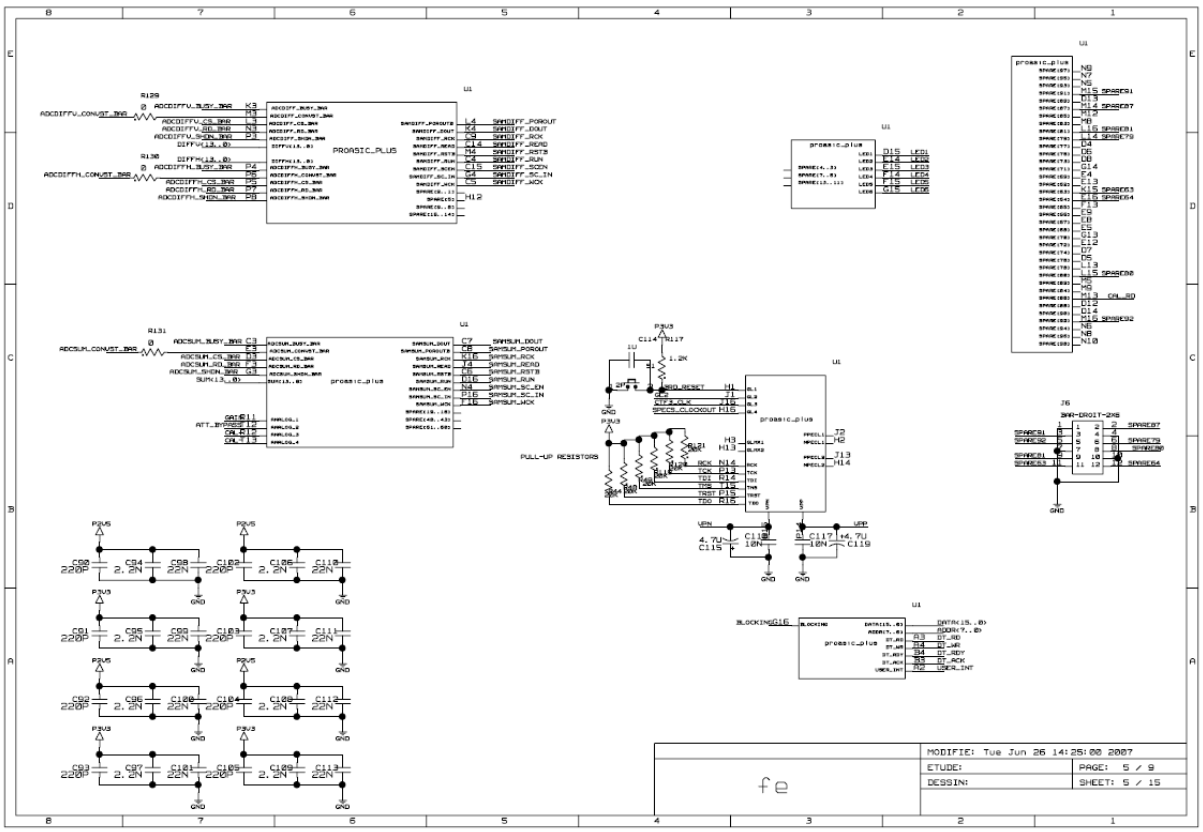
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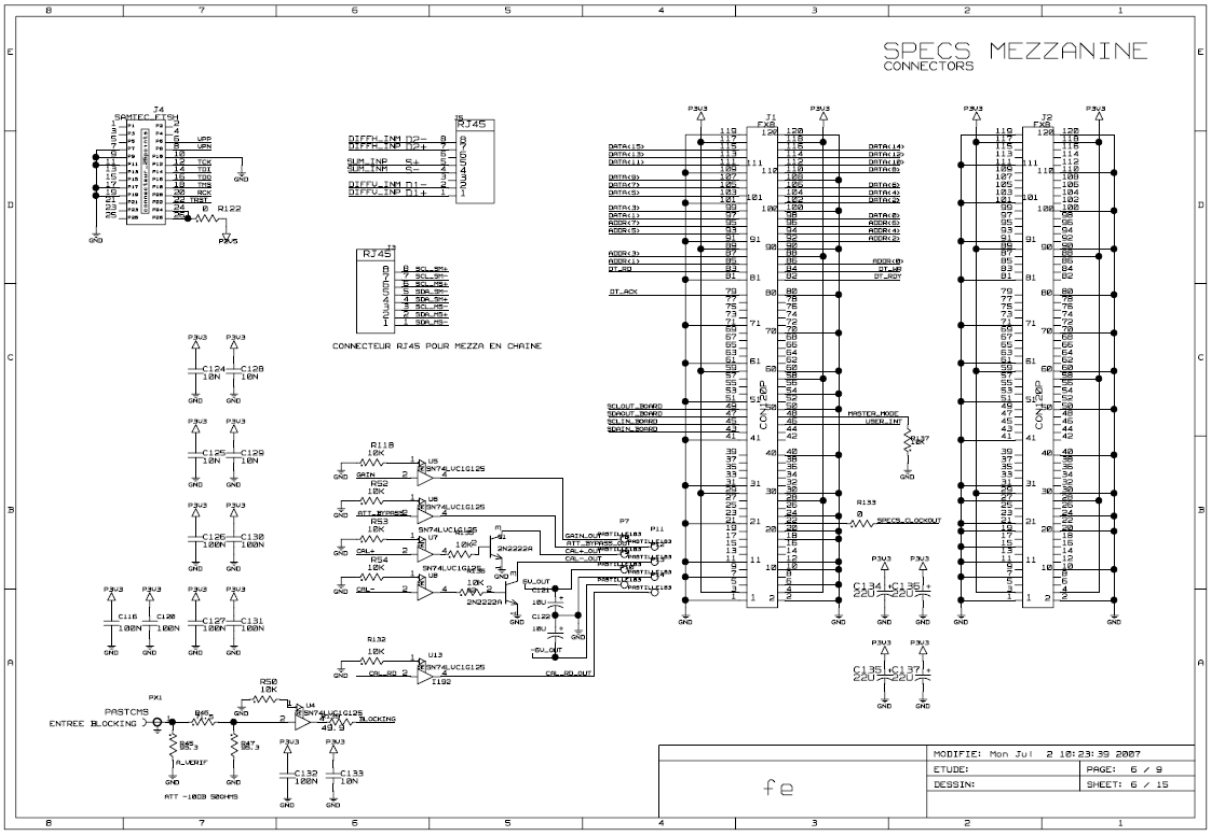
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CONNECTEUR RJ45 POUR MEZZA EN CHAINE
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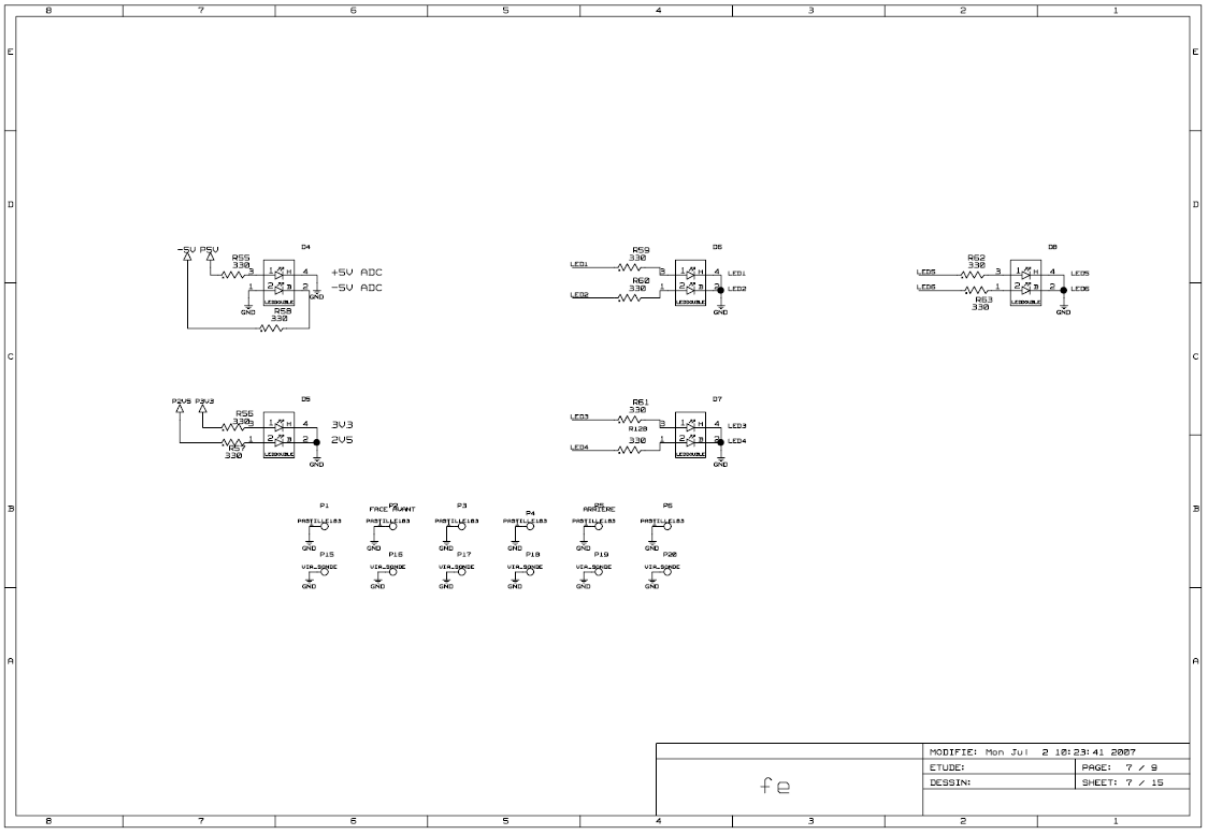
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+5V ADC
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3V3
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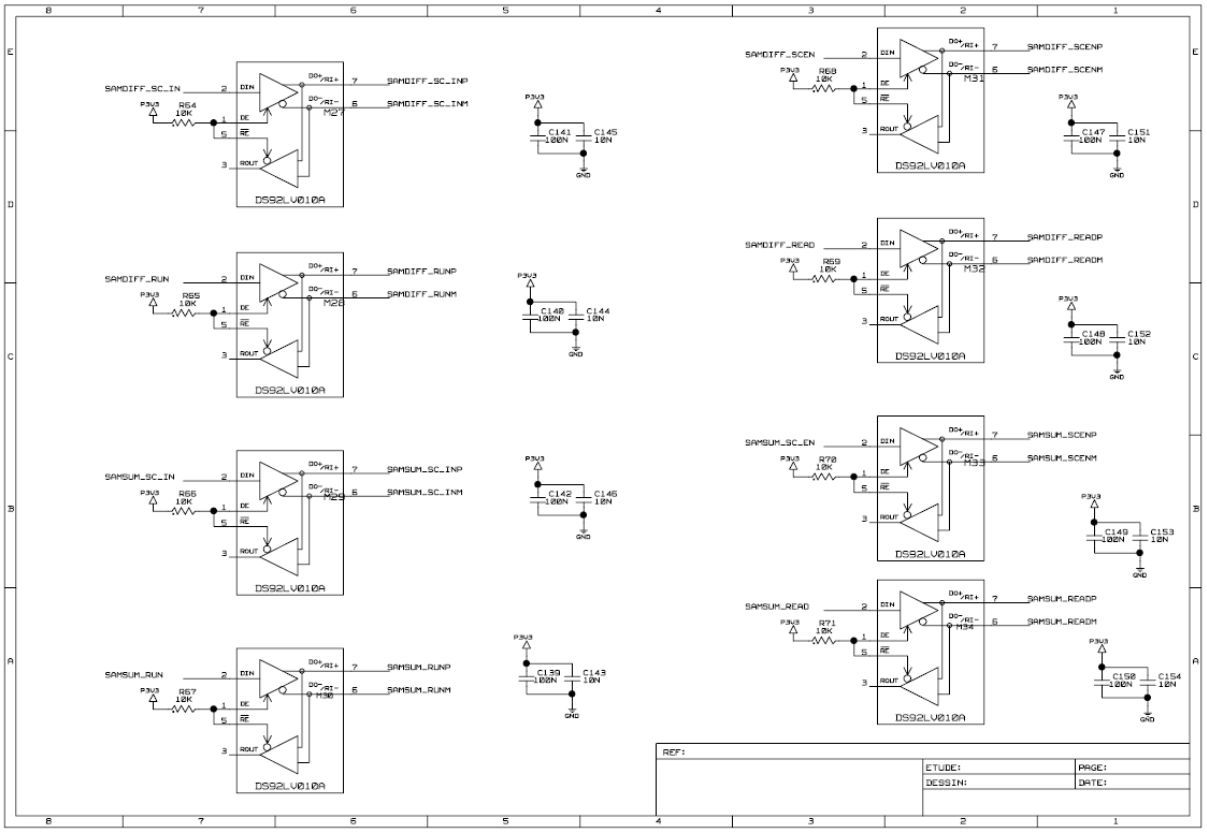
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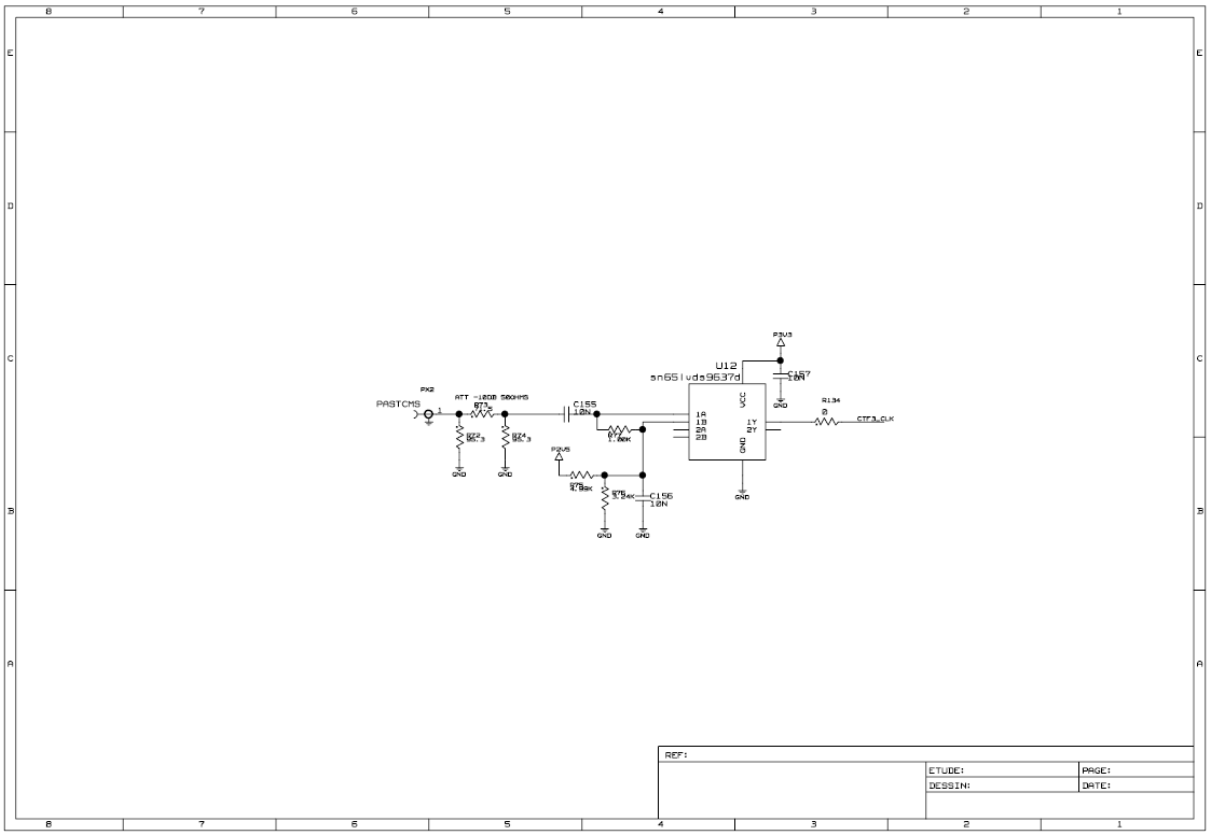
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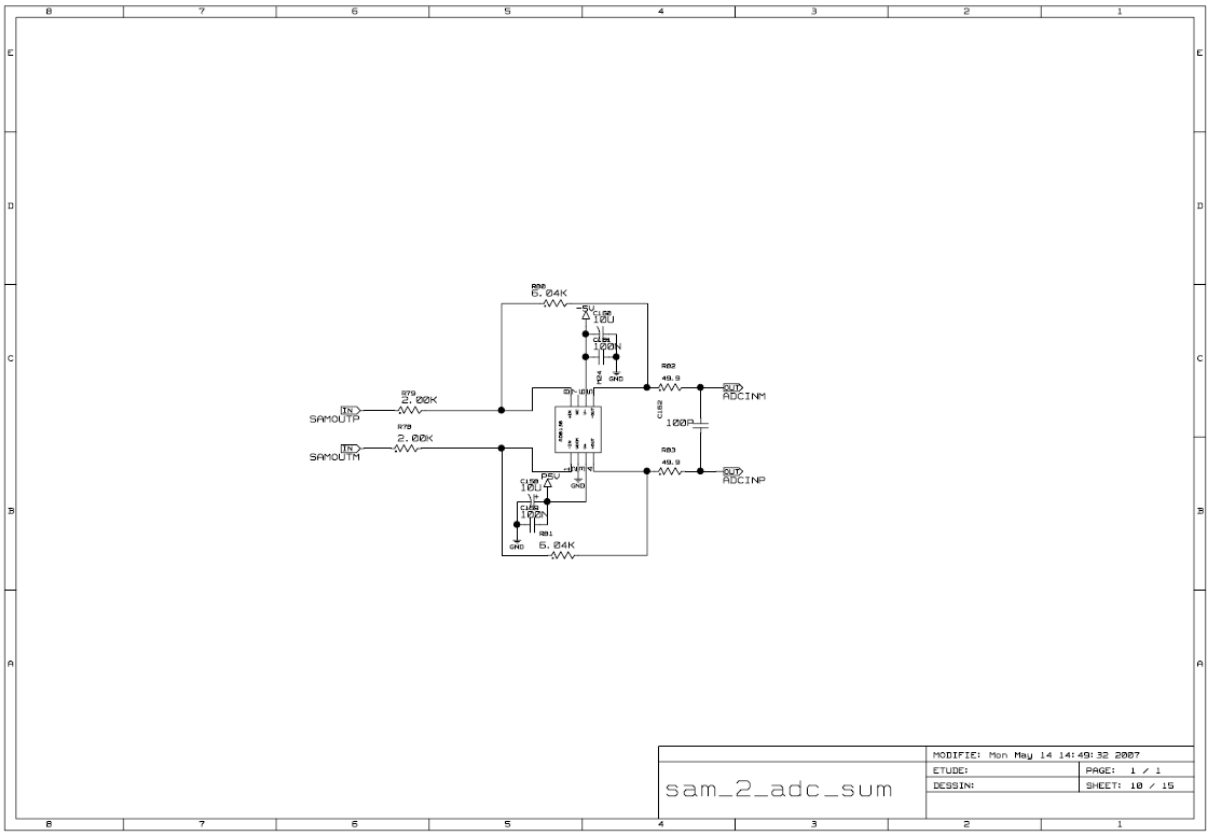
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OUT
ADCINP
R79
2.00K
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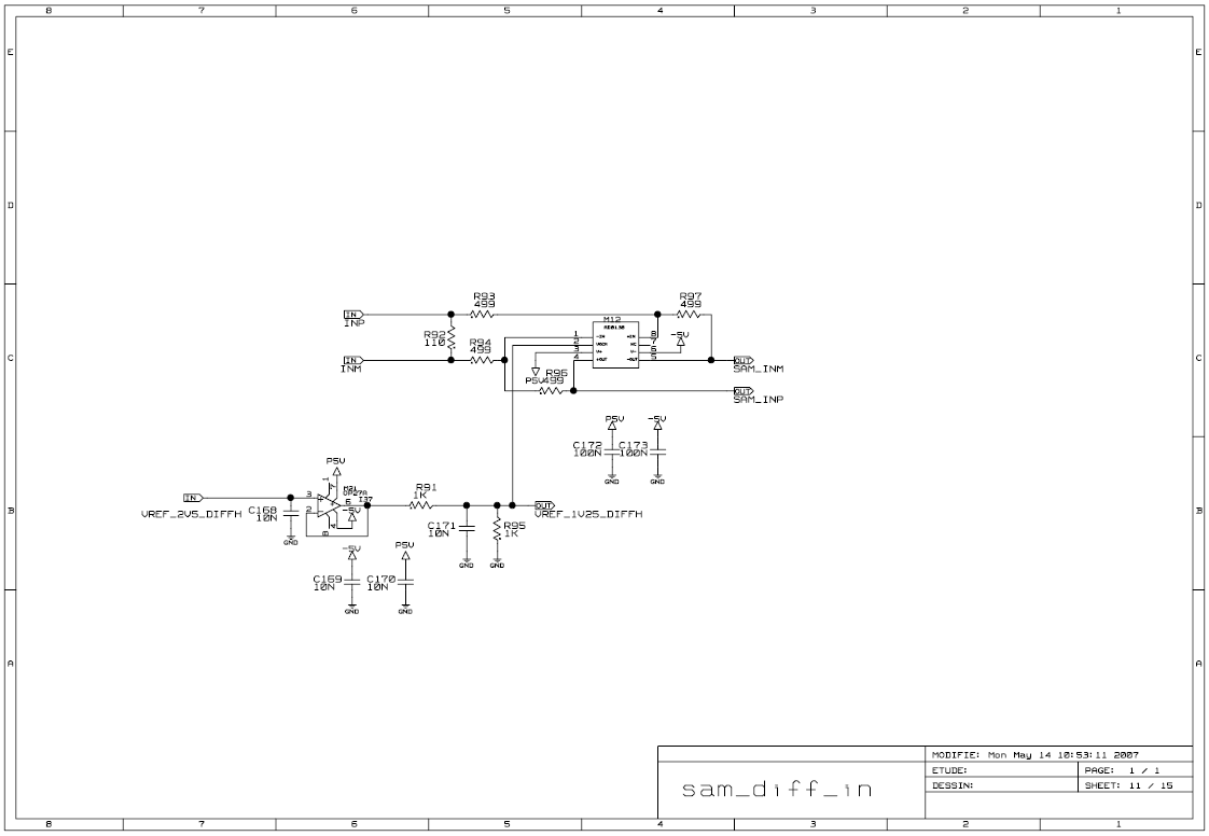

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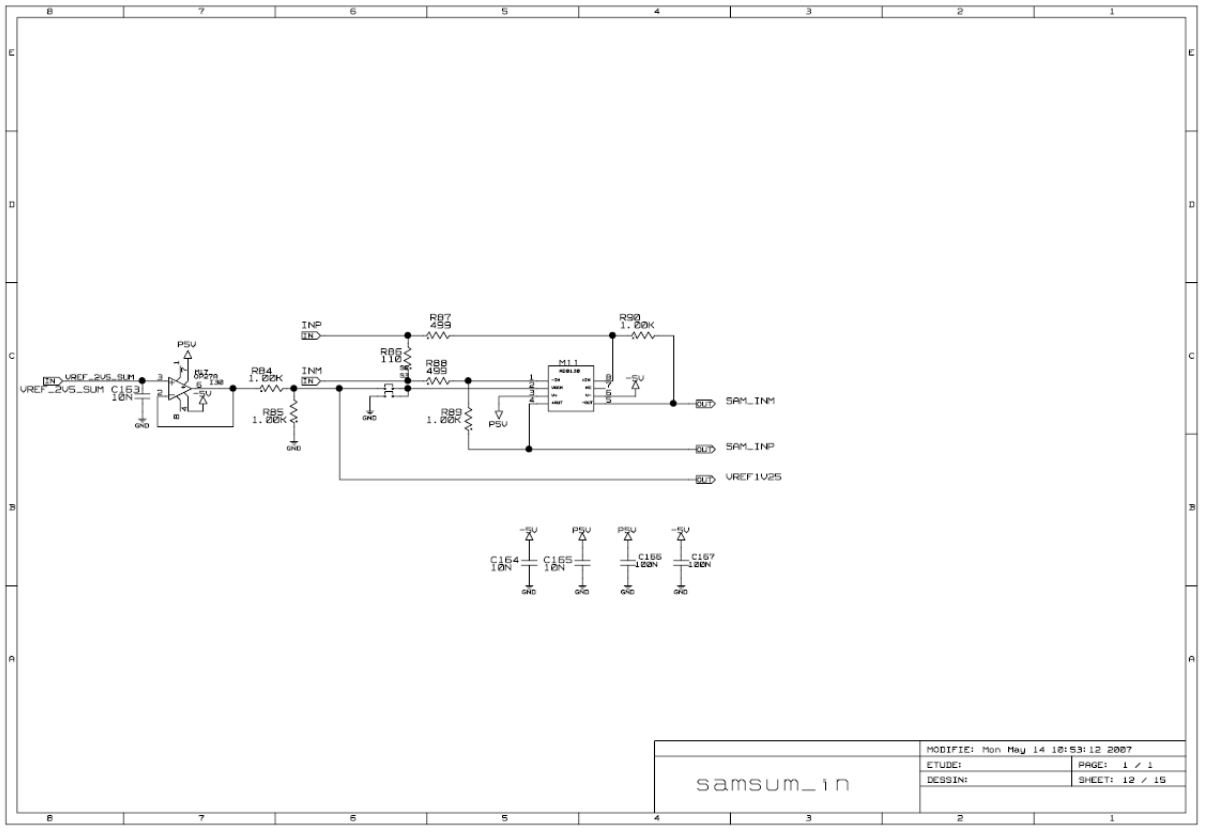

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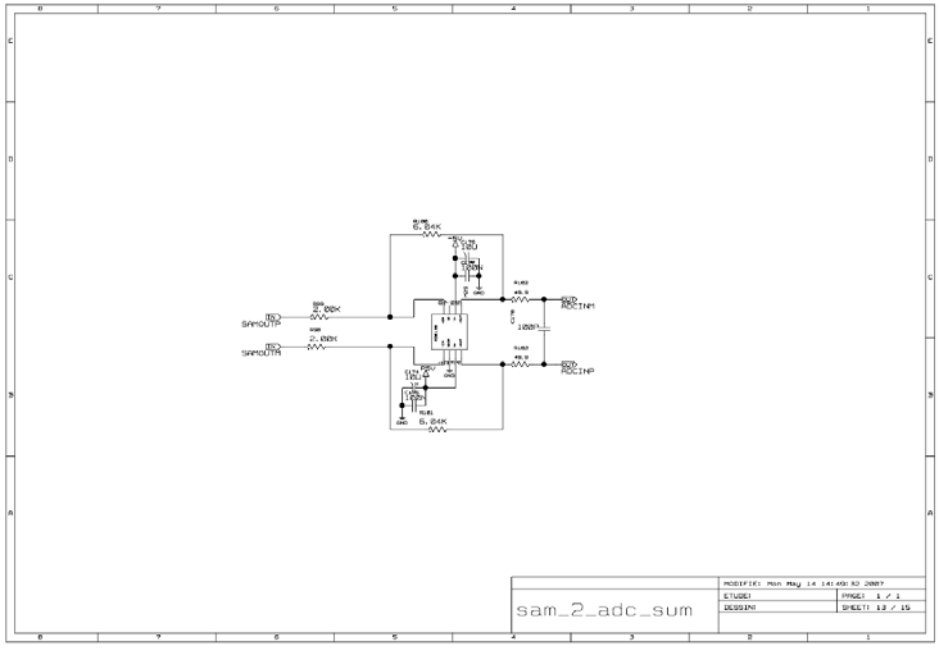
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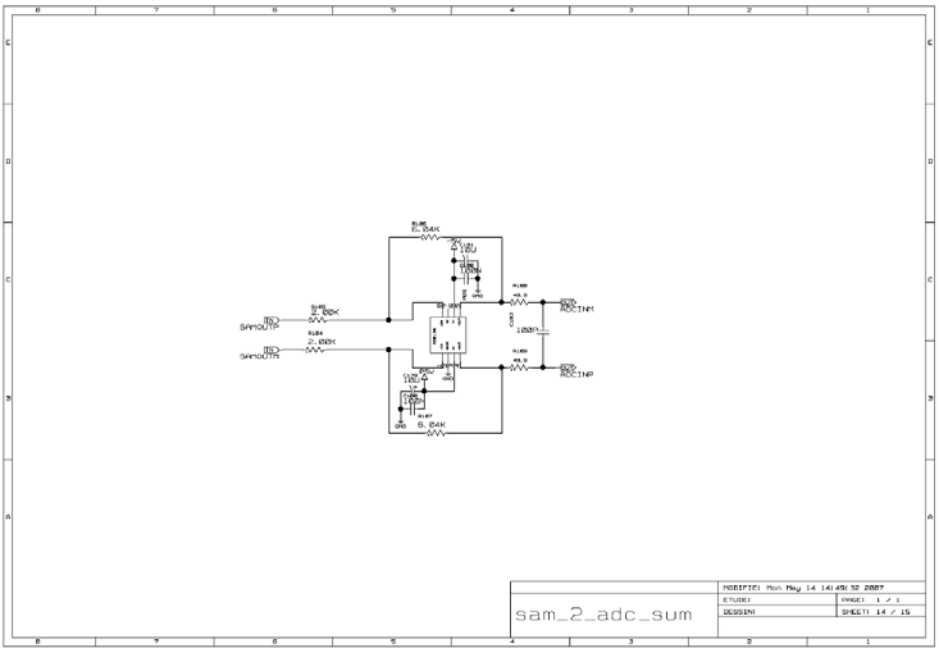
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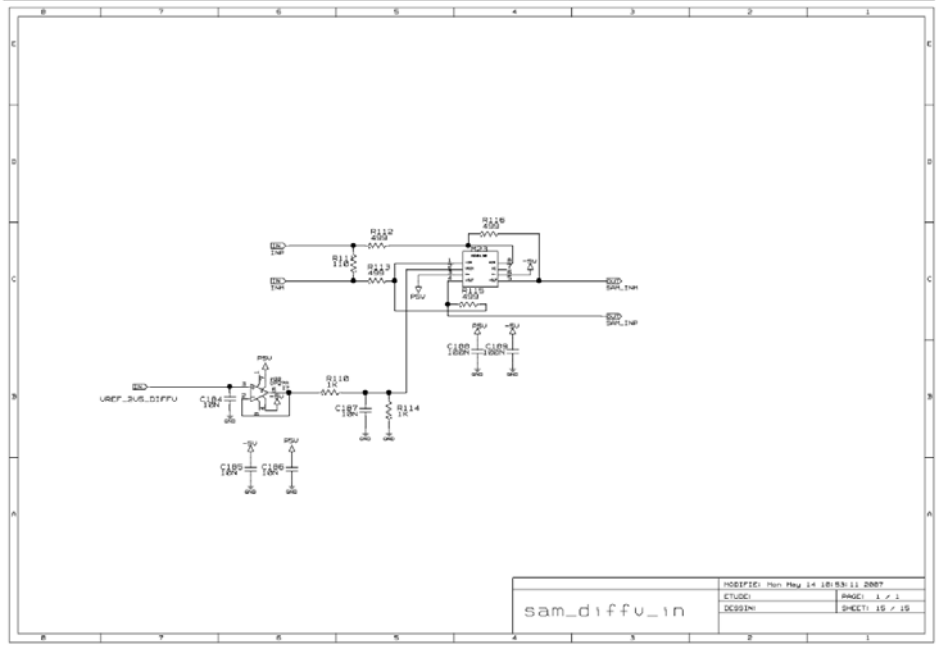
sam_diffv_in

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