Detector Control System of the ATLAS Insertable B-Layer

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Abstract

To improve tracking robustness and precision of the ATLAS inner tracker, an additional, fourth pixel layer is foreseen, called Insertable B-Layer (IBL). It will be installed between the innermost present Pixel layer and a new, smaller beam pipe and is presently under construction. As, once installed into the experiment, no access is possible, a highly reliable control system is required. It has to supply the detector with all entities required for operation and protect it at all times.

Design constraints are the high power density inside the detector volume, the sensitivity of the sensors against heat-ups, and the protection of the front end electronics against transients. We present the architecture of the control system with an emphasis on the CO_2 cooling system, the power supply system, and protection strategies. As we aim for a common operation of Pixel and IBL detector, the integration of the IBL control system into the Pixel control system will also be discussed.

DETECTOR LAYOUT

The Insertable B-Layer is a pixel detector, which is mounted directly on the LHC beam pipe. Fourteen mechanical support structures, called staves, form a cylindrical shell with an average radius of 33.25 mm and a length of 698 mm. A pseudo-rapidity of $|\eta| < 3$ is covered. Each stave carries sixteen modules. They are composed of the sensor itself and two frontend chips, whose read out cells are bump bonded to the sensor cells. While the inner modules of each stave will be built by planar sensors, the outermost modules of each stave are 3D sensors. In total there are three quarters of planar and one quarter of 3D sensors. For details of the different sensor technologies, see [1]. The frontend readout chips, the FE-I4s, are produced in a 130 nm bulk CMOS process. Its pixel cells are organized in 80 columns with a pitch of 250 µm and 336 rows with 50 µm pitch. Altogether 448 frontend chips provide 12 million readout channels.

Due to the high power dissipation of the detector modules, an efficient cooling system is required. Therefore a cooling pipe is integrated into each stave. An evaporative cooling using CO_2 keeps the detector modules at (-25 to -30) °C. A total power of 1.4 kW can be removed from the detector. Extra cooling power is available to remove the environmental losses of the transfer piping.

The data of the frontend chips are sent to the counting room via optical data transfer. In the other direction configuration, trigger and control signals are sent by the DAQ system to the frontend chips, also using the optical link. The on detector part of the opto-electrical transceivers, the opto boards, are located close to the detector itself, while the off detector part, the Back of Crate (BoC) cards are installed inside the DAQ crates.

DCS REQUIREMENTS

The Detector Control System (DCS) is responsible for the safety of human beings, the detector and other equipment. It must provide tools to control the detector in all operation modes, like normal data taking with colliding beams, as well as calibration and tuning periods. To ensure the success of a command, feedback must be given to the operator. Furthermore the DCS must deliver additional information for debugging the detector and diagnosing its behaviour. Safety, control and diagnostics vary concerning required reliability, availability and granularity. Highest level of reliability is required for the safety system, a high level for all control actions, while the level can be lower for information which is used for diagnostics. Similar levels must be considered concerning the availability of a DCS component. While the safety system must be functional at all times, control units are required as soon as an operation is performed with the detector and diagnostic tools are activated on request. Concerning the modularity the levels are reverse. If the behaviour of the detector must be analysed, detailed information on small units like individual frontend chips must be available. On the other hand, if the detector must be protected against upcoming risks, even larger parts of the detector can be stopped.

A clear user interface, automatic safety and error recovery procedures and archiving of data are tools to fulfill the above listed requirements. Furthermore the integration of the IBL DCS into the Pixel and the ATLAS wide control system [2] must be ensured. These demands have impact on the choice of hardware as well as on the software design of the IBL control system.

DCS HARDWARE

An overview on the IBL DCS hardware is given in Figure 1. The detector modules, the opto boards and the BoC/DAQ crates are subjects to DCS. Furthermore the detector environment must be permanently watched. These are the entities which require monitoring and/or control.

Several power supplies (HV, LV, SC-OL) provide all units with the power they need. On the other side the high power dissipation is compensated by the cooling system.

Various monitoring mechanisms are in place, some of them provide in parallel inputs to the interlock system. This system is responsible for the safety of human being and of the detector and acts directly on the power supplies if an error condition is found. The normal control and monitoring functions are provided by the Cooling and DCS PCs. Most parts of the DCS are located in the counting room which is about 100 m away from the inner detector itself. Just the regulator station and some monitoring units are installed inside the detector cavern.

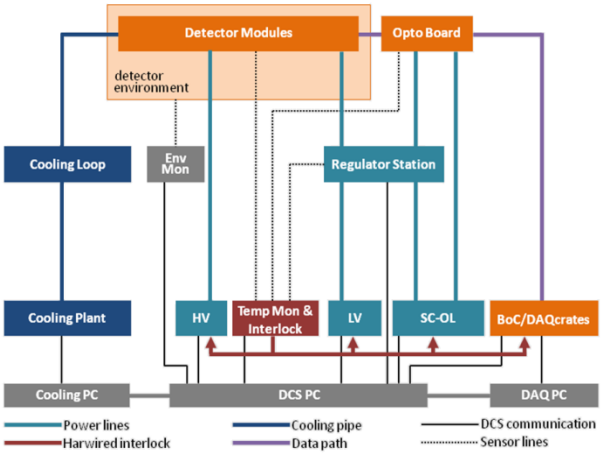

Figure 1: DCS Overview

Power supplies

Detector modules and the opto boards require a dedicated powering which is exactly adapted to the needs of the loads. To all components in common is the request of floating supplies. The output voltages must be variable. Concerning safety, over-current protection and interlock inputs are of main importance.

To deplete the sensors a HV power supply is required. While the planar sensors will need up to 1000 V after irradiation, the 3D sensors can be operated with significantly lower voltages of a few hundred Volt.

The frontend chips are powered by the low voltage (LV). Due to the required currents of up to 900 mA per frontend chip the voltage drops on the services are not negligible. The frontend chips themselves require just 1.2-1.5 V, however the LV supply will be able to deliver 10 to 15 V. As on the other side the frontend chips, which are produced in a deep submicron technology, would be destroyed by over voltages of more than 4 - 5 V, a voltage regulation close to the detector is performed. It protects the sensitive chips against transients and is therefore an important safety mechanism. Key components of the regulator station are the regulator LHC4913 and digital trimmers which allow for a remote control. For more details on the regulator station see [3].

The third voltage supply SC-OL (supply and control of the opto link) is responsible for the powering of the opto boards, which require three different low voltages [4]. The VCSEL driver chip and the decoder chip are powered by Vvdc with a maximum voltage of 10 V and 800 mA. As also the chips of the opto link must be protected, Vvdc is routed through the regulator station in the same way as LV. The receiver diodes need a higher voltage of up to 20 V, while 5 V are sufficient for Viset. Viset allows for control of the VCSEL output current. Additionally a reset signal is provided which can be sent to the decoder.

Cooling system

The 14 IBL staves are cooled with 14 parallel cooling loops with evaporative CO_2 of around -40 °C. The 14 cooling loops have manifolds in the muon detector area which is accessible in technical stops. The cooling pipe in the stave has an inner diameter of 1.5 mm and is made of titanium. The in and outlet tubes are both 12 m long and have an increasing diameter in the upstream direction to accommodate the expanding vapour. The inlet is 1 mm and 1.5 mm, the outlet 2 mm and 3 mm.

The cooling plant is located in the USA-15 cavern, the piping distance to the detector is about 100 m. The cooling system is using the 2PACL cooling concept [5] as it was developed for the LHCb-Velo cooling [6]. In a 2PACL system the pressure of boiling is controlled by an accumulator in the plant. The accumulator pressure is controlled by heating or cooling. The pressure in the detector is similar to the plant pressure and thus can the boiling pressure and hence temperature can be controlled from the plant only. With this system no active control and sensing is needed inside the unaccessible detector. The cooling inside is completely passive. Temperature sensors for monitoring are available on each stave in- and outlet. Figure 2 shows a schematic of the IBL CO_2 cooling. Half of the amount of staves will have a flow in the opposite direction so that the outlet flow can cool the inlet flow of the other tubes. This pre-cooling is needed to suppress boiling in the inlet due to parasitic heat. The cooling loops are connected to the transfer line in the junction box located in the muon detector area. The transfer line is a concentric pipe exchanging heat between the in and outlet. This heat exchange conditions the inlet flow to be the right temperature for boiling. As all the pipes are cold, they have to be insulated. Inside the detector there is vacuum insulation, outside the detector there is foam insulation. Two identical cooling units are foreseen for redundancy reasons.

Monitoring

While all power supplies have built-in monitoring units which provide information concerning voltage and current, the temperature monitoring is handled separately. Many temperature sensors are installed and deliver their information into DCS through different paths.

Any equipment which can be damaged by overheat is equipped with an NTC (Negative Temperature Coefficient) sensor, whose value is read by the DCS monitoring units. In parallel its information is fed into the interlock system (see the next section). Further NTCs on the cooling pipes, the cable trays, and elsewhere in the detector environment provide the cooling experts with information which allows for debugging of the system.

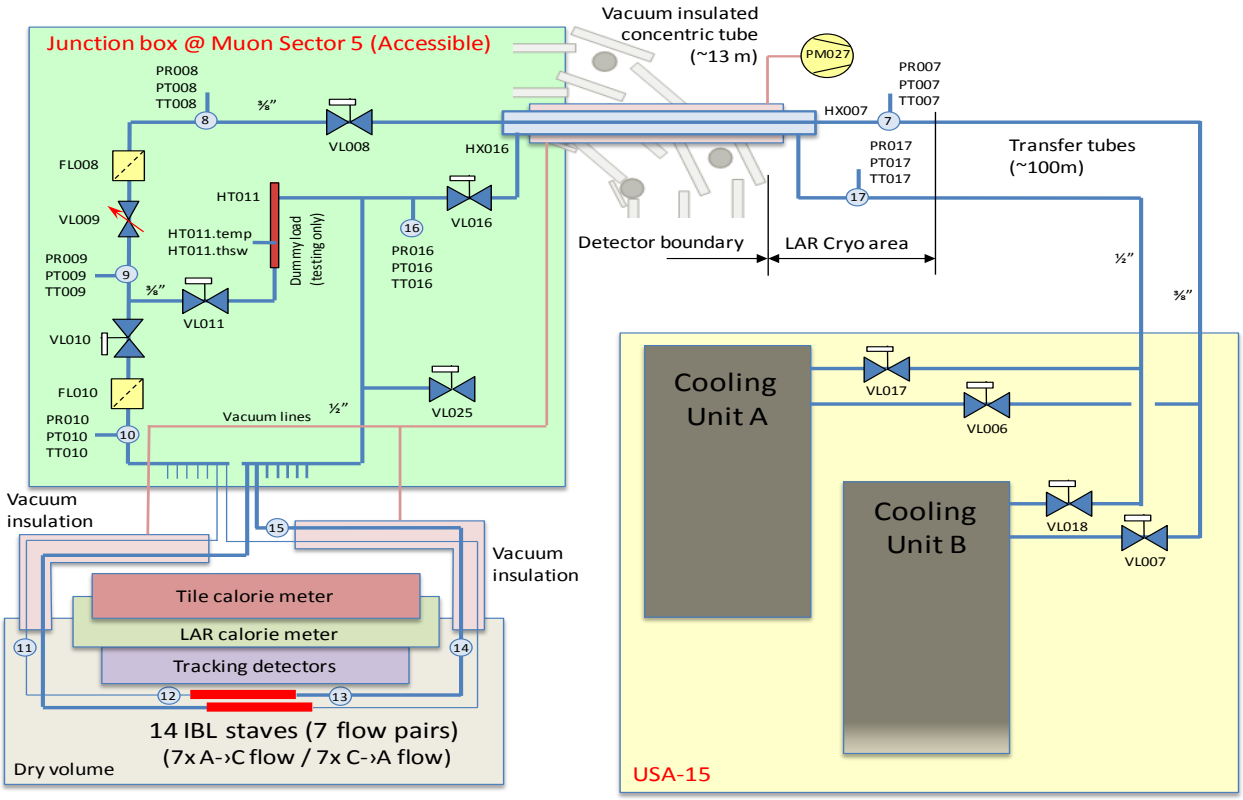

Figure 2: Cooling System

A further source for detailed debugging of the frontend chips are, among others, temperature sensors (diodes), which are built-in in the frontend chips themselves. In order to control the complex electronics of the FE-I4 [7] and its environment, several voltages and currents are monitored on-chip and digitized for readout. A 10 bit ADC has been designed for this purpose and is associated to an 8 to 1 analog mux in order to select one input among: temperature, power supplies, voltage references, detector leakage current, and other DC analog voltages. On demand these information can be sent through the standard data path. Inside the DAQ dedicated routines extract the DCS information. This monitoring is a promising approach for future Detector Control System developments in order to reduce the material inside the detector volume.

As the monitoring of the DAQ crates and BoC cards is based on standard monitoring tools, it is not described here.

Interlock

As irradiated sensors can be irreparably damaged by overheat, the detector modules are equipped with NTCs which are readout through DCS and in parallel feed their information into the interlock system. A discriminator compares the signal to a threshold which represents the maximum allowed temperature, and creates a logical signal in case of overheat. In the same way, opto boards and the regulator stations are equipped with NTCs.

All signals are collected by the interlock system. It determines which power supply must be switched off and sends out the related signal to the power supply. The core component of the interlock system is a flash FPGA with an internal EEPROM. This avoids the need of a program loading at power-on. A negative logic is implemented, which means that a missing cable or power loss cause automatically an interlock. Additional information from the laser protection system, the cooling system, the LHC or other external systems will be included into the interlock matrix.

As this system is completely hardware based and does not require any software to be running, it provides a maximum of safety.

DCS SOFTWARE

The DCS software splits into three parts, one handling the integration of the hardware into the software, the user interface to operate the detector and connections to the databases plus tools for monitoring.

It is foreseen to purchase the power supplies from the same vendors as they were selected for the Pixel detector and to use the same hardware for custom made devices

(e.g. regulator station, SC-OL). Therefore, the pixel software packages can also be applied to integrate the IBL hardware. Besides the fact that large development work can be avoided, using the same integration software also guarantees an easy integration of the IBL DCS into the pixel frame.

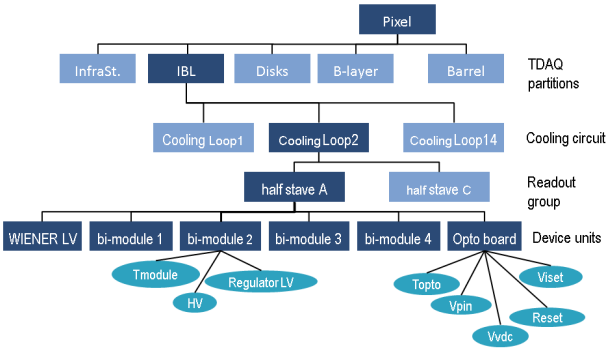

Figure 3: FSM tree of the IBL

The tool to operate the detector and all its components is the FSM (Finite State Machine). Using the control concept as it is defined by the ATLAS FSM [8] provides the integration of the IBL into the pixel detector and ATLAS. Figure 3 shows the FSM tree of the IBL. The top nodes (TDAQ partitions) are defined by ATLAS. It is also evident that the IBL is a part of the pixel detector. The nodes below IBL reflect the detector's constraints. As done for the pixel detector, a geographical approach is followed.

As the cooling loops can be controlled separately, they define the next level of partitioning. They correspond each to one stave. All modules of a half stave share the same opto board concerning the readout. This defines the next level of partitioning. Besides the opto board, LV and four bi-modules belong to a half stave, respectively readout group.

Due to the services four frontend chips with their two sensors (in case of planar sensors) are the smallest unit which can be separately steered by DCS and are called bi-module.

If the detector behaviour must be studied in more detail the 3D-viewer is a useful tool for experts. It is based on the fw3DViewer package (developed by CERN ITCO [9]) and allows for monitoring of any data available with module granularity. Online as well as historical data can be displayed in any 3D view. Especially 3D views of temperatures or leakage currents can help to diagnose problematic detector regions.

SUMMARY

In 2013 the IBL will be installed as the innermost part of ATLAS. It will complement the existing Pixel detector as a fourth layer. Although being a pixel detector, its sensors and frontend chips are different concerning their qualities and needs.

A complex detector control system is required to supply all required voltages, to keep the detector at an adequate operating temperature, to provide operators and experts with all tools and information they need, and to ensure the safety of the detector at all times.

Key component regarding safety is the interlock system. Furthermore, the sensitive frontend electronics is protected against transients by the regulator station. The standard tool to control the detector will be the finite state machine, which in parallel allows for an easy integration of the IBL DCS into the Atlas wide control system. For debugging the detector and diagnosing its behaviour the built-in sensors of the frontend electronics and the 3D viewer are of special interest.

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