Front-end multi-channel PMT-associated readout chip for hodoscope application

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Abstract

For developing a prompt gamma imaging system, we have designed a 16-channel readout chip in a BiCMOS process to be associated with multi-anode photomultipliers (MaPMTs). Each channel has one current input and two separated outputs. The input has very low impedance to minimize electrical crosstalk and effects of capacitances. The two outputs serve to, respectively, detect signal event and quantify signal charge. The channel architecture is a current-mode one, employing a current conveyor to drive both a buffered current comparator and a charge-sensitive amplifier (CSA). The current conveyor is built with super-common-base (SCB) transistor structures to obtain input impedance in the order of a few ohms. Circuit design with the use of bipolar transistor components also improves frequency and noise performances. The chip has been tested and the evaluated characteristics meet the system requirements.

Keywords:
prompt gamma imaging system, super-common-base(SCB), current conveyor, charge-sensitive amplifier (CSA),

1. INTRODUCTION

References

Ion therapy is an innovating technique used to treat tumors with enhanced efficiency for the dose deposition conformation as compared to conventional radiotherapy. It requires real-time control of the dose localization during ion therapy, since slight deviations relative to treatment planning may lead to severe consequences. With the aim of developing a primary beam monitor (a beam hodoscope) for such a quality control [1], we propose a prompt gamma imaging system shown in Figure 1. For typical proton and carbon therapeutic beams, the required hodoscope should have a count rate capability of 10^8 pps, with an accuracy of 1ns. This has led us to implement the system employing arrays of scintillating fibers with read out by MaPMTs or multi-channel plates (MCPs) [2].

The system development requires a dedicated multi-channel readout ASIC (Application Specific Integrated Circuit) to be associated with the MaPMTs. Each channel should have very low input impedance to avoid electrical crosstalk between adjacent channels and to minimize effects of detector and wiring capacitances (Cd + Cw). Crosstalk between channels may degrade position resolution [3], while these capacitances may degrade both frequency and noise performances [3]. Each channel should also provide two separated outputs corresponding respectively to high-speed signal-event detection and low-noise signal-charge quantification at low counting rate.

This paper presents a readout chip for this purpose. It has been designed in a 0.35μm SiGe BiCMOS process (AMS). This process allows the use of RF and large-transconductance bipolar components, which is useful for the design of wide-band, low-impedance and low-noise circuits with improved performances[3].

2. CIRCUIT DESCRIPTION

The readout MaPMT-associated chip includes 16 channels whose input impedance should be very low (in the order of ten ohms) to minimize crosstalk and wiring capacitance effects. Each channel is a current-mode architecture (shown in Figure 1) defined to allow better achievements in speed and noise performances. It is composed of a current conveyor (with two current outputs) as an input stage, and two separated output stages: a current comparator as a discriminator for signal-event detection and a charge-sensitive amplifier (CSA) for signal charge quantification. The signal-event detection requires high-speed operations for the current conveyor and the current comparator, while the signal charge quantification has a major low-noise requirement for the current conveyor and the CSA.

2.1. Current Conveyor

The current conveyor has a low-impedance input and two high-impedance current outputs, with a 4-bit current gain control to compensate effects of optic fiber ageing and the MaPMT's gain dispersion. Figure 2(a) shows the structure of the current conveyor. It employs two Super Common-Base (SCB) transistors [4-5] (see Figure 2(b)) to drive complementary switched current mirrors having variable-gain output branches. The current input signal is applied to one SCB, and a referenced current is applied to the other to cancel bias offset contribution to the output signals.

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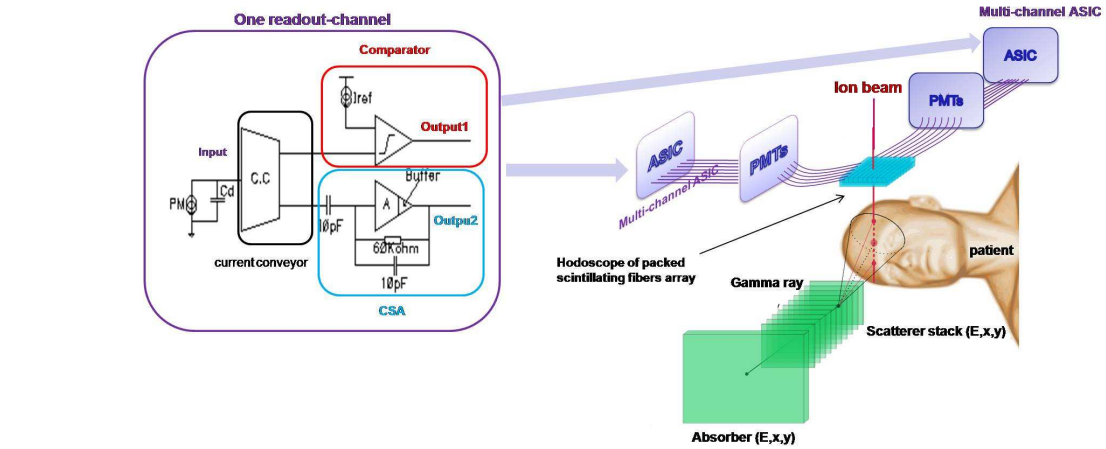

Figure 1: Prompt gamma imaging using a beam hodoscope

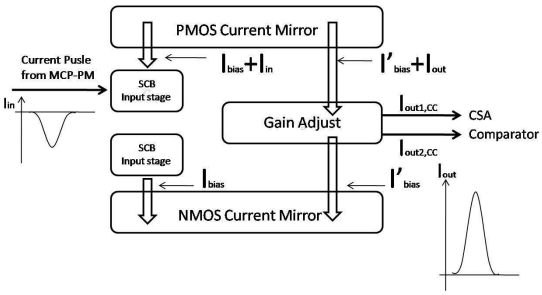

Figure 2: (a)Low-impedance,variable-gain current conveyor

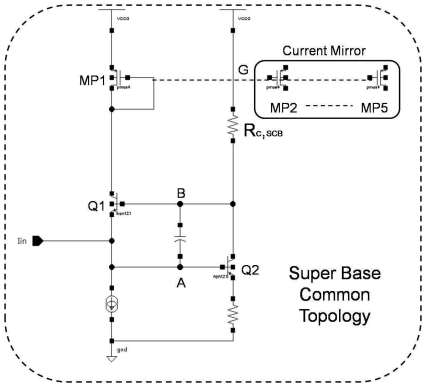

Figure 2: (b)super-common-base SCB transistor structure

The SCB transistor shown in Figure 2(b) is basically a common-base topology (Q_1) with a negative feedback loop (Q_2). The input impedance of the current conveyor, mainly determined by that of the SCB, is expressed as:

$$Z_{in} = \frac{1}{(1+\frac{A_0}{(1+s/\omega_A)(1+s/\omega_B)})\cdot g_{m,Q_1+sC_A}} \quad (1)$$

$$A_0 = g_{m,Q_2}\cdot R_{C,SCB}$$

$$\omega_A = g_{m,Q_1}/(2\pi\cdot C_A)$$

$$\omega_B = \frac{g_{m,Q_2}\cdot R_{C,SCB}}{2\pi\cdot(1+g_{m,Q_2}\cdot R_{C,SCB})\cdot r_{\pi,Q_1}\cdot(C_{\pi,Q_1}+C_{\mu,Q_2})}$$

$$C_A = C_{DB,M_1}+(1+g_{m,Q_2}\cdot R_{C,SCB})\cdot(C_{\pi,Q_1}+C_{\mu,Q_2})+C_{\pi,Q_2}+C_D$$

where A_0 is the voltage gain of Q_2 at low frequencies; C_A is the sum of parasitic capacitances at the input node A (including the detector output capacitance C_D), ω_A and ω_B are poles related respectively to nodes A and B. At moderate frequencies, the input impedance is given by $Z_A \approx 1/(A_0\cdot g_{m,Q_1})$. Thanks to the use of large-transconductance bipolar components in the SCB, Z_{in} can be reduced to a few ohms.

The current gain of the current conveyor is given by[6]:

$$\frac{I_{out}}{I_{in}} = \frac{g_{m,MP_2-MP_5}}{g_{m,MP_1}} \times \frac{1}{(1+\frac{sC_1}{g_{m,Q_1}})(1+\frac{sC_2}{g_{m,MP_2}})} \quad (2)$$

with $C_1 = C_{be,Q_1}$ and $C_2 = \Sigma C_{nodeG}$
where g_{m,MP_2-MP_5} is the total transconductance of the 4-bit switched transistors MP_2 to MP_5 in parallel. As $g_{m,Q_1}(BJT) \gg g_{m,MP_2}(PMOS)$, and $C_1 \ll C_2$, the bandwidth is limited by g_{m,MP_2} and C_2.

2.2. Current Comparator

The current comparator following the current conveyor detects current signal events. It compares the current conveyor's corresponding output signal (typically lasting a few nanoseconds) with a referenced threshold current and produces a pulsed output voltage response.

Figure 3 shows the current comparator mainly consisting of a signal current mirror and a 2-stage output buffer. The signal current mirror employs bipolar transistor components to reduce its input impedance and to improve the speed performance of the circuit. This current mirror performs current-to-voltage conversion at its output:

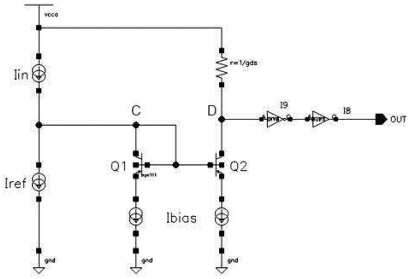

Figure 3: Current comparator for signal-event detection

$$\triangle V_D = \begin{cases} \triangle I_c \cdot \frac{g_{m,Q_2}}{g_{m,Q_1}} \cdot \frac{1}{g_{ds}+g_{ce,Q_2}} & when \quad \triangle I_c = I_{in} - I_{ref} > 0 \\ 0 & when \quad \triangle I_c = I_{in} - I_{ref} < 0 \end{cases} \tag{3}$$

The time constants at nodes C and D are respectively $\tau_C = C_C/g_{m,Q_1}$ and $\tau_D = C_D/g_{m,Q_2}$ with $C_C = C_{ce,Q_1} + C_{be,Q_1} + C_{be,Q_2} + (1 + g_{m,Q_2}/g_{ds}) \cdot C_{\mu,Q_2}$ and $C_D = C_{ce,Q_2} + C_{invertor}$. As $C_C \gg C_D$ and $g_{m,Q_1} < g_{m,Q_2}$, the speed performance of the current comparator is determined by τ_C. It can be optimized by careful layout and proper sizing of transistor components to reduce different capacitance contributions to C_C. The 2-stage buffer converts $\triangle V_D$ to a logic-level pulse.

2.3. CSA(Charge Sensitive Amplifier)

The CSA consists of a buffered amplifier and a R_fC_f feedback network (Figure 4(a)). For a fast input current pulse during a time $t_{pulse}(\sim 20ns)$, the CSA output produces a voltage swing given by:

$$\triangle V_{out,CSA} = -\frac{1}{C_f}\int_0^{t_{pulse}} I_{in}(t)dt \tag{4}$$

After the input current pulse, $V_{out,CSA}$, returns exponentially to its steady level with a time constant determined by R_fC_f. This time constant is chosen according to the maximum counting rate.

The buffered amplifier has an input part shown in Figure 4(b), which is a folded-cascode structure with R_A and C_A for feedforward compensation [7-8]. The second cascode transistor Q_1 is a bipolar component for better gain, speed and/or phase margin achievements. The input transistor MP_1 has a large W/L ratio to minimize its noise contribution.

3. RESULTS AND DISCUSSION

Figure 5 shows the fabricated readout chip. The chip area including pads is $6.16mm^2$. Each channel occupies a surface area of $680\mu m \times 120\mu m$. The chip has been tested using a board shown in Figure 6(a).

The test board includes a structure shown in Figure 6(b), to generate an input current signal for the testing:

$$I_{in}(t) = \frac{C_g \cdot dV_{gen}(t)}{dt} \tag{5}$$

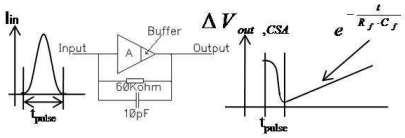

Figure 4: (a)Charge-Sensitive Amplifier

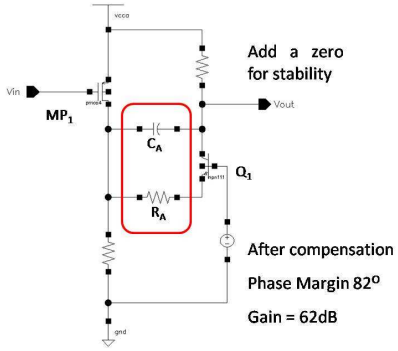

Figure 4: (b)Amplifiers with feed forward compensation

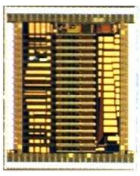

Figure 5: Microphotograph of the readout chip

The magnitude of $I_{in}(t)$ can thus be evaluated from the waveform of V_{gen}. By measuring directly the magnitude of V_{in}, the input impedance of the current conveyor can be determined by $Z_{in} = \frac{\triangle V_{in}}{\triangle I_{in}}$. We have obtained $Z_{in} = 12\Omega$.

Figure 7 shows signal waveforms of a channel. The circuit operation is verified by observing the output signal of the current comparator $V_{out,comp}$ and that of the CSA $V_{out,CSA}$: the pulsed output of the current comparator indicates the signal event, and the output signal of the CSA gives a magnitude $\triangle V_{out,CSA}$, from which an input signal charge can be evaluated.

For signal-event detection, the detection threshold for the current comparator is set by I_{ref}, which can be adjusted from $100\mu A$ to $400\mu A$.

For signal charge quantification, the conversion gain at the output of the CSA is 98mV/pC. The evaluated noise in ENC (Equivalent input RMS Noise Charge) is 91fC. The maximum measurable charge before saturation (limited by the current conveyor) is 10 pC. The dynamic range is 36 dB. The crosstalk between adjacent channels is 1.7% (i.e. 35 dB).

Figure 6: (a)Test board

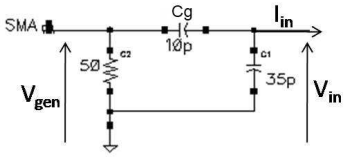

Figure 6: (b)Structure for generating input current signal

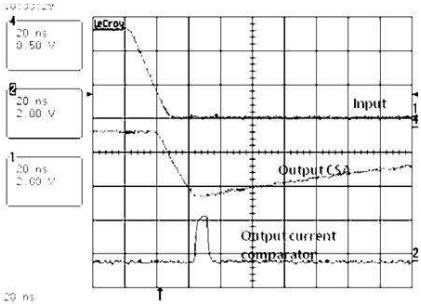

Figure 7: Signal waveforms of a channel:the two outputs $V_{out,CSA}$ and $V_{out,comp}$ in response to V_{gen}

Table 1: Summary of characteristics of the designed readout ASIC

	Post-Layout results	Test results
Power consumption /channel(under 3.3V) @ current gain from 0.25 to 2	15 to 22mW	16 to 23mW
Input dynamic range	$50\mu A(525\,fC)$ @gain 2 — 2.4mA(25.2pC) @gain 2	—
Input impedance @ working frequencies	4Ω	12Ω
Current Conveyor Bandwidth	200MHz	—
Current comparator Bandwidth	667MHz	—
CSA Peaking time	30ns	28ns
1-full-channel ENC	42fC	19fC
Xtalk	—	1.7%
Chip Size (including pads)	$6.61mm^2$	$6.61mm^2$

Table 1 summarizes the measured characteristics of the readout chip in comparison with post-layout simulation results.

We would like to mention that,our readout chip has similar integrated functions to a 10-channel chip reported in [9]. The power consumption and chip sizes are also comparable. We have obtained improved performances especially in terms of input impedance (12Ω compared to 180Ω), thanks to optimal design with the use of bipolar components in a BiCMOS technology.

4. CONCLUSION

We have designed a 16-channel readout chip in a BiCMOS process to be associated with MaPMTs or MCPs for developing a prompt gamma imaging system. Each channel is a current-mode architecture consisting of three main building blocks: a current conveyor, a buffered current comparator and a CSA. Testing of the chip has shown improved characteristics compared to a reported chip with similar functions. The channel input has very low impedance (~ 12Ω) to minimize crosstalk (~ 1.7%). The evaluated speed and noise performances meet the system requirements. We are undertaking a new chip design with performance optimization to reduce power consumption per channel, for high-resolution hodoscopes.

5. ACKNOWLEDGMENT

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