Drive beam stripline BPM electronics and acquisition

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DRIVE BEAM STRIPLINE BPM ELECTRONICS AND ACQUISITION.

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Abstract:

LAPP is involved in the design of the local module acquisition crate, described in the document *STUDY OF THE CLIC MODULE FRONT-END ACQUISITION AND EVALUATION ELECTRONICS* [1]. This acquisition system is a project based on a local crate, assigned to the CLIC module, including several motherboards. These motherboards are foreseen to hold mezzanines dedicated to the different subsystems. The next developments and sub-systems definition of specifications should determine the necessity of using the mezzanine architecture or only motherboards dedicated to subsystems. The module and controls are described in the CLIC CDR [2].
LAPP is involved in the development of Drive Beam stripline position monitors read-out. LAPP also develops a generic acquisition mezzanine that allows to perform all-around acquisition and components tests for drive beam stripline BPM read-out.
The choice of the presented stripline BPM as the drive beam position monitor is not definitive. The aim of this study is to estimate the feasibility of the acquisition according to the current CLIC drive beam specifications and to participate to the BPM qualification.
This document describes the chosen technical solutions and the possibilities for the future.

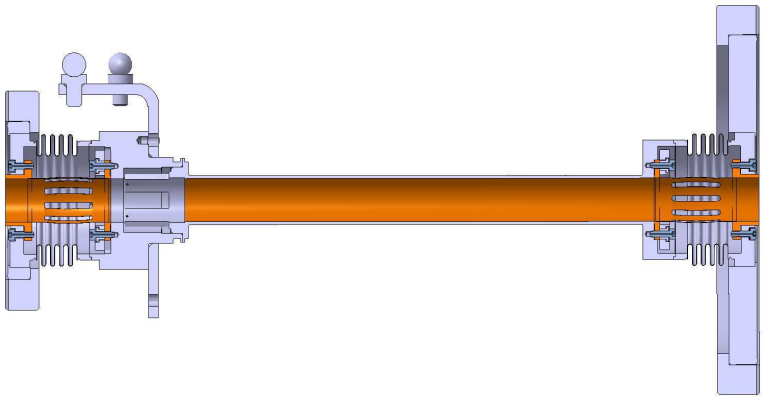
Summary:

1- Stripline BPM sub-system.

1-1 Description of the BPM stripline and specifications.

The specifications in term of position measurement for the nominal centered Drive Beam are:

- Transverse resolution =<2µm.
- Temporal resolution =< 10ns.
- Position accuracy =<20µm.



Stripline BPM and quad inner vacuum tube.

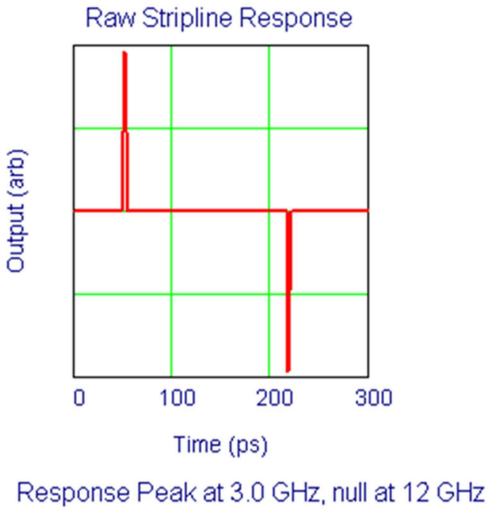
Stripline BPM characteristics: here, the first version of BPM is described.

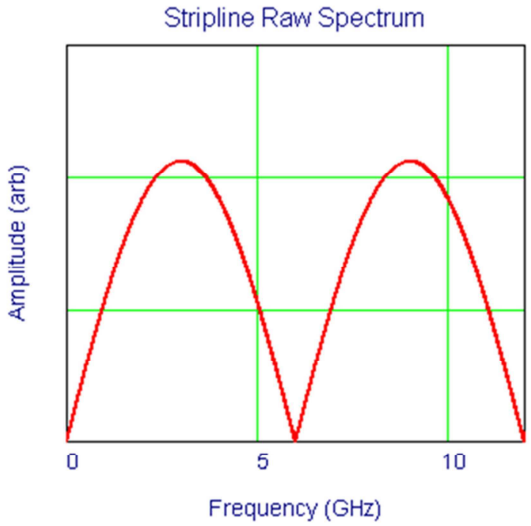
24mm diameter, 12.5% circumference width per strip, impedance 50Ω, stripline length 25mm.

The stripline intercepts a fraction of the image current depending on the circumference width. When a bunch is travelling in front of the upstream gap, an image charge splits in the two directions because the characteristic impedances are the same looking at the two sides. Two current pulses are created, travelling in the two directions. When the bunch travelling to the downstream termination encounters the downstream short-circuit, another pulse is created with the opposite polarity. This change of polarity is due to the inversion of the electric field between the ground plane and the edge of the stripline. This second pulse also splits in the two directions. As the velocity of the beam and of the stripline are the same, the current pulse descending on the stripline cancels with the descending opposed half pulse created at the downstream gap. So there will be no energy dissipated. The result is a pulse with half image charge, ascending to the upstream termination with a delay corresponding to *t=2L/c (with L the length of the stripline)*.

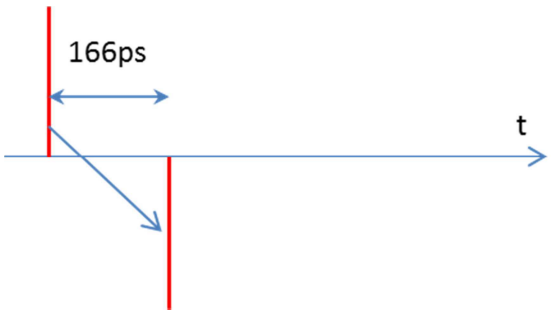
$$t = 2 \times 25.10^{-3}/_{3.10}\,8 = 166.7ps$$

In CLIC, the bunch frequency in beam is ***12GHz***. The 25mm stripline is resonant at frequencies multiple of 3GHz and anti-resonant at frequencies multiple of ***6GHz***. For frequency<6GHz, the response amplitude is $G \sim \sin(\frac{\pi f}{6.10^9})$:

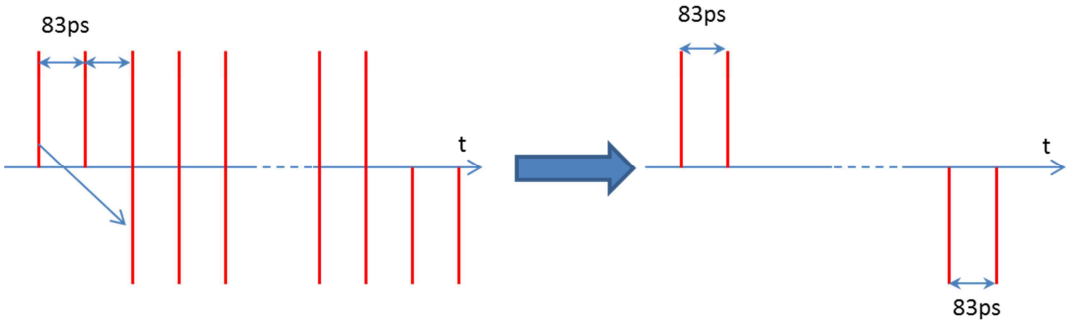




A single bunch beam will produce a signal with two opposed pulses with 166ps delay:



In the case of a train, bunches occur every ***1/12GHz=83ps***:



For a centered multi-bunch train, the first bunch produces an inverted pulse which cancels with the third bunch, and so on for the following ones. At the end of the train, two last inverted pulses are not cancelled. So finally a centered train of bunches produces a signal formed by two pulses at the beginning and two opposed pulses at the end. The cancellation occurs for a centered beam. For not centered beam, a fraction of pulse still remains not cancelled.

- Centered beam stripline response and charge:

The bunch charge produces an image charge on the stripline proportionally to its circumference width. The splitting and cancelation of pulses give an output signal made of a first pulse and of a second 166ps later with opposed polarity.
With a centered beam and Q the charge of the bunch, we can write the stripline induced current:

$$I(t) = \frac{\Phi}{2\pi}\frac{dQ}{dt}\left[\delta(t) - \delta(t - \frac{2L}{C})\right]$$

With δ(t) the Dirac function, ϕ the circumference angle occupation of the stripline and L the length of the stripline.
So a single bunch of charge Q produces two image charges on the stripline:

$$q' = \frac{1}{2}\frac{\Phi}{2\pi}Q$$

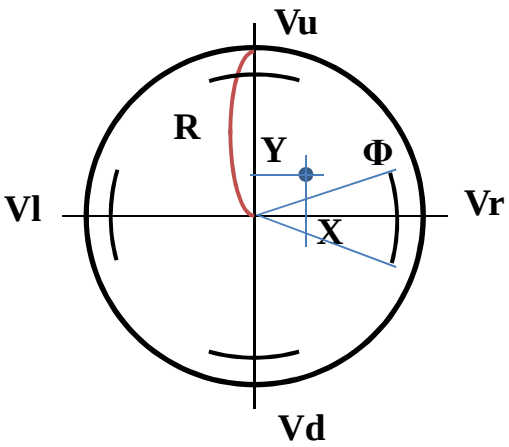
These image charges correspond to two current pulses with opposed polarities:

$$I = \pm\frac{1}{2}\frac{\Phi}{2\pi}\frac{dQ}{dt}$$

In CLIC, the bunch charge is ***Q=8,3nC*** and $\boldsymbol{\phi=\pi/4}$. So the stripline response corresponds to two induced charge pulses about $\frac{1}{2}.\frac{1}{8}.8{,}3.10^{-9} \approx \mathbf{0,52nC}$.

- Sensitivity:

The line is terminated by its characteristic impedance, 50Ω.
The resulting voltage depends on the deviation.



Stripline BPM cross section.

For example, the electrode current *Ie* on the right electrode can be written as follows:

$$Ie = -Ib\frac{2}{\pi}.\tan^{-1}\frac{[(1+x)^2+y^2]\tan{}^{\phi}/_{4} - 2y}{1-x^2-y^2}$$

With *Ib* the beam current, ϕ the stripline angle occupation, *x* and *y* the normalized beam displacements.

x=X/R and *y=Y/R* with *R* the radius of the BPM.

To estimate the specifications of the acquisition system, we have to estimate the maximum deviation response. The maximum foreseen deviation to observe is the half aperture, ***R/2=+/-6mm.*** The maximum signal will occur for a beam deviation aligned on electrodes axis.
So for example, for *Y=0* and *ϕ=π/4*, the expression becomes:

$$Ie = -Ib\frac{2}{\pi}.\tan^{-1}\frac{(1+x)^2\tan{}^{\pi}/_{16}}{1-x^2}$$

Maxima and specific cases:
Current for centered position current on the electrode:

- X=0; Ie=-0,125.Ib ; Predictable because of the 8th stripline angle occupation.

- X=R/2: x=0,5; Ie=-0,344.Ib ; corresponds to the maximum current.

- X=-R/2: x=-0,5; Ie=-0,042.Ib ; corresponds to the minimum current.

So, for a half aperture, the current on the closest electrode will be ***2,75*** times the reference current of a centered beam. The opposed electrode current will be ***1/3*** the reference centered beam current.

So a maximum factor ***~8*** between two opposite electrodes due to the half aperture deviation.

- Small deviation approximation:

The usual technique used to extract the position is the normalization Δ/Σ with Δ the difference between two opposed electrodes signals and Σ the sum of these two signals. For small X deviation, we can simplify the expression:

$$Ie = -Ib\frac{2}{\pi}.\tan^{-1}\frac{(1+x)^2\tan{}^{\pi}/_{16}}{1-x^2}$$

$$Ie = -Ib\frac{2}{\pi}.\tan^{-1}\frac{(1+x)\tan{}^{\pi}/_{16}}{1-x}$$

$$Ie = -Ib\frac{2}{\pi}.\tan^{-1}\frac{(R+X)\tan{}^{\pi}/_{16}}{R-X}$$

For x~0 , Arctan(x)=x

$$Ie = -0{,}125.Ib\frac{R+X}{R-X}$$

$$Vr = Z_0 Ie(X)\ ;\ Vl = Z_0 Ie(-X)$$

Calculating Δ/Σ with *Δ=Vr-Vl* and *Σ=Vr+Vl*; we obtain:

$$\frac{\Delta}{\Sigma} = \frac{4RX}{2R^2+2X^2}$$

For *X<<R*,

$$\frac{\Delta}{\Sigma} = \frac{2X}{R}$$

For small deviation, we can assume that the response is linear:

$$X = \frac{R}{2}\frac{\Delta}{\Sigma}$$

So the sensitivity is: ***R/2=3mm***.

This response is of course linear for small deviations of a centered beam.
The calculation does not take into account the possible mismatch between the gains of the signals chains used in the formula.
Gain mismatch produces a parasitic offset and a tilt in the sensitivity.
These issues are discussed in the chapter 4.

- Resolution:

Even if the response can be assumed as linear for small deviations, the reconstructed value depends on two electrodes readout electronics chains that should be the same. It means that the architecture allows to optimize gains in order to cover the maximum acquisition dynamic range for the electrode close to the beam and so the far electrode signal will not cover the maximum dynamic range. The consequence is a resolution reduction when deviation increases. It has been decided to acquire the electrodes and not to process the Δ/Σ in the preamplification chain.
We can calculate the resolution for any deviation on an electrode axis (X or Y, with V1 and V2 the electrodes voltages):

$$\frac{\delta x}{x} = \sqrt{\left(\frac{\delta\Delta}{\Delta}\right)^2 + \left(\frac{\delta\Sigma}{\Sigma}\right)^2}$$

with *Δ=V1-V2*, *Σ=V1+V2* and *V* the ADC input voltage:

$$\Delta = V\left(1 - \frac{V1}{V2}\right) \text{ and } \Sigma = V\left(1 + \frac{V1}{V2}\right)$$

$$\delta x^2 = 2x^2.\frac{\delta V^2}{V^2}.\left(\frac{1}{\left(1 - \frac{V1}{V2}\right)^2} + \frac{1}{\left(1 + \frac{V1}{V2}\right)^2}\right)$$

Replacing x by its value, we can calculate the resolution for any position on the axis. This resolution calculation does not take into account the possible gains mismatch between V1 and V2. This point is described in chapter 4.

<u>Particular point: centered beam</u>.

$$\delta X = \frac{R}{2\sqrt{2}} \frac{\delta V}{V}$$

The final position resolution will depend on the acquisition dynamic range.
With a 12mm radius and a centered beam 2µm resolution, we can calculate that ***δV/V=1/2121***, so a minimum ***67dB SINAD*** acquisition, corresponding to ***ENOB#10,7.***
In order to keep this resolution up to the half aperture, the needed resolution should be increased by a factor ***#2,75***, so a ***75,3dB SINAD*** acquisition, corresponding to ***ENOB#12,2.***
Because the electrodes responses are not linear in function of the deviation, the resolution will not be constant on the deviation range.
The ADC dynamic range will determine a resolution range corresponding to the deviation. At chapter *2-2 Foreseen resolution*, we trace this resolution with a chosen ADC.

- <u>Position accuracy:</u>

The needed position accuracy is 20µm, ten times the resolution. Even if the ADC ENOB is good enough, deviation precision could be limited by the integral nonlinearity, the different drifts and the common mode due to gains differences. Often calibrations should fix drift and common mode problems.
Concerning the integral nonlinearity, current ADCs have better linearity than the 3,3 bits (factor 10).
Even if the ADC linearity allows a better accuracy than needed, we have to keep in mind that absolute reconstructed position with BPM meets the specifications (20µm) for small deviations of a centered beam.
Calculating the difference between theoretical and calculated positions using the centered beam formula, we can estimate that the error is about ***20µm*** – the specified accuracy – for a deviation about ***0,6mm*** from the center, so about 10% of the full specified possible deviation (full radius):
If the 20µm accuracy is needed on an extended range of deviations, the calculation of the position should take into account the non-linearity of the electrodes signals. As raw data are transmitted to the calculation computer, this is easily achievable.

1-2 Configurations and shaping.

As the system is foreseen to be implemented close to the beam, the collaboration chose to acquire and to transmit electrode raw data in order to simplify the local system. A minimum of code has to be implemented close to the sampling devices, so a local FPGA should manage the board.
No processing as normalization will be made in the local FPGA. The signals are very intense and very short. This energy has to be spread over time using an analog shaping before digitalization.
The solution is to integrate the signal using low pass filters before the ADC.
Finally the sampled signal results in the convolution product of the beam and of the full chain transfer function (BPM, filters). A de-convolution product of the sampled signal and of the chain transfer function will allow the reconstruction of the beam profile.

- Beam configurations: (see also CLIC CDR[2])

The commissioning should allow to increase the beam current progressively.
The nominal beam can be divided in ***121 sections*** of ***24 bunches*** each. So finally, it will represent ***121x24=2904 bunches***, for a total duration of ***241ns***.

First, commissioning should start with ***30 sections*** and with ***1/24 bunch*** per section.
Then with ***60*** and ***121*** sections, with ***1/24 bunch*** per section.
Progressively, sections will be filled up to ***24/24 bunches***.

Excepted for a nominal centered beam, resolutions are not yet specified for the different steps of the commissioning.
The needed resolution for the nominal centered beam is ***2µm***.
So, we estimated the resolution with current electronics performances.

Acquisition should be synchronous with the machine and the minimum time resolution should be about 10ns. So sampling rate should be ***96Msps*** or ***192Msps***.

A final maximum beam deviation is not yet specified but it should correspond to the half aperture, ***R/2=6mm***.

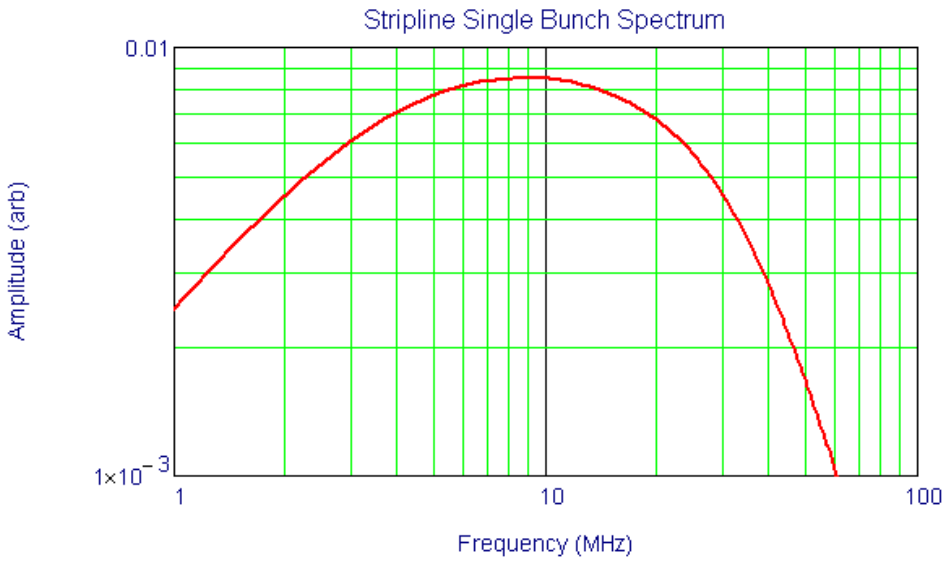
- Signal filtering:

The stripline BPM signals could be exploited in different frequency bands. The band that allows to avoid confounding signals and that allows a good SNR is the baseband. With a train duration of about 240ns, a window of 4-20MHz is a good choice.
The response of the stripline is ~sin(f), so in the baseband region, the BPM acts as a derivative filter because for $\alpha \sim 0$, $\sin\alpha \approx \alpha$. Amplitude increases linearly in function of the frequency.

For good time resolution, filters time constants should be chosen allowing a full integration of the first charge group before the opposed second group arrives about 241ns later.

So a good option is to implement three low-pass filters:
1st order LP @4MHz.
1st order LP @20MHz.
2nd order LP @35MHz.

It corresponds to the following transfer function: BPM + 3 filters:



Note that the final transfer function is a band-pass because of the derivative behavior of the stripline (high-pass).

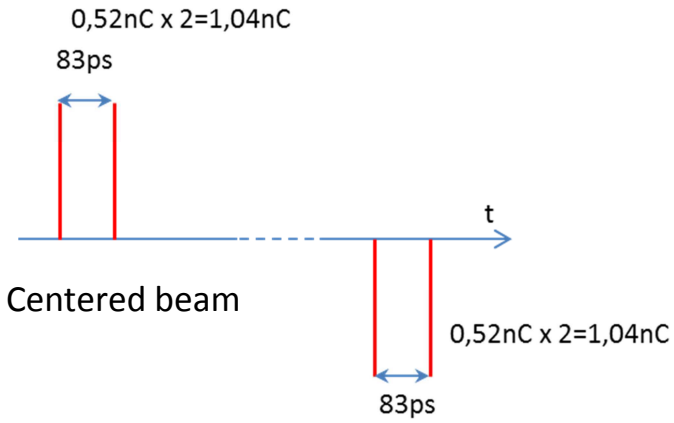
The matching of the readout chain is important to avoid signal reflections in the BPM and so problems of interpretation on signals.
The BPM feedthrough connector brings a 4pF capacitance. So with 50Ω line & termination, a pole should be introduced at about 800MHz. This pole should begin to integrate the charge and limit the voltage due to the short and intense charge pulse.

We can assume that the readout chain has to keep a good matching up to 500-800MHz.

- Nominal beam response:

Two couples of charge pulses create two couples of currents pulses of opposed polarity delayed of about 241ns. As the filters time constants are very high in front of the signals durations, the couples of charges can be grouped to be seen as a single one. Here, maximum beam deviation is taken as ***R/2=6mm***.

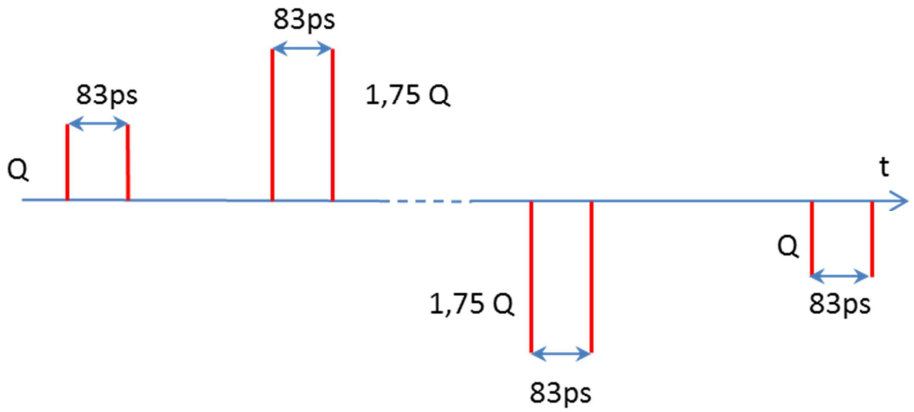
For a centered beam, the charge is ***2 x 8,3nC/(2 x 8)=1,04nC***.
For maximum deviation, the charge is ***2 x 0,52nC x 2,75=2,86nC***.
For minimum deviation, the charge is ***2 x 0,52nC x 0,33=0,344nC***.



The integrating filters have to spread the power of the signal.
Calculations and simulations show that these filters can only be implemented in a passive lumped elements version (cf. *2-3 Stripline BPM shaping and ADC driving stage*).

- 10ns train of maximum deviation:

The R/2 maximum deviation produces a charge on the electrode ***2,75*** times higher than the centered beam bunch. A deviated train of bunches inside the centered beam produces a couple of pulses of ***2,75-1=1,75*** times higher charge because of the cancellation with the opposed charge:



- Beam shape reconstruction, deconvolution, calibration:

Beam shape can be reconstructed by deconvoluting the acquired signals with the response of the chain BPM + electronics to a Dirac impulsion. Originally, the simplest beam configuration was the single bunch beam. Even if not infinitively short and intense, a single bunch spectrum covers well the frequency domain of the signals. The reconstruction could have been performed by deconvoluting the beam signals with the single bunch response.
Unfortunately, the single bunch configuration is no more foreseen so another reconstruction process is to be developed. The possibility to use the theoretical response of the system coupled with an accurate calibration has to be studied in order to allow this reconstruction.

2- Electronic architecture.

We saw that the short pulse has to be spread using analog lumped elements filters. The architecture will be the simpler as possible: matched analog filters, ADC driver and finally ADC.

2-1 ADC choice.

Specifications for stripline BPM acquisition are today:

- Time resolution ~10ns.
- 2µm resolution corresponding to ENOB=12,2 for a R/2 maximum deviation and to ENOB=10,7 for centered beam (cf. 1-1).

As we intend to implement a specific mezzanine for BPM sub-system, we face some constraints: the use of mezzanine limits the number of links on the motherboard-to-mezzanine connectors.
For each stripline BPM we have to acquire 4 electrodes signals.
So we need 4 ADC channels per BPM.

An important issue is to limit jitter on ADC clocks and also to limit gain dispersion between channels of a BPM. This dispersion corresponds to common mode on the deviation measurement.
For these two reasons we think that a quad ADC is a good choice.
This choice brings also other advantages: a single clock generation, a single control, less power consumption.

As we are limited in the number of links on the connector, the solution is to select high speed serial data outputs. This type of ADC should be also the standard in the future. We selected HSMC connectors because they currently allow the highest data rates.

As this system should be implemented in CTF3 first, the ADC sampling clock should be 96Msps, so the ADC should be compatible with this clock.

The 12,2 bit resolution (75,3dB) for signals up to 35MHz means a maximum ADC jitter of:

$$Tj = \frac{1}{2\pi . 35.E6 . 10^{\frac{75,3}{20}}} = 0,8ps$$

So we selected the ***Linear Technology LTC2174*** which is currently, we think, the best compromise between dynamic range, power consumption, architecture and sampling rate:

http://cds.linear.com/docs/Datasheet/21754314f.pdf

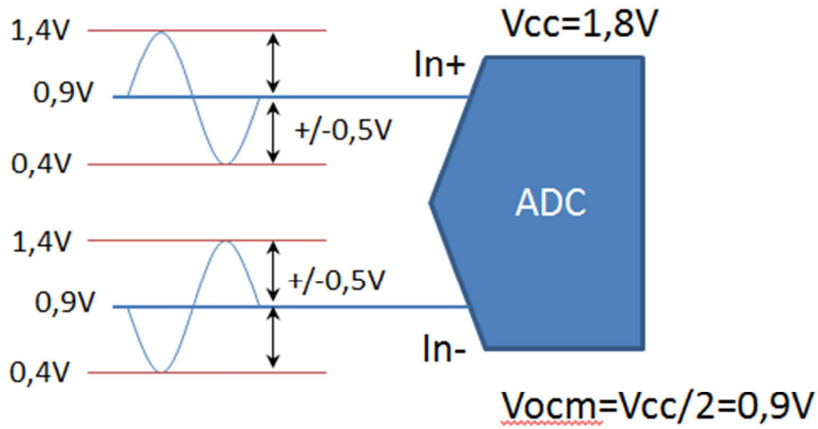
4-Channel Simultaneous Sampling ADC, 14bits.
73dB SNR and SINAD
Sampling up to 125Msps.
Low Power: 450mW, Single 1.8V Supply.
Serial LVDS Outputs.
Selectable Input Ranges: 1VP-P to 2VP-P.
800MHz Full Power Bandwidth S/H.
0,15ps jitter.

The use of this ADC allows to implement two of them on each mezzanine, so a mezzanine could allow two stripline BPMs acquisitions.

The sampling clock has to be synchronized on the machine clock (i.e. 96MHz for CTF3).
With the use of a National Semiconductor jitter cleaner LMK02002 (http://www.national.com/ds/LM/LMK02002.pdf) implemented on the mezzanine, we can reach jitters of ***0,2ps*** so with a good margin in front of ***0,8ps*** needed.

The analog inputs are differential with selectable +/-1V or +/-2V input ranges.
For nominal beam configuration, simulations have shown that we need to attenuate the signals, so we will give priority to the +/-2V range to limit the noise figure but in some cases +/-1V range could be selected.

+/-2V input range corresponds to a maximum +/-1Vpk range on each differential input:



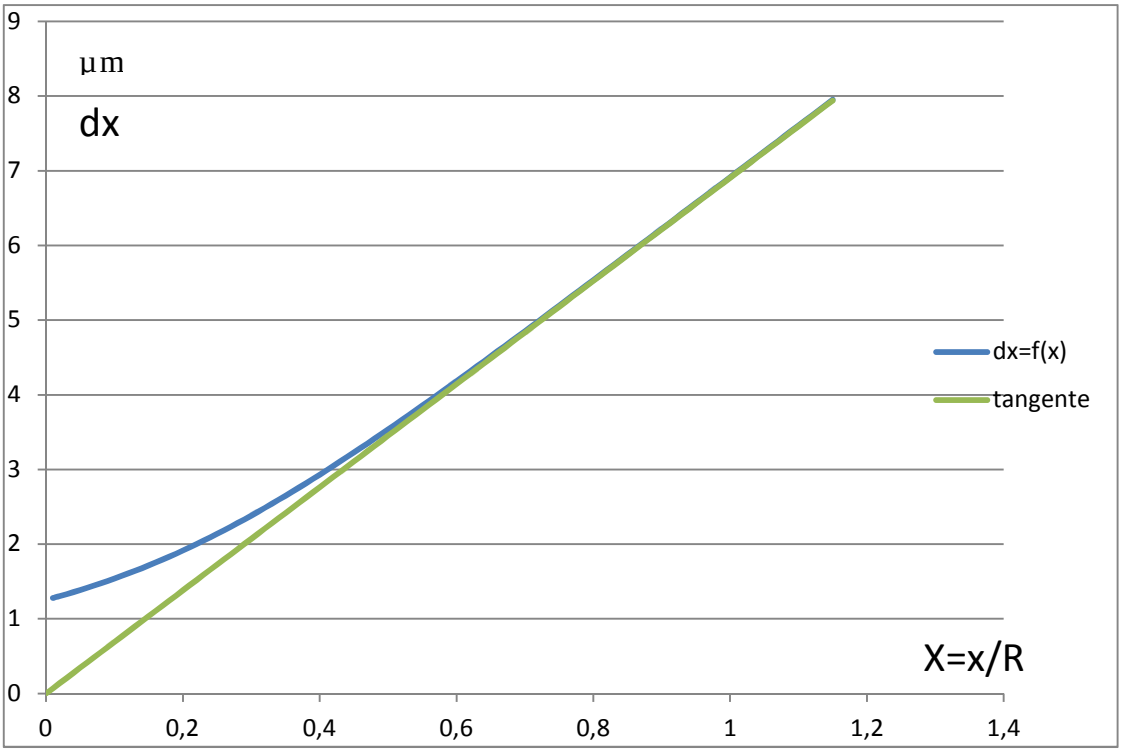
So the signal will have to be shifted to 0,9VDC and will not exceed the 0,4V/1,4V range.
The use of a full differential amplifier to drive the ADC is a good way to shift the DC, to keep linearity and to transform single ended signals to differential (ADC driver).

The ***2V - 11,8 ENOB*** dynamic range corresponds to an input noise of about:

$$\frac{2}{\sqrt{12}.\,2^{11,8}} = 162\mu Vrms$$

2-2 Foreseen resolution.

The announced ***73dB SINAD*** corresponds to an ***ENOB=11,8.***
We tested the ADC and measured ***ENOB=11,7*** which is a good result quite close to the announced value (cf *3- tests results*).
We can trace the theoretical resolution *dx(µm)* in function of the *X* deviation using the formula (1-1 Description of the BPM stripline and specifications):
X is the relative deviation and *x* the absolute deviation, ***X=x/R***.



To reach the 2µm resolution for a R/2 deviation, the needed ENOB is ***12,2bits***, so with this ***11,7bits*** ADC we miss 0,5bit but we think that it is not an issue because it corresponds to a ***~3,5µm*** resolution (see X=0,5).
For a centered beam the resolution should be about ***~1,2µm*** if signals are well scaled with the ADC input range. These numbers are of course calculated for an ADC dynamic range fully used. We will see that except for the first commissioning configuration, it is almost possible.
We can also assume that next ADCs generations should reach higher resolutions and rates. The important thing is that the chosen architecture will not limit the performances in the future: tests on HSMC connectors have shown data rates up to 10Gb/s and 0,2ps jitter. It should limit sampling to ***87dB***, ***ENOB=14,2***.

2-3 Stripline BPM shaping and ADC driving stages.

The analog chain has to shape the signals in order to spread the energy of the short and intense charge pulse. As the BPM acts as a derivative part, the implementation of low pass filters, combined to the BPM, allows to produce a shaping filter. Then, we need to drive these single ended signals to the ADCs differential inputs.
We have to perform three low pass filters:

1st order LP @4MHz.
1st order LP @20MHz.
2nd order LP @35MHz.

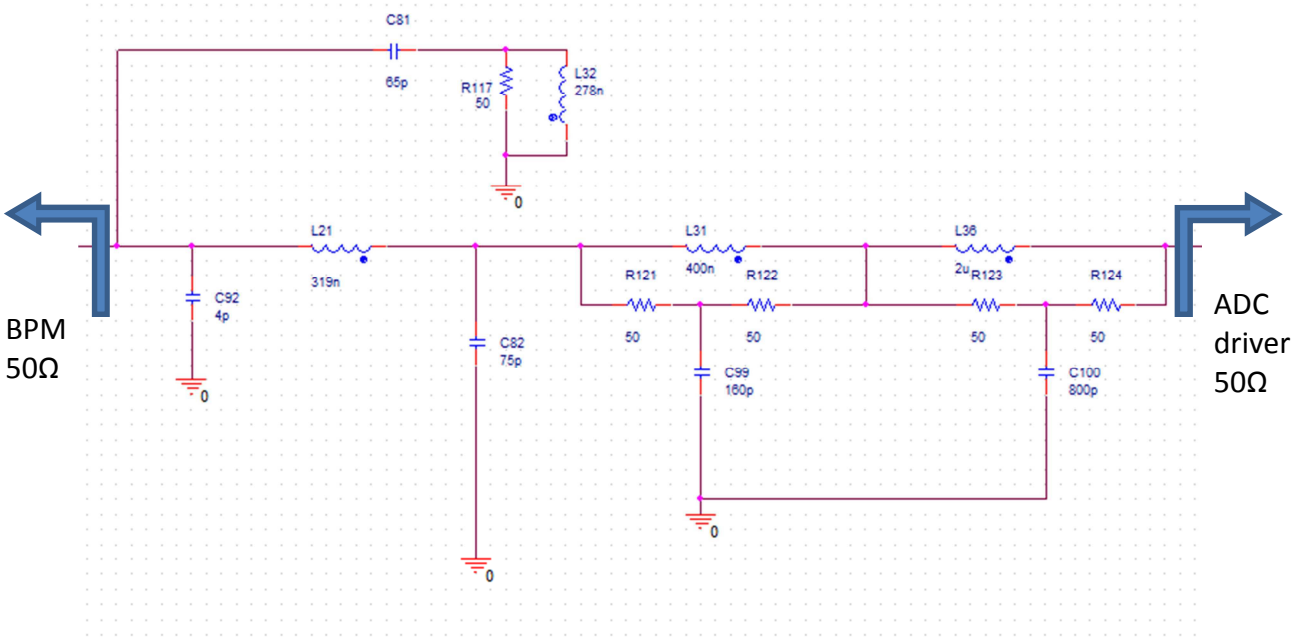
In order to drive the signals to differential ADC we selected the amplifier *Linear Technology LTC6406:*

http://cds.linear.com/docs/Datasheet/6406fc.pdf

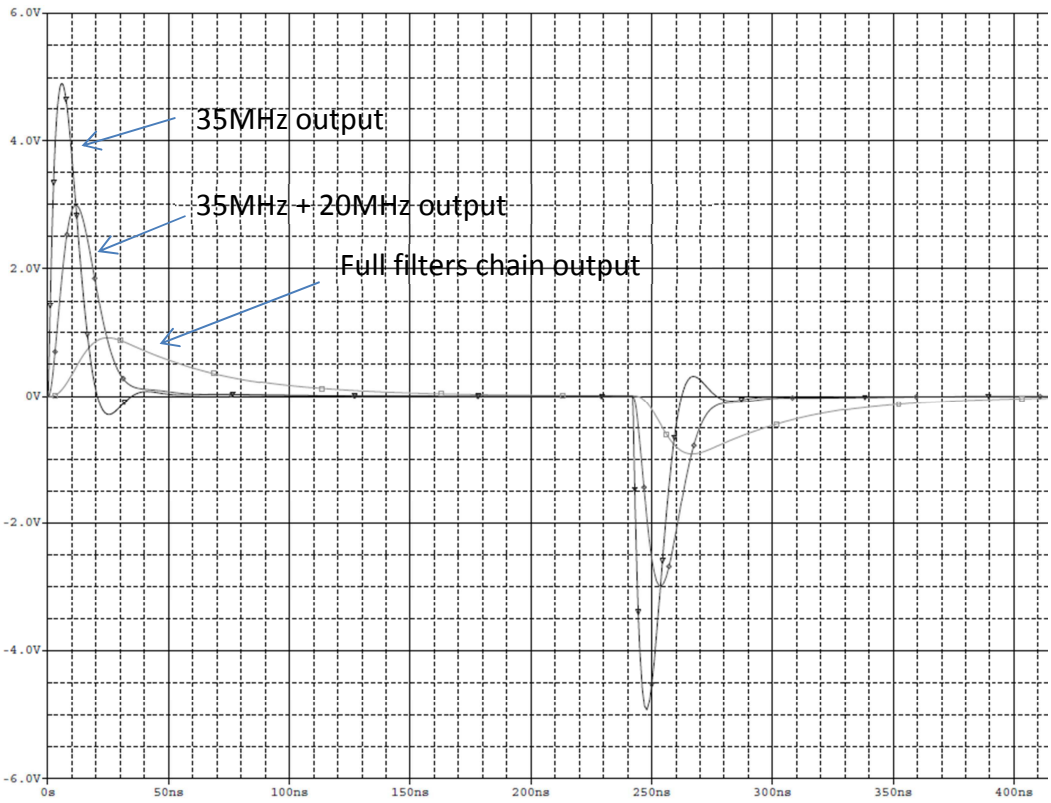
Noise: 1.6nV/√Hz
Power: 18mA at 3V
Distortion (HD2/HD3):
–80dBc/–69dBc at 50MHz, 2VP-P
–104dBc/–90dBc at 20MHz, 2VP-P
Rail-to-Rail Differential Input
2.7V to 3.5V Supply Voltage Range
Gain-Bandwidth Product: 3GHz
Power Shutdown
Compatible with the ADC 0,9Vocm.

2-3-1 *Lumped element input filters:*

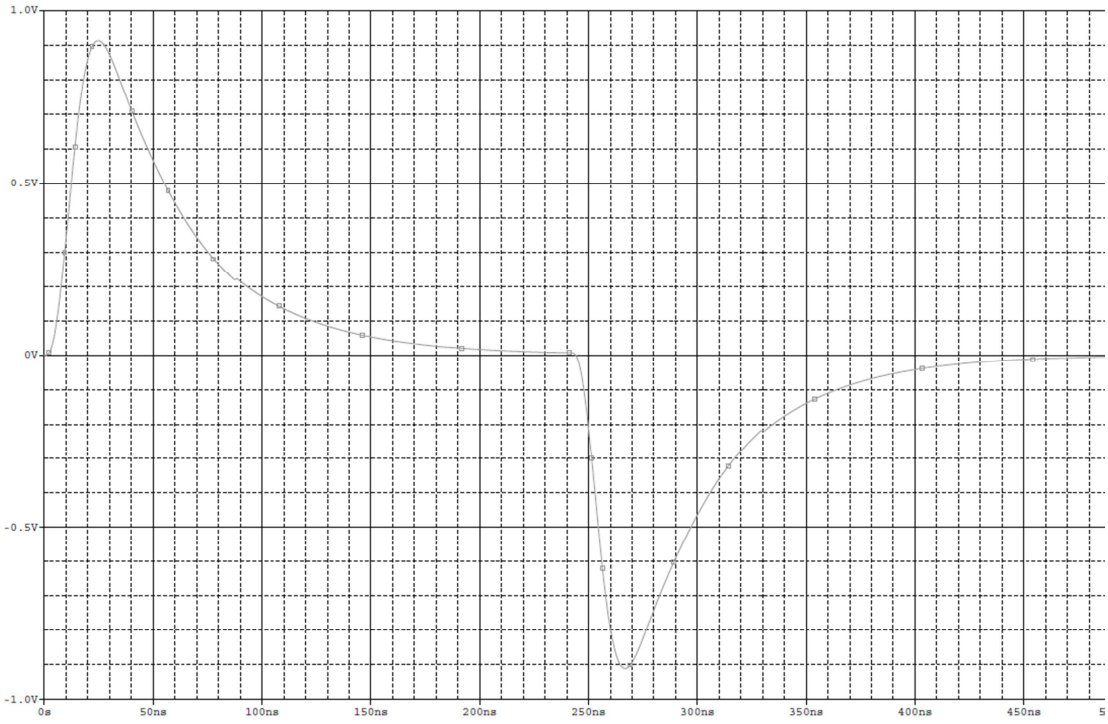
These filters need to be matched with the characteristic impedance of the system, 50Ω. We implemented a 35MHz second order diplexer at the beginning of the electronic chain, then two T-bridge first order filters at 20MHz and 4MHz. In order to keep a good stability we implemented Butterworth filters.



- Time domain characterization: for a nominal centered beam the temporal simulation gives the following results:

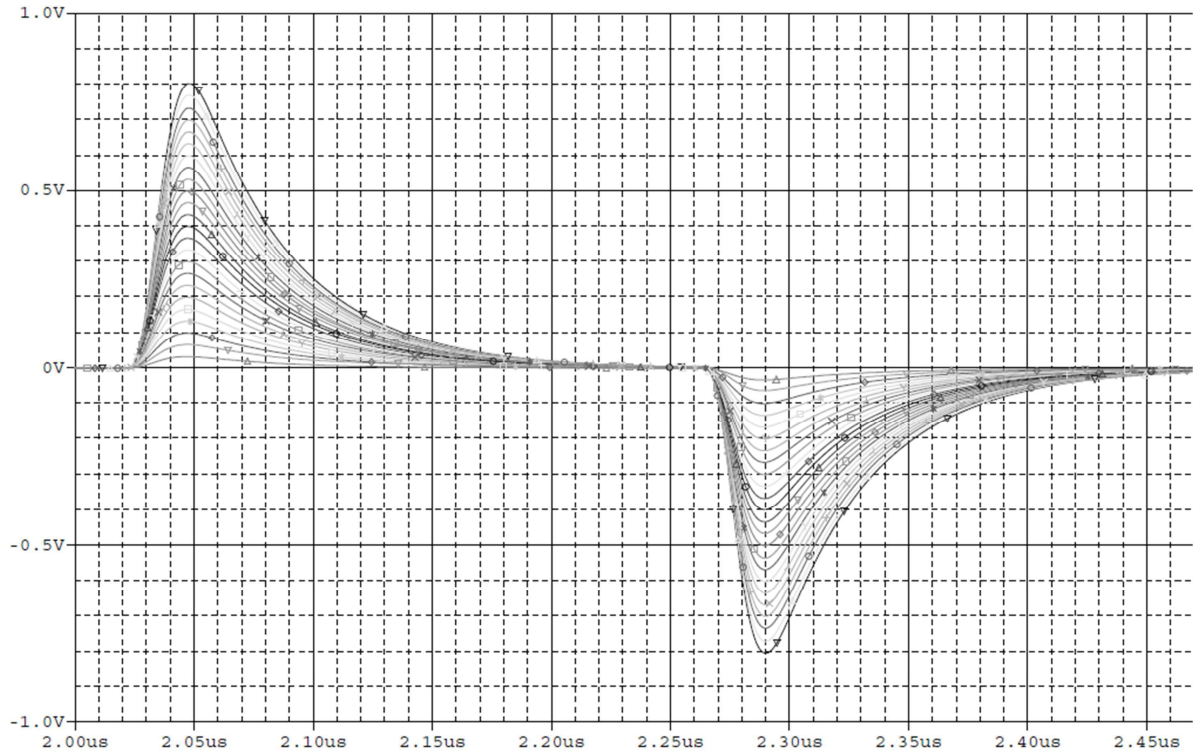


Looking at the chain output:



For a centered nominal beam the foreseen output voltage level is ~800mVpk.
We can notice that the shaping window is well chosen.

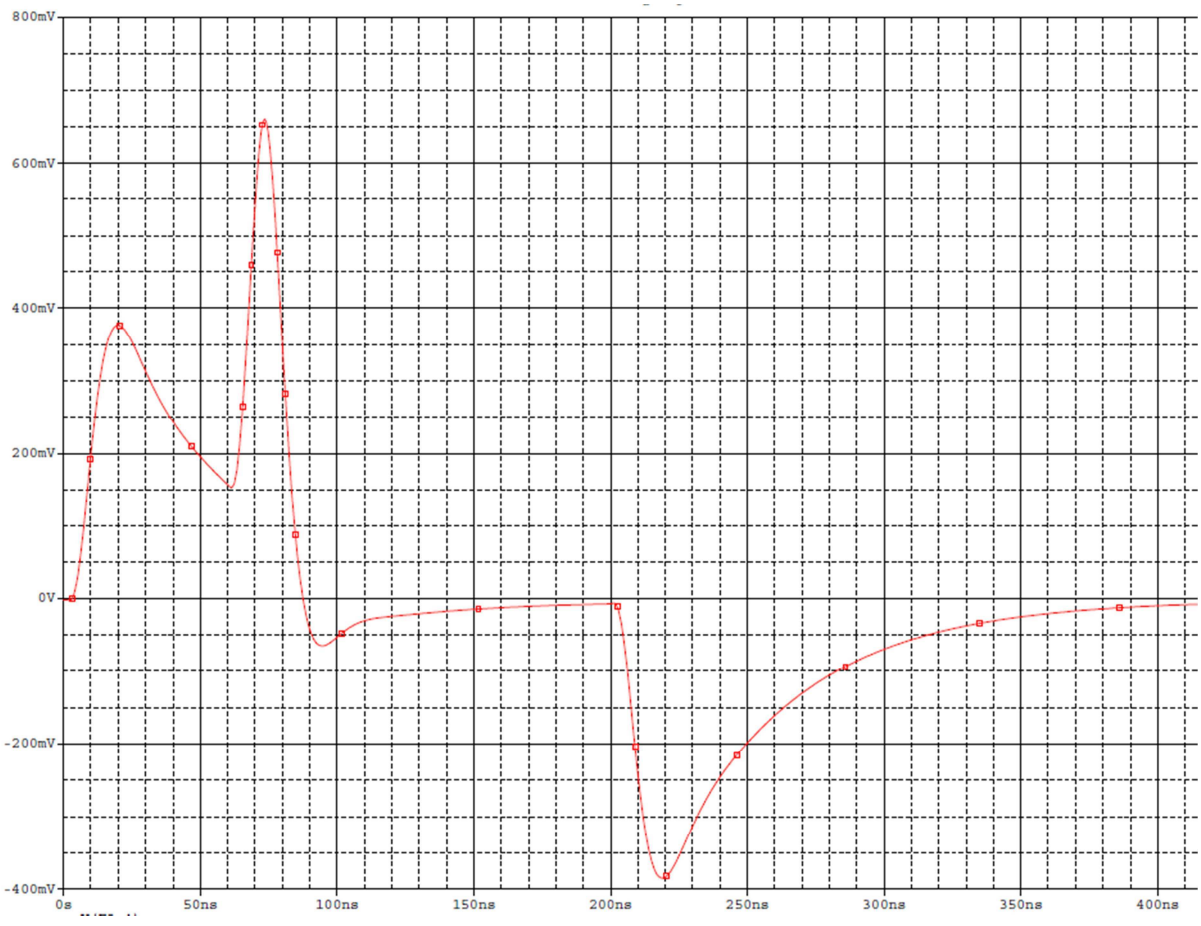
For the different beam configurations, as the inducted charge is integrated, the response will be linear. The following curve shows the output filters voltage for all the beam configurations (see 1-2 Configurations and shaping):



We obtain signals from ~34mV to ~800mV.
If we want to save resolution, this signal has to fit the maximum ADC dynamic whatever the configuration.
So for low signals, low occupied sections, the signals should be amplified.
For a maximum ***R/2=6mm*** deviated nominal beam, we calculated that the signal should be ***2,75*** times higher. As the filters response is linear, the output voltage level should be ***~2,2V***. In this case the signal should be attenuated.

In order to adapt the dynamic range whatever the configuration, we can implement a tunable attenuator and a constant gain on the driver stage. The limitation should be the SNR obtained with such a system (cf. *ADC driver*).

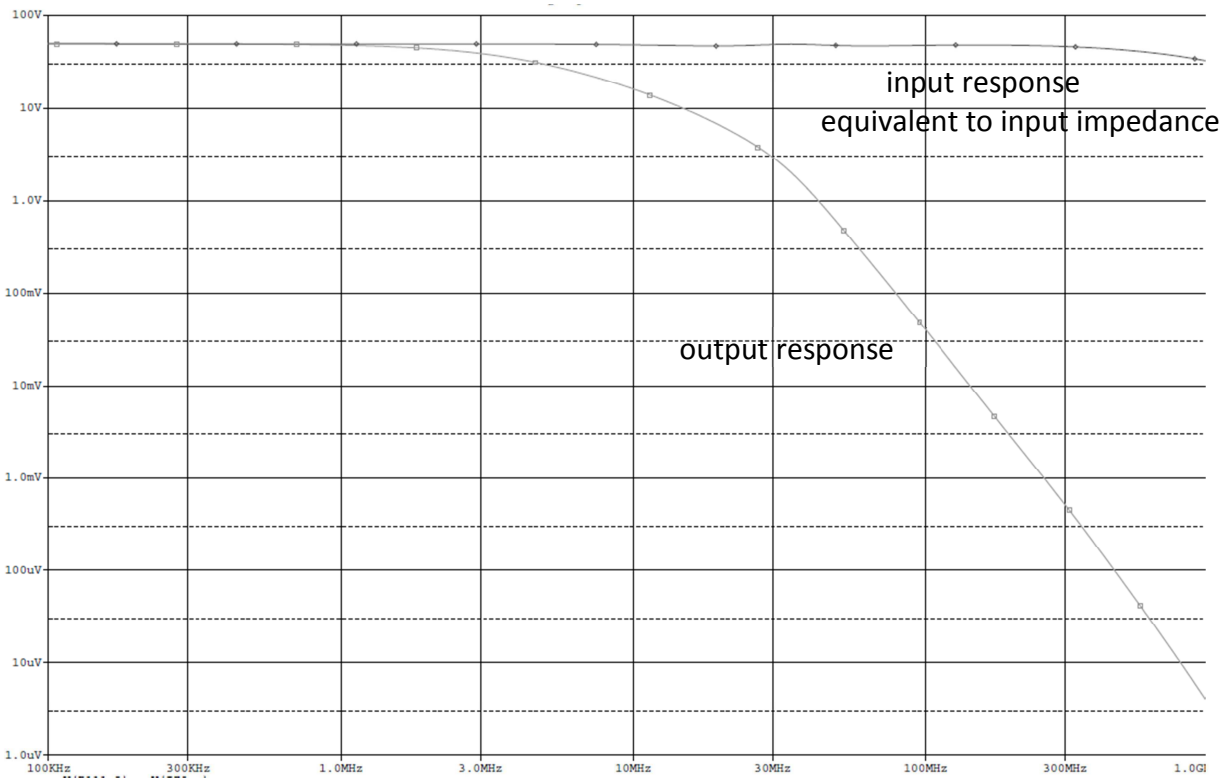
<u>10ns length deviation, maximum R/2 inside a centrered train</u>:
Here, we implemented a -6dB attenuator in order to keep signals in the ADC input range.



Whatever the place and the length of the deviated train of bunches and because of the charge integration, the maximum possible signal will correspond to the signal of a full train deviation.

<u>Remark:</u>
As the filters time constants are very high in front of the bunch duration, filters act as integrators for the stripline bunch charge image. We use them in their "linear" part of the response function. The consequence is that whatever the duration of the signal corresponding to the bunch (with constant charge), the output shaped signal will be the same for bunches lengths up to 1-2ns; i.e. response will be the same for 1nC/10ps or 0,1nC/100ps charge pulses.
It is important for tests and characterization.

- <u>Frequency domain:</u> the following curve shows the simulated transfer function of the filters chain and its input impedance.



The voltage response is simulated for a 1A AC input current generator so the 50V response corresponds to a 50Ω impedance. We can identify the roll-of frequencies and we can notice that the impedance seen from the BPM remains 50Ω up to 300MHz.

2-3-2 ADC driver:

The LTC6406 amplifier allows to transform single ended signals to differential signals plus common mode voltage.
We saw that the ***2V - 11,8 ENOB*** ADC input dynamic range corresponds to an input noise of about ***162µVrms***.
Cutting the output bandwidth of the driver to 50MHz allows to reduce its integrated noise. For small gain implemented on the driver, the dynamic range will be limited by the ADC. So we can use the excess of dynamic of the driver to implement gain and so to save dynamic range for low signals, especially for low commissioning signals.

> *Remark:* regarding to levels at the input of the driver, It could have been possible to implement the 4MHz filter in an active version, directly on the feed-back of the driver. The consequence should be to cut the driver noise bandwidth to 4MHz and at the same time implement the filter. Unfortunately, it introduces a zero on the transfer function that perturbs the response.

We calculated that a ***11,7bits*** ADC allows to obtain a ***1,2µm*** resolution if the scale is fully used, so an excess of dynamic about 2/1,2= ***1,67***. So ***2µm*** resolution should be reached from input voltage level about ***0,6V***.

For g=1 (g, the single ended to differential driver gain), the simulations showed that the response of a centered nominal beam is about 800mVpk (cf. *Time domain characterization*).

For the nominal centered beam, acquisition should have an excess of dynamic range about 0,8x1,67=***1,33***. It means that with g=1, even if the centered nominal beam response does not cover the full ADC dynamic range (typically 0,8V), the resolution is still 2/1,33=***1,5µm***.

We can calculate the maximum gain that we can apply on the driver until degrading the 2µm resolution:
11,7bits correspond to an ADC input noise about ***173µVrms.*** Multiplying by the 1,33 factor of excess, we could stand a total noise, with the driver, of about 173x1,33=***230µVrms***. This should represent just for the driver an output noise about

$$\sqrt{230^2 - 173^2} = 151\mu Vrms$$

Simulations of the driver output noise in function of the gain show that for gains above 2, ***Vnoise#16,4g+19,5***. So we can estimate a maximum ***g=8*** with no degradation of the 2µm resolution.

Minimum signal occurs for n=1/24 bunch per section and is about 34mV.
With g=8 and for different n, the input ADC voltage Vin should be:

n=1, Vin=272mV. dX=(0,6/0,272).2µm#4,4µm.
n=2, Vin=544mV. dX=(0,6/0,545).2µm#2,2µm.
n=3, Vin=816mV. dX=(0,6/0,816).2µm#1,5µm.

From n=4, the digital attenuator should allow to fit the dynamic range.

We can notice that the ***2µm*** resolution could be reached from ***n=3*** for centered beams.

- Future performances considerations:

In the future, ADCs should have better performances in term of SNR. So we will be able to reduce the gain of the driver. We can estimate that with a +/-1V ADC, we could save 2 bits only thanks to this gain reduction.
The idea of implementing LNAs in order to perform the gain was taken into account in this study. It could be possible in the future if resolution becomes an issue.
We decided to not implement LNAs at first for different reasons: high power consumption, not needed in term of current specifications, more complicated to implement in a system that we want to be the simpler as possible (need to be switched). Even if the discussed resolutions are not the final specifications, this study allows to estimate the feasibility of such an acquisition.

- Input impedance with g=8:

The driver input impedance Re depends on the gain because of the resistances set.

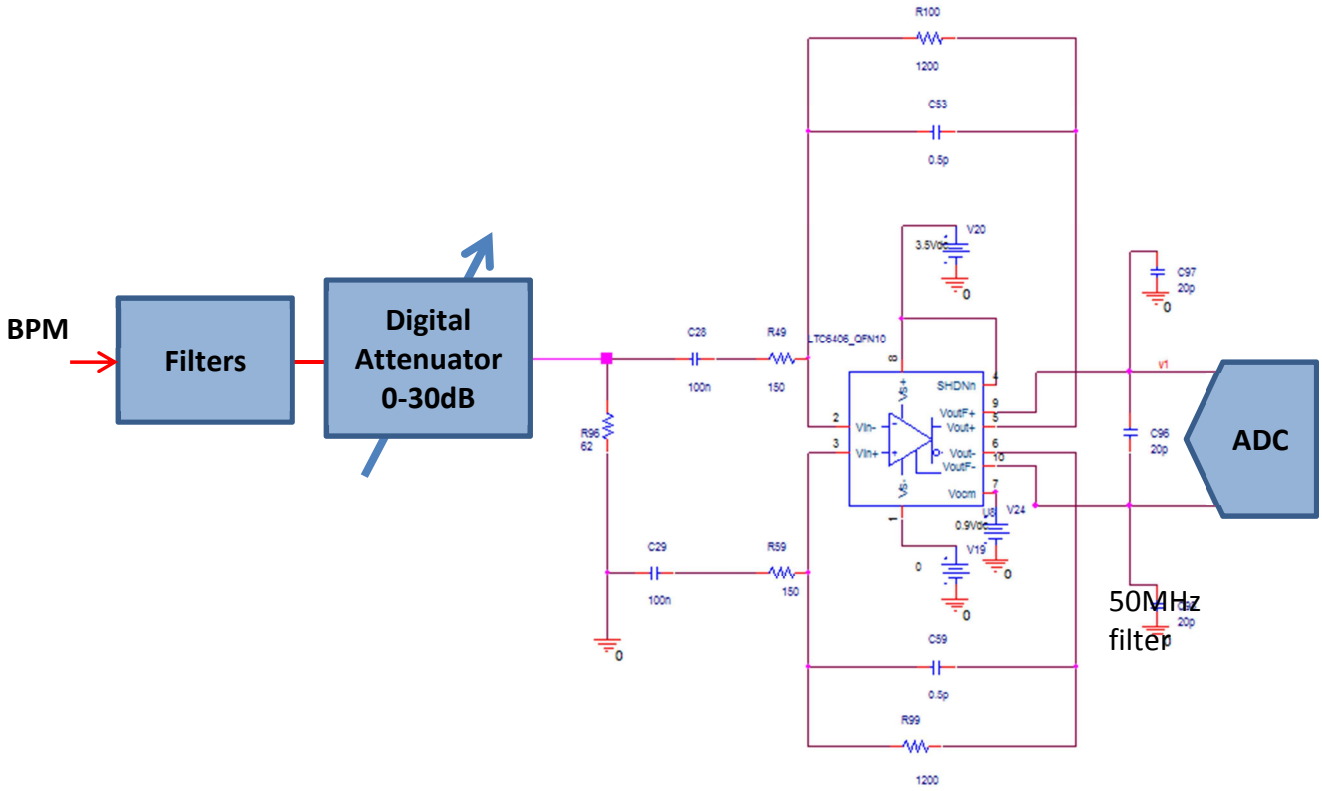
$$Re = \frac{150}{1 - \frac{g}{2(1+g)}} \approx 270\Omega$$

To match a 50Ω input impedance, ***Rin~62Ω.***

- Digital attenuator:

With g=1 we simulated a 0,8Vpk signal for the nominal centered beam. For the maximum deviated nominal beam, the signal should be 2,75 times higher: ~2,2Vpk.
With g=8, we will have to implement a minimum 1/(2,2x8)=1/17,6 attenuator, so ***25***dB.
It should be implemented after filters and before gain for levels issues.
2,2Vpk/50Ω represents about 17dBm.
Digital attenuators are currently existing in versions up to ~30dB, 5bits/1dB steps, 25dBm input.
Attenuators technology is usually GaAs and so naturally more resistant to radiations.

- Electronic chain schematic:

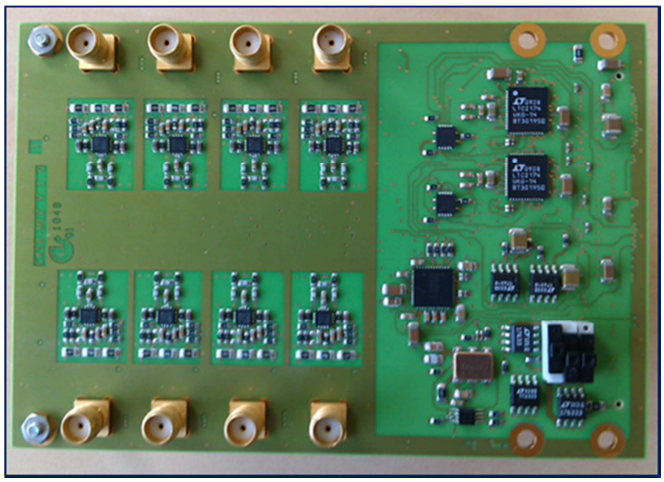


2-3-3 *Multi-purpose ADC driving stage:*

Because we wanted to test first the ADC performances, the data transmission on the HSMC connector, the clocks synchronization and the selected amplifier (LTC6406) before the stripline BPM acquisition itself, we developed a multipurpose acquisition mezzanine. This development answers also to the need to perform a no shaped generic acquisition.

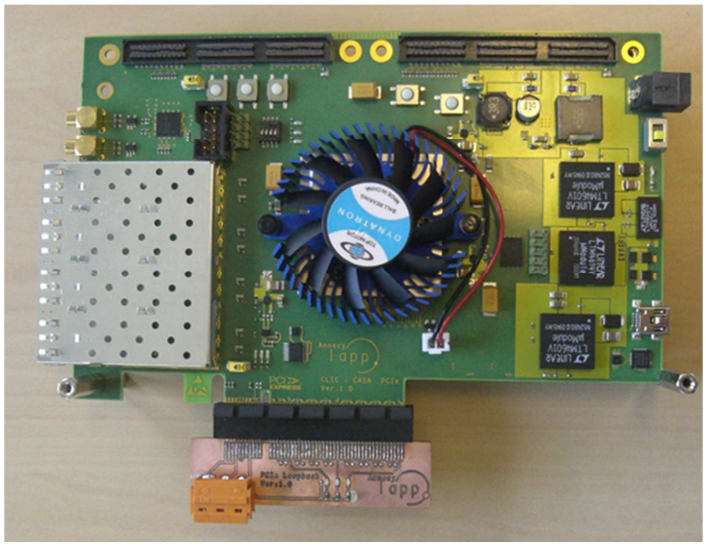
We implemented a gain of 8 and a 26dB attenuator in front to be able to adapt the dynamic range of the chain to different purposes. The foreseen sampling rate is 96Msps and the bandwidth is limited to 48MHz.

The multipurpose acquisition mezzanine:



This mezzanine can be plugged on the evaluation board or PCIe board, already designed for the project, via the HSMC connector.

PCIe board.



3- Tests results: ADC and BPM.

3-1 Tests on ADC LTC2174.

The announced performances are:
73dB SNR, 73dB SINAD.
Integral Linearity Error: +/-1 LSB.
Differential Linearity Error: +/-0.3 LSB.

To test dynamic parameters we used two methods: single tone and two tones injection. We processed 8192 points FFTs for the tests. It represents the typical memory size we can store in the FPGA acquisition.
The tests have to be performed with a generic ADC driving stage that does not shape the signal. So we used the generic acquisition board.
To limit the noise contribution of the amplifier stage we implemented a gain 2 on a 48MHz BW. The theoretical noise should be about 6,88nV/√Hz, so a ***~48µVRMS*** integrated noise. The calculated noise for a G=8 amplifier is 150µVRMS.

- *SNR:*

The noise floor is uniform on the full FFT and can be averaged to -107,5dBc.
It represent a SNR about 107,5-10log(8192/2)=***71,5dB***. It represents an input ADC noise about 189µVRMS.
If we subtract the 48µVRMS amplifier noise, we obtain:
$\sqrt{(189^2-48^2)}$=183µVRMS so a ***11.62bits*** dynamic range, ***SNR=71,7dB***.
The announced SNR is 73dB so a lack of 1,3dB.

We checked this method with the measurement of the noise floor with G=8: SNR=69,7dB which corresponds to a 231µVRMS total noise; The amplifier noise is about 150µVRMS so the difference is 176µVRMS which represents a ***11,68bits*** dynamic range and a ***SNR=72,1dB***.

Finally, we can estimate the ADC SNR to ***72dB***; ***11,7bits***.

- *Single tone:*

We used the Tektronics AFG3252 arbitrary function generator.
Because of its internal construction, it gets good results in even harmonics.
With a 10MHz sine, the ***H2*** harmonic is ***-74dBc*** and the ***H3*** is ***-52dBc***.
These levels allow to relax the filter order needed to measure the ADC nonlinearity.
With a simple L-C 10MHz 2nd order, we are able to reject H2 (20MHz) by a factor ***-26dB*** and H3 (30MHz) by a factor ***-44dB***. It means a theoretical ***-100dBc H2*** and ***-96dBc H3***. It is difficult to verify these numbers with even a good spectrum analyser because these numbers reach the linearity of the device.

We observed ***-87,3dBc*** for ***H2*** so a theoretical lack of 12,7dB and ***-95,6dBc*** for ***H3*** which is the waited rejection.

The ADC measurements give ***-88,3dBc*** for ***H2*** and ***-79,3dBc*** for ***H3***.
As the ADC rejection is superior to the rejection observed with the spectrum analyser we can assume that the lack of rejection is due to the analyser nonlinearity and so we can trust the ADC rejection for the SINAD calculation.
The higher order levels are not significative (under floor level or inferior to -100dBc) , the SINAD can be calculated using H2 and H3:

$$SINAD = \frac{Psignal}{Pnoise + PH2 + PH3}$$

With Psignal, PH2 and PH3 the signal powers. The tests have been performed with Psignal=-6,7dBm.
Scaling the powers to the full scale, Pnoise=-72dBFS, Psignal=0dBFS, PH2=-88,3dBFS and PH3=-79,3dBFS.
So we obtain ***SINAD=71,2dB*** which corresponds to a dynamic range of ***11,5 ENOB***.

Remarks:

- We obtain the same results using coherent sampling or incoherent sampling with windowing.
- We used also a two tones method to estimate the nonlinearity. The advantage of this method is to measure ADC nonlinearity with no incidence of the function generator nonlinearity. We chose F1=11MHz and F2=13MHz. The results are not so easy to interpret because differences in levels of symmetrical products. However, the results are the same.

- *Integral nonlinearity, DNL:*

The INL should be better than 0,18% to reach the 20µm precision.
For a 14bits ADC It represents 9,12bits so 4,88 spare bits: so a maximum allowed limit of ~29LSB INL. The LTC2174 is given for a maximum worst case INL about +/-3,25 LSB so we can assume that it gives a large margin.
Its worst case +/-0,8LSB DNL insures its monotonicity.

Conclusions:

The measured SINAD is slightly less than announced by Linear Technology; 71,2dB for 73dB announced. It corresponds to a measured effective number of bits of ***11,5*** for 11,8 announced. This difference can also be due to the accuracy of our system or unexpected noise contribution degrading the noise floor.
The observation of nonlinearity shows that the dynamic range will be limited by the noise floor as announced (SNR≈SINAD).
These tests showed the good performances of the multipurpose driving ADC stage:

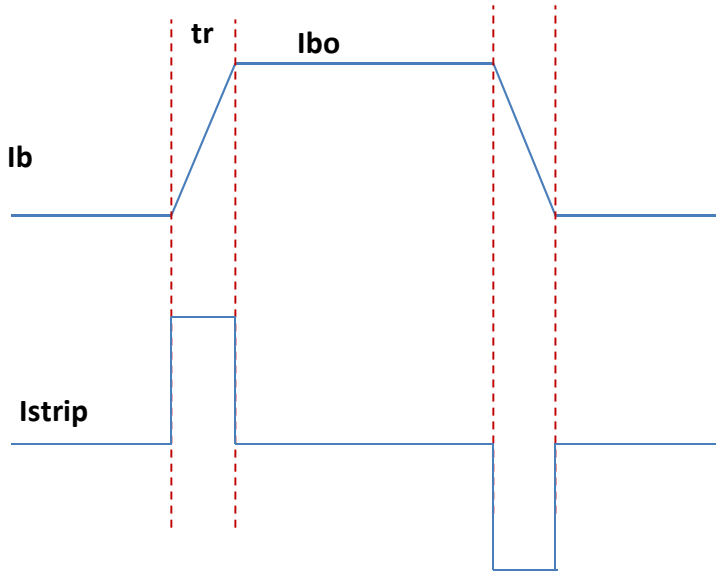
- LT6406: good general performances at needed VOCM=0,9V.
  Good linearity and noise results.
- HSMC connectors good for high speed data transmission.
- Validation of the architecture around the ADC: clock management, jitter cleaning…
- Stability of the acquisition and processing between FPGA and ADC.

3-2 Stripline BPM tests.

In order to tests the BPM in lab., we should be able to reproduce the beam. The common way to test a BPM is the wire method: placing a well known impedance wire inside the BPM and injecting a current. This current should have the same structure than the foreseen beam.
The stripline BPM acts as a derivative part for low frequencies. We saw that, for a nominal train of bunches, it recovers the two first and two last charges.
We are not able to perform a 12GHz signal on the wire but we can inject a current pulse, which derived by the stripline corresponds to the expected charge.

Filters act as integrators for the stripline bunch charge image. Whatever the duration of the signal corresponding to the bunch (with constant charge), the output shaped signal will be the same for bunches lengths up to several ns; i.e. response will be the same for 1nC/10ps or 0,1nC/100ps charge pulses.
Even for very long pulse integration (>20ns), the response is very close (10%) and should allow to characterize the BPM.

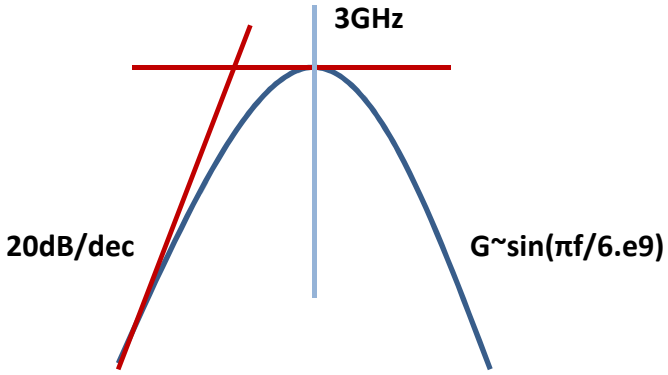
The aim is to inject an high current pulse with a short and linear rise and a constant amplitude: the BPM derives this current and the stripline output should be a pulse.



With Ib the injected current on the wire, Istrip the stripline output current and tr the rise time:

$$Istrip = \tau_0 \frac{\delta I_b}{8\delta t}$$

With a centered beam, a stripline recovers the eighth of the wire current.
The BPM acts as a high pass filter for the low frequencies.
We can calculate its equivalent time constant by tracing the tangent of the transfer function:



The BPM transfer function is *G~sin(πf/6.e9)*
For low frequency, we can assume that *G~πf/6.e9* because *sin(f)~f*.

So identifying with a normalized G=1, the fo cut-off frequency is:

πfo/6.e9=1 so fo=1,91GHz

It corresponds to a time constant about τo=83ps.

If the rise/fall time is linear, with Ibo the amplitude current plateau after the rise:

$$Ib = t.\frac{I_{bo}}{tr} \quad so \quad \frac{\delta I_b}{\delta t} = \frac{I_{bo}}{tr}$$

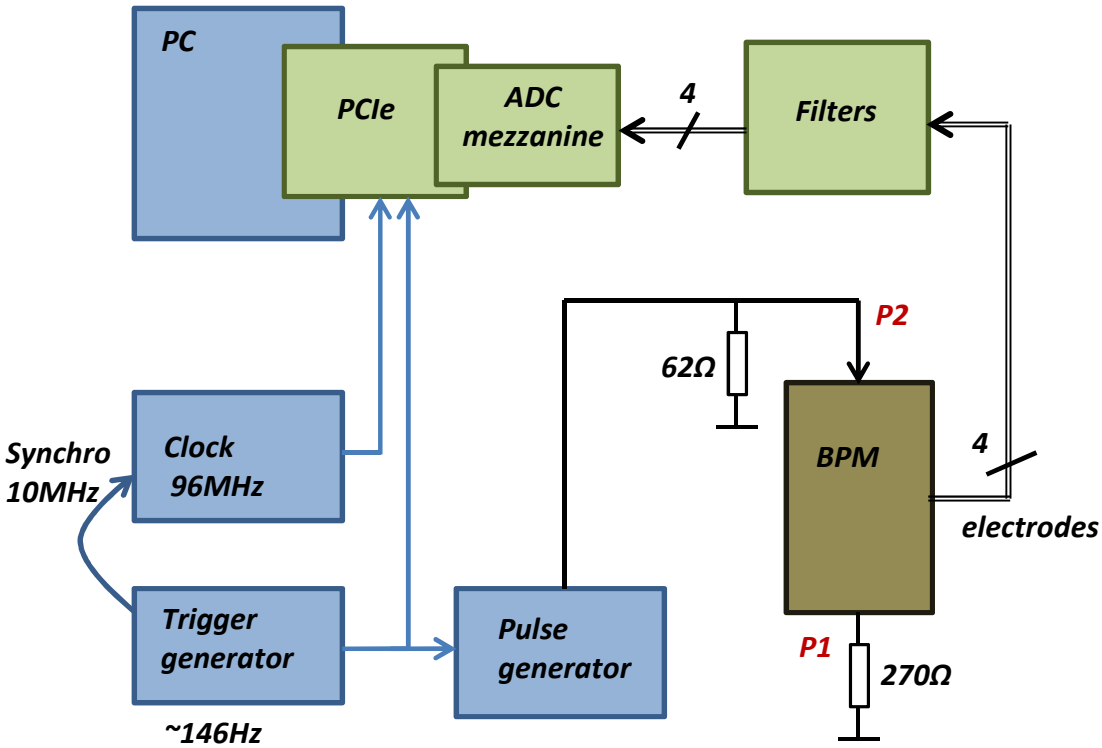
Finally,

$$Istrip = \tau_0 \frac{I_{bo}}{8.tr}$$

For a centered nominal beam, we saw that the stripline recovers a total charge about 1,04nC.
We developed a current pulse generator with tr~15ns, 10A/50Ω.
An important issue is to match the input impedance of the system wire/BPM with the pulse generator.
This system input impedance has been measured to ~270Ω using a TDR.
We implemented a 62Ω resistance at the input of the system in order to see (62//270)=50Ω.
Even this resistance doesn't allow to use the full capability of the generator because of the formed divider (62/62+270), it allows to inject neatly ~19% of the pulse.

- *Test set-up:*

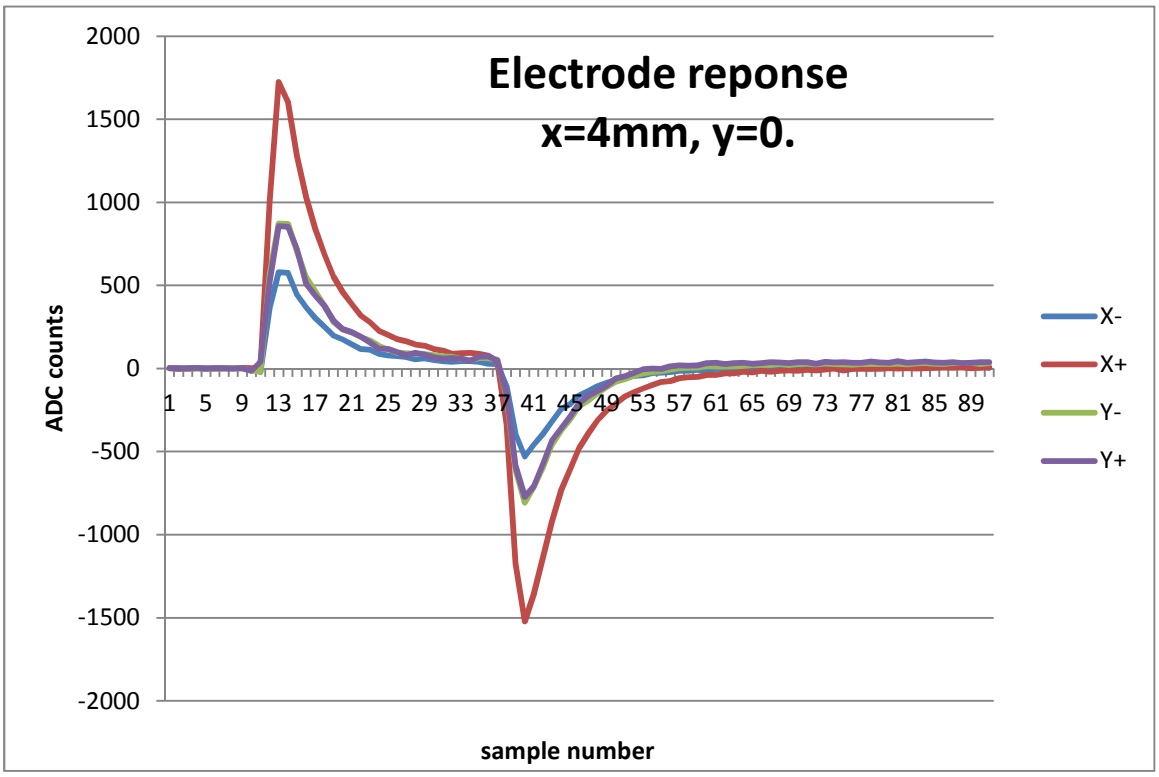
Thanks to the CERN BI-PI's wire test bench, we realized two series of tests.
We used the following test-bench:



Because the BPM is foreseen to be installed in CTF3 we did tests with a 96MHz sampling clock reference. The PCIe express hosts here the acquisition mezzanine and is plugged on a computer. This computer allows the data collection.
As in the machine, we have to provide a synchronous clock and a beam trigger to the PCIe. The ADC samples continuously the BPM signals and a FPGA FIFO is fed in. When receiving the trigger, the FIFO is frozen with a delay corresponding to the length of the wanted data window and the latency of the full system. Then data can be sent to the PC via the PCIe bus. Clock and trigger have to be synchronous. As the current is generated by discharging capacitances, the trigger rate cannot exceed a maximum frequency (typically 500Hz). So the principal issue of the timing is to produce synchronous clock and trigger with very distant frequencies.
As we already developed a multipurpose mezzanine, we performed filters in a stand-alone version.
A software has been developed in order to process the data.
It allows to calibrate the offsets, to tune the length of the data acquisition window, to average the data on a configurable number of windows, to seek the maximum of the curves… It also allows an on-line reconstruction of the pulse by a deconvolution processed with a theoretical transfer function.
The BPM was previously aligned. So, first we calibrated the Acquisition chain alone and then we calibrated the electrical + mechanical center.

- *Test results:*

We typically obtained the following curves: for instance, a 4mm deviation on the X axis, no deviation on Y axis.

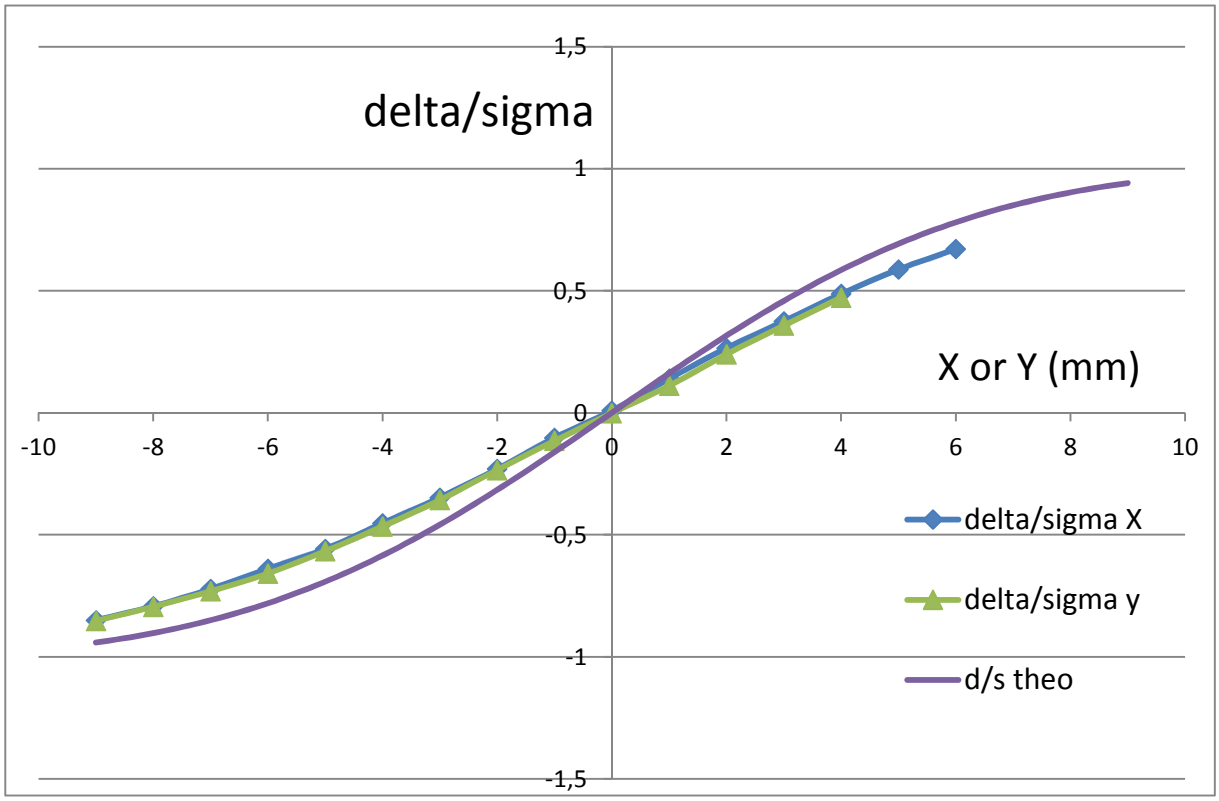


The response is the same on the two Y electrodes and the response of the electrode close the wire (X+) is larger than the far one (X-).

Sweeping the X and Y axis we can acquire the set of electrodes signals and process the sensitivity curve using a reference value. The peak value offers the best SNR.
The system needs a perfect synchronization of the sampling clock (96MHz) with the current pulse whose repeats at about 146Hz.
This low repetition rate is due to the architecture of the generator. It allows the charge of the internal capacitors. Because of the very large ratio between these two frequencies and because of drifts in the generator, it was difficult to sample the curves every time at the same place.

We noticed fluctuations on several measurements for the same position, so we implemented an average on a number of windows. Searching the averaged maximum values for the two set of curves, we calculate Δ/Σ.

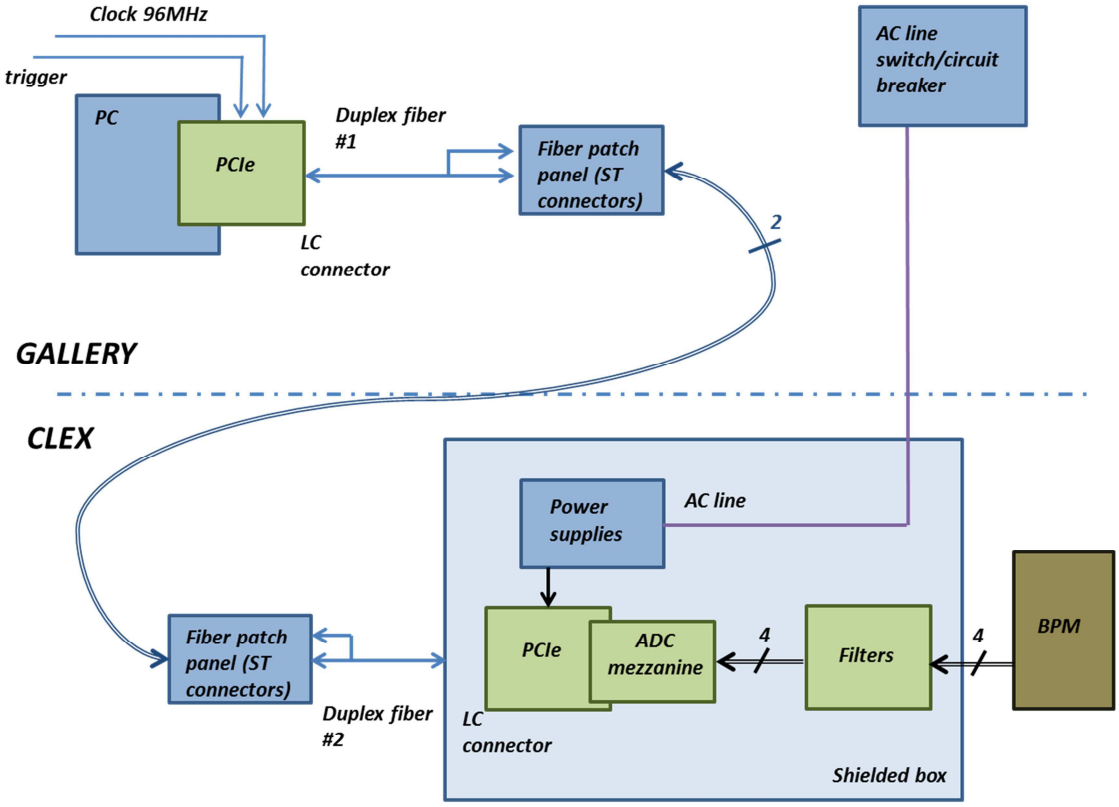
Sweeping X and Y axis, we obtained:



The experimental curves (green and blue) show a normal shape but we noticed a tilt in the slope corresponding to a lower sensitivity than the theoretic model (d/s theo, violet).
Even if the high frequency tests show that the BPM does not act as foreseen (cut-off frequencies, length of electrodes…), it does not explain this sensitivity shift. A second tests session showed the same behavior. We also noticed an abnormal behavior in the return to zero of the first shaped pulse. It could correspond to a charge storage in the set-up. So a charge storage and an impedance mismatch should be the most probable causes of the sensitivity shift.

- *CTF3-TBL Test set-up:*

The next step is the tests of the BPM on the CTF3 TBL line. It should allow us to qualify the sensitivity with no set-up constrains.
We installed beginning January the following electronics in CLEX-TBL:



We use the PCIe board (cf 2-3-3) in a stand-alone configuration in the accelerator and a second PCIe board plugged in a computer in the gallery. This system will allow to qualify BPM and its front-end electronics but also it associated network. This network [1], based on the use of a single optical link, should allow to transmit the data and timings by forcing the carrier and so to perform synchronous acquisitions with the machine. Collaboration with CERN CO should allow to recover data with compatibility with the CERN back-end infrastructure in the future.

4- Beam reconstruction, calibration.

4-1 Beam reconstruction.

The four digitized electrodes signals correspond to the beam responses after filtering of the BPM itself plus the shaping filters implemented in the electronics. If the global transfer function (BPM+filters) is well known, we should be able to reconstruct the beam image by dividing the frequency spectrum with this transfert function. It corresponds to a deconvolution in the time domain.
As the energy spectrum spread by a single bunch is constant on the frequency bandwidth of the transfer function in the needed dynamic range, single bunch should be a good way to calibrate the BPM.
Unfortunately single bunch configuration is no more foreseen in the CLIC.
An accurate calibration is also needed in order to reach the reconstructed beam resolution. Calibration's principal role is to measure the gains of the four chains. If not known, differences on gains introduce offset and tilt in the sensitivity.
Calibration could be sufficient to measure the gains and the transfer functions if it is enough accurate.

The reconstruction process is the following:

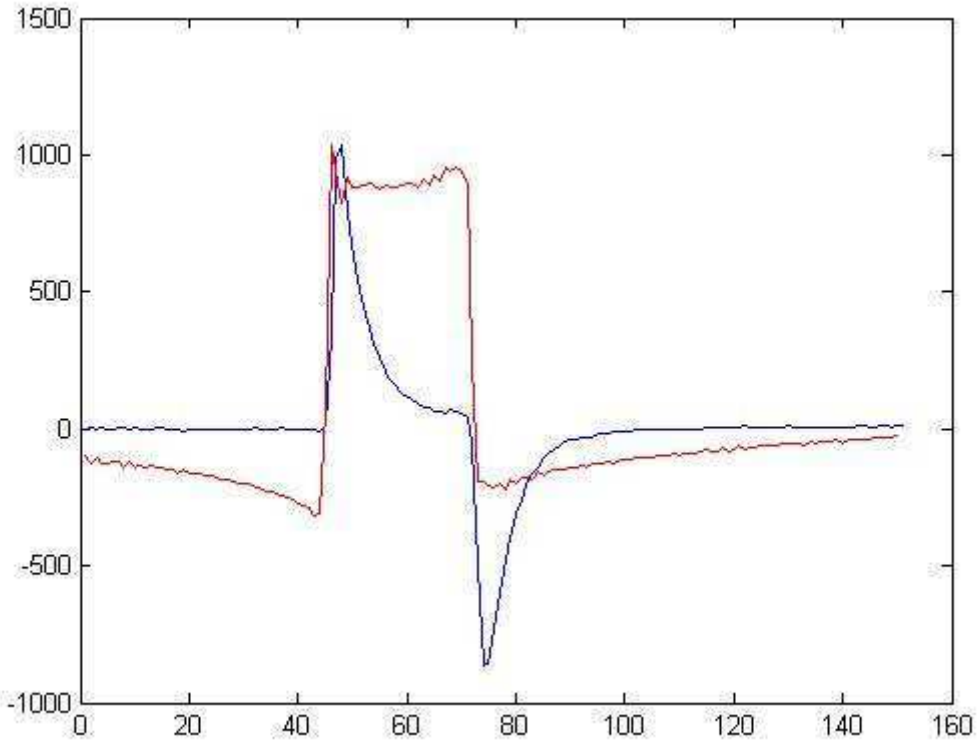
- Process a Fast Fourrier Transform of the four acquired windows.
- Divide point-to-point these spectrums by their corresponding transfer functions.
- Process an Inverse Fast Fourrier Transform.

Then the four reconstructed beam images can be processed by differences/sums in order to obtain the X and Y positions.

The calculations are foreseen to be performed in the frequency domain for two reasons: calculations (divisions) are faster than deconvolutions and the "real" measured transfer function can be directly corrected.
The window acquisition should not exceed about 200 points, even future 5ns sampling over 1µs. So FFTs and the reconstruction are very fast.

We performed first tests of deconvolution with Matlab software on simulated beams with success.
We also developed a specific on-line software which performs the full process.

Processing the wire test values, we reconstructed a deformed pulse (not square) whatever the soft we used:

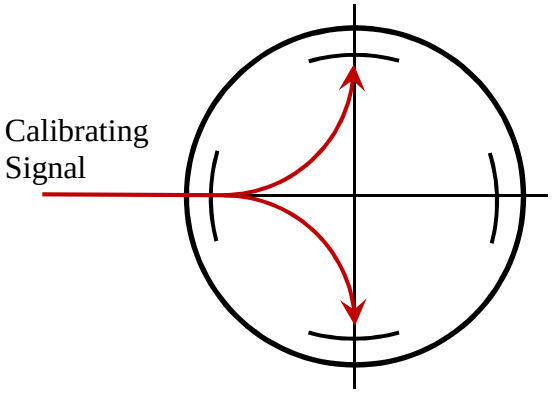


We can notice there is a problem at the foreseen zero levels before and after the pulse. It can be explained by the problem already discussed in the tests section.

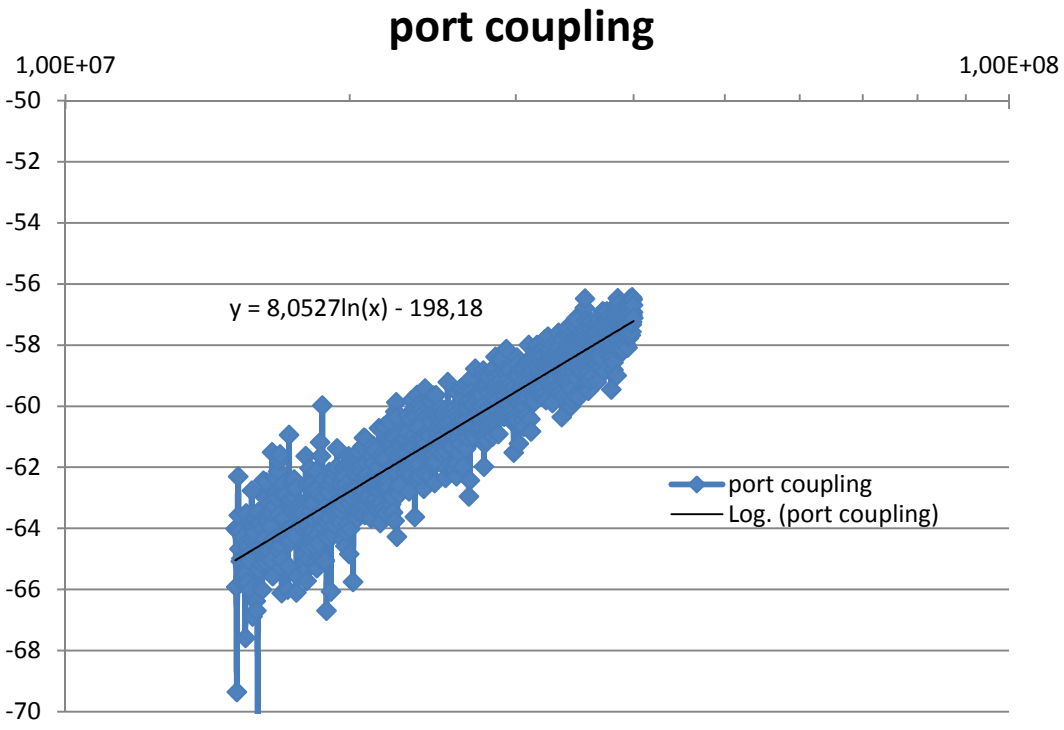
Tests with Matlab soft show that the resolution is not degraded by the FFT-IFFT process. The resolution/precision of the FFT-IFFT process is first limited by the used data format.

4-2 Calibration principles.

As discussed in 4-1, an accurate calibration is needed in order to compensate gains variations but it could also replace the single bunch response measurement which was foreseen in order to obtain the transfer function of the BPM+electronics chain.
The vertical and horizontal positions are calculated using the two opposite electrodes respectively. The calibration should allow to measure the differential gain between two opposite electrodes and the transfer functions. A difference between gains can be seen as a position offset and tilts the sensitivity too. A simple way to perform this calibration is to inject a signal on one of the two perpendicular electrodes and so to use its coupling with the two electrodes under calibration.
Of course these gains represent the magnitudes in the transfer functions.



Couplings have been measured on a high frequency test bench:



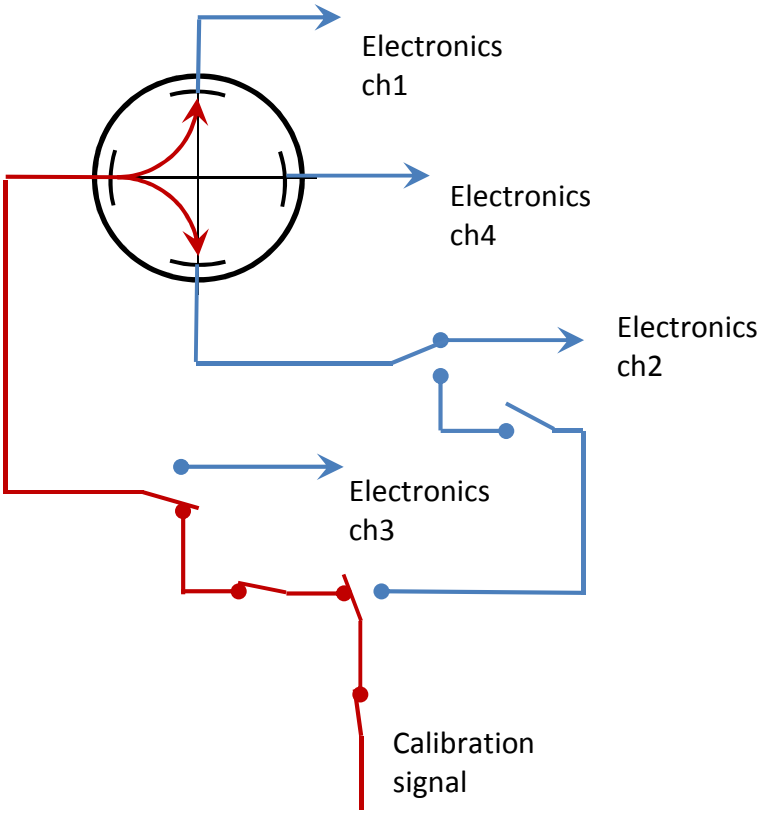
Fitting the curve (the curve shown is just an extracted part of the total curve), we obtain the following global behavior:

$Y=8,053.\ln(f)-198 = 8,053.\log_{10}(f).\ln(10)-198 = 18,53.\log_{10}(f)-198$

As 18,5#20, this equation corresponds well to a derivative 1st order.
So we can conclude that for the band we work within, the BPM response is the same in electrodes coupling mode than in beam-electrode coupling mode. This result is the theoretical waited result.

So we can estimate the coupling at 4MHz which corresponds to the gain of the BPM+electronics transfer function plateau:
$18,53.\log_{10}(4E6)-198=$**-75,7dB.**

We could implement a system as follows :



The ch1 and ch2 channels are calibrated by switching the calibration signal to the ch3 electrode. The ch3 and ch4 channels are calibrated by injecting the signal on ch2 electrode.
When the calibration signal is connected to ch3 or ch2, we have to ensure a minimum coupling with the acquired channels. Typically, this coupling should not exceed the maximum acquisition dynamic range, so about 80dB.
GaAs switches reach typical isolation about 30dB in our bandwidth. So we can add serial switches which only role is to increase the isolation.

Switches losses are about 0,5dB, so 4 serial switches add a total -2dB loss.
Finally, the calibration coupling between electrodes should be about **-78dB**.

- Calculation of the resolution with unmatched gains:

Recalculating the resolution with the introduction of two gains, g1 and g2, corresponding to the gains of the BPM+electronics chain, we obtain:

V1'=g1*V1, V2'=g2*V2.
V1' and V2' are the acquired voltages, affected by gains.
V1 and V2 correspond to "perfect" voltages.
As these gains should not vary in function of the deviation and because their measurement using calibration configuration corresponds to a centered beam, we estimate the new resolution for a centered beam:

$$X = \frac{R}{2}\frac{\Delta}{\Sigma}$$, Δ=g1V1-g2V2, Σ=g1V1+g2V2.

Finally,

$$\delta X = \frac{R}{2}\left(\frac{\sqrt{g1^2 + g2^2}}{g1 + g2}\right)\frac{\delta V}{V}$$

Remark:
With g1=g2=1, we find again $\delta X = \frac{R}{2\sqrt{2}}\frac{\delta V}{V}$.
The tolerance that we can afford depends on the margin of the acquisition dynamic range. With the tested ADC, the foreseen resolution for a centered beam is about 1,2µm while the specification is 2µm. For instance +/-50% on gains – so, g1=1,5 and g2=0,5 - results in an increase of the resolution by 12% so 1,34µm.

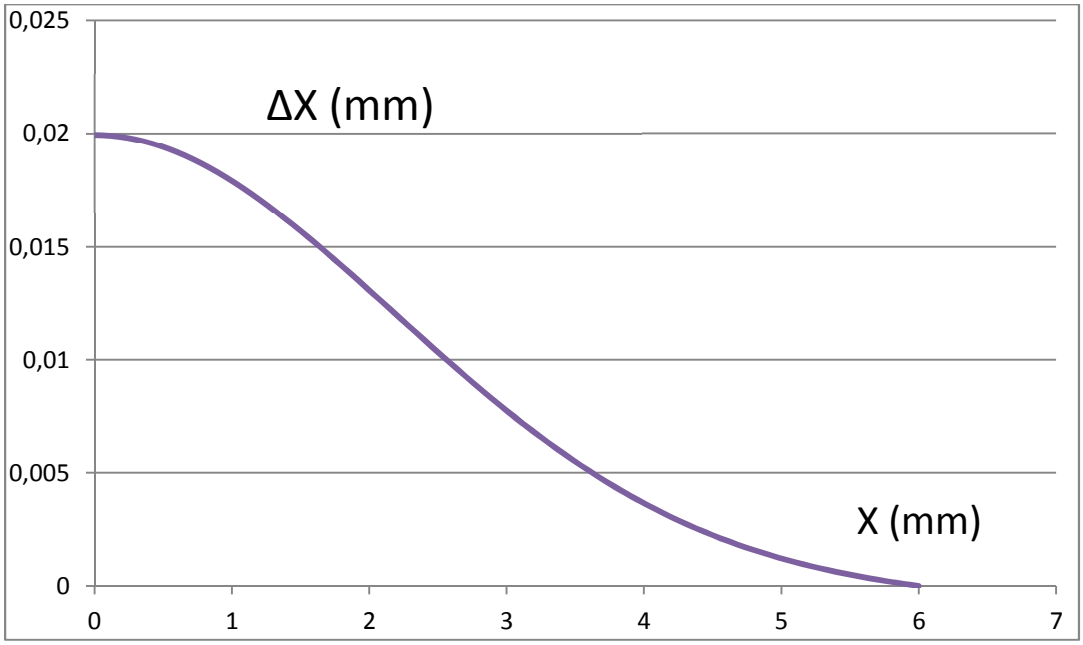
We can conclude that with a minimum of resolution margin, due to ADC dynamic margin, large variations of gains do not affect the resolution.

- Calculation of the precision with unmatched gains:

Gains variations affect directly the result of the calculated deviation: for centered beam,

$$X = \frac{R}{2}\frac{\Delta}{\Sigma} = \frac{R}{2}\left(\frac{g1V1 - g2V2}{g1V1 + g2V2}\right)$$

We can compare this deviation to the recalculated perfect deviation
X (for g1=g2=1) by calculating their difference ΔX.
We can estimate the maximum gains shifts that allow to keep the accuracy in the precision specification, 20µm.
Tracing ΔX in function of X and for a maximum ΔX of 20µm, we obtain:



We can notice that precision is degraded the most at the center.
We obtain this maximum ΔX value for the couple g1=1,00665 and g2=0,99335 which represents about 0,67% opposed gains variations.
We obtained the same result for g2=1 and g1=1,0134 which represents 1,34% of the unmatched gain.

For a centered beam, V1=V2, so:

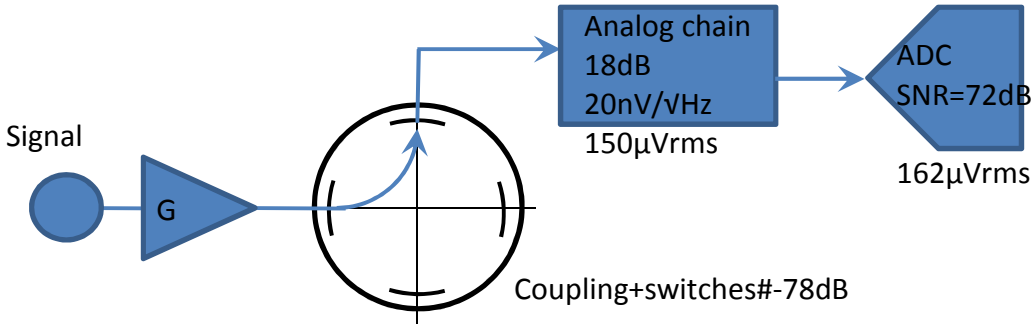
$$X = \frac{R}{2}\frac{\Delta}{\Sigma} = \frac{R}{2}\left(\frac{g1 - g2}{g1 + g2}\right)$$

We can see that X depends on the gains difference.
In conclusion, gains should be calibrated for a sum of their shift higher to ***1,34%***.
The second conclusion is that gains should be calibrated with a better S/N ratio acquisition than 0,67% which corresponds to the worst case, so ***S/N=150#44dB***.

Gains variations result from the variation of several parts in the acquisition chain: filters, amplifiers, ADC... The gain compensation will be possible as soon as the coupling is the same for the two opposed electrodes. Finally the difference between couplings should not exceed ***0,67%***. First tests showed that couplings were very close, even with the low analyzer acquisition dynamic range.
Tests have to be performed in the future in order to prove this calibration is reliable.

4-3 Transfer function measurement.

With a ~250ns pulse long, the typical acquisition window should be longer than 50ns because of the shaped "tail" signal. As we have to process a FFT, the number of samples has to be a power of two: with a 96e6MSPS ADC we should acquire ***2^7=128 points***, so a window about 1,33µs.
It corresponds to a ***64*** points FFT and so to a ***df=750KHz***. The deconvolution will need a transfer function with the same bandwidth and same df.
The transfer function can be obtained different ways: sweeping the frequencies with a sine generator, producing the tones at the same time, injecting white noise.
Whatever the excitation, we can represent the calibration scheme as follows:



We saw that transfer function points have to be measured with a ***44dB*** SNR. Because of the couplings and of the desired SNR, we will have to implement longer acquisitions than the typical ***128*** points for beam signals. The aim will be to reach the desired noise floor that allows to measure the transfer function. A long acquisition FFT allows a "processing gain" that decreases this noise floor.
Whatever the injected signal, we can calculate first the theoretical maximum processing gain of the ADC: we can imagine that it corresponds to the FFT processed with an infinite number of acquisitions, so df=0Hz. As with an analog chain, the ADC theoretical spectral density noise floor can be calculated as ***162µV/√(BW)***.
We can see that the processing gain will not be limited by the analog part because its noise is ***150µVrms***. With M the number of acquisition points, ADC will limit the processing gain to 10log(M/2)=20log(√48e6)=77dB. So ***Mmax=2^26***.
It corresponds to a -72-77=***149dB*** noise floor.
This represents a very long acquisition and the limitation should appear on the FFT calculation first (memory,…). The typical length of a window acquisition should be 2^13=***8192*** points for local memory and processing reasons.

4-3-1 Sweep sine:

The frequency should sweep with the same df than FFT, so every 750kHz.
With a +/-1V injected signal (ADC full scale as a reference), the FFT should have a ***78-18+44=104dB*** dynamic range.
The SNR of a the ADC is about ***72dB***, so the noise floor of the FFT should be ***104-72=32dB=10log(M/2)*** with M the number of points in the FFT process.
M#3170 but M should be a power of 2 so ***M=2^12=4096***, low comparing to the theoretical maximum processing gain.
Finally the acquisition of a point of the transfer function should take 4096 samples, so 4096*1/96e6=***42µs***.
The total 64 points of the transfer function can be performed in ***64x42µs#2,7ms***.

With a larger signal, the length of the acquisition will reduce.
I.e. with a +/-5V sine, the gain on SNR is about ***14dB***. It represents now a processing gain of 32-14=18=10log(M/2), so ***Mmin =128***. It corresponds to the typical signal window acquisition.
The full 64 points transfer function could be performed in a total time of ***64x128x1/96e6#85µs***. We can imagine that with a 50Hz rate machine, the calibration could be performed as a systematic routine between each beam pulses.
This method has drawbacks:

- The sweep has to be completed to reconstruct a beam shape. Degraded but faster reconstructions need alternative calibration process.
- The sine generation needs to implement a synchronous system with a high speed DAC (96MHz), even the needed SNR is not very important (44dB=7ENOB).
- The sweeping method needs the implementation of a complex sequential software.

4-3-2 Random noise:

An alternative to a sweep sine could be a white noise excitation on the desired bandwidth. The advantage of this method should be the simplicity of the signal generation and of the calibration software. A digital random noise can be produced by a FPGA. The longer the acquisition and its associated FFT will be, the more precisely the transfer function will be measured. The drawback is that the longer the acquisition will be, the smaller the df will be. So the noise power will be spread on a larger number of frequencies.
With a +/-1V square random noise (ADC full scale as a reference): it corresponds to a ***1Vrms*** noise. On the acquisition bandwidth, 48MHz, it corresponds to a density spectrum noise floor about 20log(48.e6^0,5)=***-77dB*** under the 72dB SNR.

Finally, we should have to reduce the power spectrum acquisition SNR to 77+44+60=***-181dBFS***.
With the 72dB ADC SNR, it corresponds to a processing gain about 181-72=***109dB***. We calculated that the theoretical maximum processing gain is about 77dB so the calibration with 1Vrms noise is impossible.

Remark: the use of a gaussian noise should give the same results but needs larger signal amplitude. The solution should be to gain 181-149=32dB on the signal injection. That means a +/-40V random noise, which is here impossible.
Even if this generator was feasible, or changing the ADC for a perfect one and with a system allowing FFT calculation of 2^40 points, the calibration should represent a total time close to minimum 47min.

4-3-3 Dirac comb/tones comb:

Another alternative to a sweep sine can be a comb of the 64 needed frequencies. We could perform it using a Dirac comb or a sum of all the sine tones. An advantage of this technique is to allow the combination of several FFT windows.

- *Dirac comb*:
  A df=750kHz frequency comb can be produced by a time comb with Dirac impulsions every dT=750kHz=1,33µS, so ***128*** acquisition points. So with a 128 points FFT and ***A*** the amplitude of the Dirac pulse, the comb amplitude in the frequency domain (64 points) is ***A/64*** so a ***-36dB*** reduction. So for a 2V Dirac pulse (ADC full scale as a reference), we should perform a -60-36-44=***-140dB*** noise floor. So the processing gain should be about 140-72=***68dB***. The theoretical maximum has been calculated to ***77dB***.
  68=10log(M/2), ***Mmin=2^23***. As the typical length of an acquisition is **2^13=8192** points, the FFT should be performed by the combination of ***2^10*** windows for a total acquisition time about ***87ms***.
  This solution looks attractive because of the simplicity of the system and of the software. The Dirac pulse could be performed by an amplified FPGA output but the system has to be able to process a final ***2^23*** points FFT.

- *Tones comb*:
  With the use of a DAC we can perform the 64 tones simultaneously and so simplify the calibration software comparing to sweep sine solution.
  The sum of these 64 sine signals with the same amplitude ***A*** corresponds to a signal with a maximum amplitude about ***40xA*** so a difference of ***32dB***.
  It means that a +/-1V DAC will allow to generate 64 tones about +/-25mV.

With a +/-1V DAC, so +/-25mV tone excitation, FFT processing gain has to perform a noise floor about ***-60-32-44=-136dB***. So with a 72dB SNR, 10log(M/2)=136-72=64dB. It corresponds to Mmin=2^23. The result is the same than with the Dirac comb. It should be easy to amplify this signal by a factor 5 to obtain a +/-5V excitation.
In this case, the processing gain is 64-14=50dB, which corresponds to M***min=2^18***. With 2^13 points windows, it corresponds to a total of 2^5=***32*** windows and a total time of ***2,7ms***. We can notice this result is the same than for the +/-1V sweep sine method.

Conclusion:
the transfer function measurement should be impossible with a white noise generator. The implementation of a DAC and an amplification (typically g=5) seems to be mandatory and will allow to tests the different techniques. A comb technique will allow to simplify the software routine in front of a sweep sine technique. This calibration should be systematic in the acquisition cycle. For instance a 2^13 points window could be acquired before or after each beam acquisition and so the transfer function should be permanently recalculated.

5- Conclusions and perspectives.

The study of this first prototype of BPM stripline has shown that a simple base band electronics is theoretically well adapted according to the CLIC drive beam specifications. The choice of the BPM is not definitive and the instrument should evolve in the future. The most problematic part of the project looks to be the transfer function and calibration because of the lack of single bunch configuration.
Whatever the technique that will be used, the tests in TBL should allow to qualify the read-out electronics: analog preamplification, acquisition and synchronous optical network. Collaboration with CERN's divisions should also allow the definition of a global and reliable architecture.

References:

[1] Study of the CLIC module front-end acquisition and evaluation electronics: http://hal.in2p3.fr/in2p3-00666173

[2] CLIC Conceptual Design Report: http://project-clic-cdr.web.cern.ch/project-clic-cdr/