The SAMPIC Waveform and Time to Digital Converter

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***Abstract*– SAMPIC is a Waveform and Time to Digital Converter (WTDC) multichannel chip. Each of its 16 channels associates a DLL-based TDC providing a raw time with an ultra-fast analog memory allowing fine timing extraction as well as other parameters of the pulse. Each channel also integrates a discriminator that can trigger itself independently or participate to a more complex trigger. After triggering, analog data is digitized by an on-chip ADC and only that corresponding to a region of interest is sent serially to the DAQ. The association of the raw and fine timings permits achieving timing resolutions of a few ps rms. The paper describes the detailed SAMPIC0 architecture and reports its main measured performances.**

Index Terms— Analog-digital conversion, Time measurement, Delay lock loop, Mixed analog-digital integrated circuits, Front-end electronics, CMOS.

I. Introduction

Time stamping with picosecond accuracy is an emerging technique opening new fields for particle physics instrumentation. For example, it permits the localization of vertices with a few mm precision, thus helping associating particles coming from a common primary interaction even in a high background, or it can be used for particle identification using Time of Flight techniques. It has recently been demonstrated that ps timing accuracy can be reached by sampling the detector signal with ultra-fast digitizers and extracting time information by interpolation of the samples located in the leading edge of the signal [1]-[3]. Moreover, the knowledge of the signal waveform permits extracting other useful parameters like charge, pulse width or rise-time and optimizing the timing extraction algorithm during or even after data taking.

II. Introducing the notion of waveform TDC

Standard fast waveform digitizers as well as oscilloscopes are usually based on standard ADCs, often interleaved in order to virtually increase their sampling frequency. But high timing precision implies high sampling rate above 1GS/s that generates a huge local data rate at the output of the ADC (>> 10 Gbits/s). This makes the associated digital electronics expensive and power consuming so that this kind of solution is not usable for medium or large scale experiments.

Modern ultrafast analog memories using Switched Capacitor Arrays (SCA) nicely solve this problem [2]-[7] especially in terms of power, space and money budgets but their readout deadtime (~ 2 to 100 µs) may be a limitation. Moreover they require extra electronics to be used as timing systems.

In recent systems, TDCs, either embedded in high-end FPGAs or ASICs, are usually used for time measurement. Here, the information is concentrated into a simple digital integer value, thus reducing drastically the dataflow, which is good for large scale measurement. But TDCs do not provide information on waveform, except under the form of Time Over Threshold (TOT) for those able to measure both edges of the signal. Anyhow, in this case, the precision on the amplitude or charge of the signal remains poor.

The most advanced TDCs are based on the association of a coarse time counter running on the main clock and of Delay Line Loops (DLLs) interpolating the latter. The DLLs can be smartly interleaved in order to improve the resolution. Resolution is given by the DLL step but it is usually limited by stability of calibration or environmental effects. Actually, the weak point of the TDC is to have only a digital input, which means that, as shown in Fig. 1, it requires an extra discriminator to transform the analog signal into digital.

This discriminator introduces additional jitter and always suffers from residual time walk – which is the dependency of timing with signal amplitude – even in its most advanced implementation (CFD), or after correction using the TOT information. Thus the overall timing resolution is degraded to the quadratic sum of the discriminator and TDC respective timing resolutions, usually above 25 ps RMS. Moreover, the power consumption of the discriminator necessary to reach good timing performance is usually high.

To overcome all these limitations, we are introducing here the new concept of Waveform TDC, shown in Fig. 1.

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* corresponding author; eric.delagnes@cea.fr
[1] CEA/IRFU, Centre de Saclay, 91191 Saclay, France.
[2] Laboratoire de L'accélérateur Linéaire from CNRS/IN2P3, Centre scientifique d'Orsay, Bâtiment 200, 91898 Orsay Cedex, France.
[3] Now with SCICPP, Santa Cruz (USA)

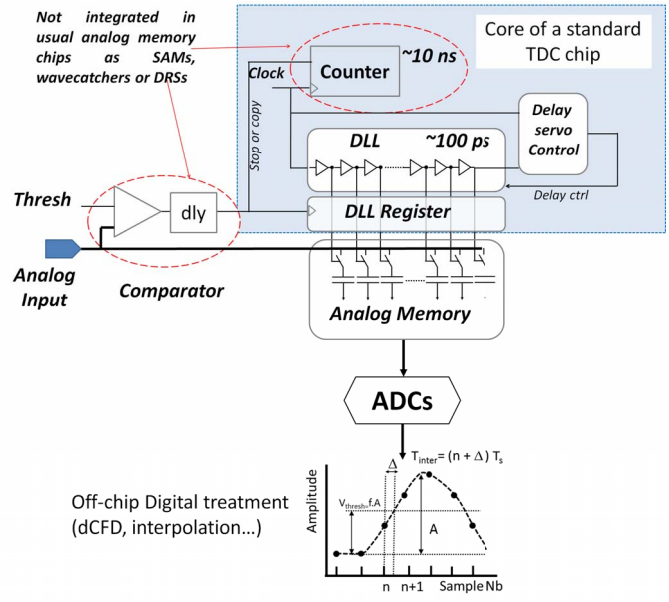

Fig. 1: the usual implementation of a pure TDC.

An analog memory is added in parallel with the delay line. It samples the input signal which can now be analog and permits performing an interpolation of the samples recorded on the latter. The discriminator is not anymore in the critical timing path. Time information is given by association of three contributions:

- Coarse = Timestamp gray-code Counter (few ns step)
- Medium = DLL locked on the clock to define region of interest (100 ps minimum step)
- Fine = samples of the waveform (interpolation will give a precision of a few ps RMS)

The time resolution can reach a few ps rms, even on small analog signals. Moreover, digitized waveform shape, charge and amplitude are available.

III. THE SAMPIC PROJECT

The SAMPIC project is a R&D project initially intended to develop a common WTDC prototype addressing the need for high precision timing (5 ps RMS) required by ATLAS AFP and SuperB FTOF. Its natural targets are indeed all the new fast detectors for Time Of Flight (TOF), particle identification, pile-up rejection (ATLAS AFP…), TOF-PET, based on MCP-PMTs, diamonds, APDs, SiPMs, and their associated characterization test benches.

The goals for the first prototype were the following ones:

- Design of a new ASIC called SamPic0 for the validation of the Waveform TDC structure.
- Evaluation of AMS 0.18µm CMOS technology for mixed design.
- Design of a system where the multichannel chip is already usable in a real environment, which means connected to detector with a real readout and DAQ system.

SamPic0 was designed to be the core of a future "dead-time free" or more complex chips.

IV. THE SAMPIC0 ASIC

A. Generalities and principle

SamPic0 is a 16-channel ASIC. Its inputs directly receive the (externally amplified) analog signal coming from the detector, via an AC-coupling located on the board. The main elements of the chip architecture, depicted in Fig. 2, are listed below:

- 16 single-ended channels, each equipped with a discriminator with programmable threshold, independent and self-triggered (OR with Central OR Trigger or External Trigger);
- 64 analog switched-capacitor-based sampling cells per channel;
- One 11-bit ADC per cell, which corresponds to a total of 64 x 16 = 1024 on-chip ADCs;
- One common 12-bit gray-code counter (running up to 160 MHz) for coarse time stamping;
- One common 64-step DLL, servo-controlled to the clock period of the aforementioned gray-code counter, running between 1 and 10 GS/s, for medium precision timing & providing the signal required for analog sampling;
- One other common 11-bit gray-code counter running @ 1.3GHz, used for the massively parallel Wilkinson ADCs;
- One 12-bit LVDS readout bus (potentially running up to 400 MHz);
- A SPI Link for internal registers configuration.

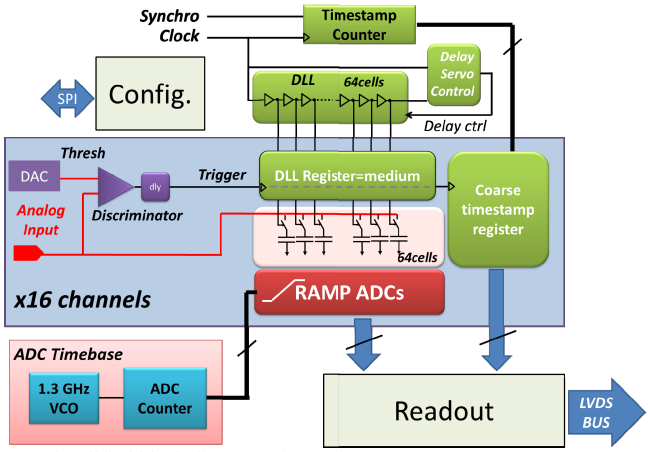

Fig. 2: Simplified block diagram of SamPic0.

The time tagging sequence for a given channel is the following. When the discriminator output fires, it:

- catches the state of the counter output: coarse timestamp (down to 6.4 ns steps)
- catches the state of the DLL, giving a medium precision (down to 100 ps steps)
- stops the waveform sampling which will give the few ps time precision after interpolation between the analog samples.

Fig. 3 shows the layout and the implementation of the chip on its board. Its main characteristics are:

- Technology: AMS CMOS 0.18µm;
- Size: 7 mm^2;
- Package: 128-pin QFP, pitch of 0.4mm.

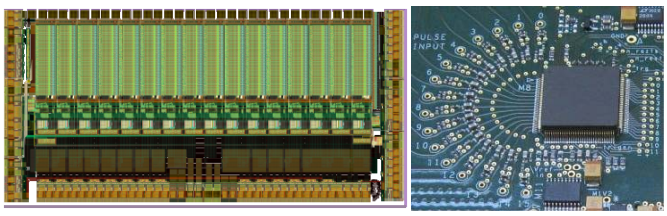

Fig. 3. Left: layout of SamPic0. Chip is rotated of 90° clockwise wrt block diagram of Fig. 2. Right: the chip mounted on its board.

B. SAMPIC triggering options

Each channel is equipped with one signal discriminator and one 10-bit DAC for each discriminator threshold (which can also be external).

As shown in Fig. 4, several trigger modes are programmable individually for each channel: local, external, "central" trigger (only OR in this chip). Discriminator edge can be selected. Channels can be disabled. Three option are available for post-trigger delay (0, 1, 2 delays of ~1ns).

A common deadtime optional operation using a Fast Global Enable input is also available.

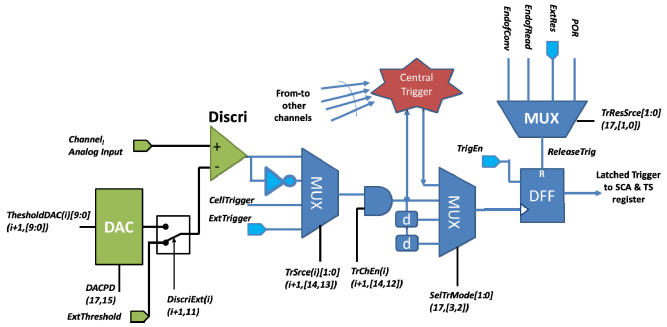

Fig. 4: triggering options of SamPic0.

When a trigger occurs:

- sampling in the analog memory is stopped and coarse timestamp is latched;
- the trigger position is recorded in the analog memory;
- the chip rises a first flag for the user (FPGA) to start the ADC conversion and once done with the latter a second flag to ask for data readout.

C. DLL and sampling memory

The chip houses a single 64-step long Delay Line Loop locked on the Timestamp (TS) counter clock, thanks to an on-chip servo-control (phase detector + charge pump), as shown in Fig. 5. It provides 64 incrementally delayed pulses with constant width used to drive the Track & Hold (T/H) switches of the 64 cells for all SCA channels. It provides the 'virtual multiplication' by 64 of the TS clock (for instance a 6.4 GSPS sampling rate will be obtained from a 100 MHz TS clock).

T/H signals can be disabled independently on each channel (to stop the sampling). An option allowing speed mode for sampling below 3 GS/s is also available

A special care has been taken in ensuring a perfect continuity between last & first cells of the DLL.

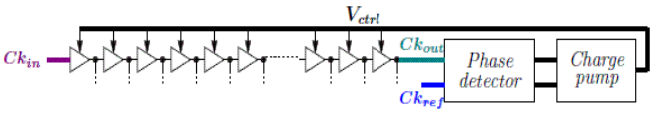

Fig. 5: the main DLL of SamPic0.

The chip has no analog input buffer, and the signal is unipolar. The memory cell is based on the 3-switch structure shown in Fig. 6, minimizing the effects of leakages and ghost pulses (memory persistence). Switch 3 also isolates from input bus during conversion. For these purposes:

- switches 1 and 2 are closed while 3 is open during tracking;
- to sample, switches 1 and 2 are released. Switch 3 is then closed to set the potential to the node between switches 1 and 2. The cell is then in hold mode;
- During few ns before coming back in track mode, switch 2 is closed, then resetting the storage capacitance.

The storage cell capacitance, including parasitic elements , is 35 fF. This values allows a compact design, 1.5 GHz bandwidth and theoretical kTC noise small enough (340 µV RMS) for a 11-bit range operation.

The length of 64 cells is a trade-off for:

- Time precision and stability requiring a short DLL;
- Input capacitance requiring a short DLL;
- Time for trigger latency requiring a long DLL.

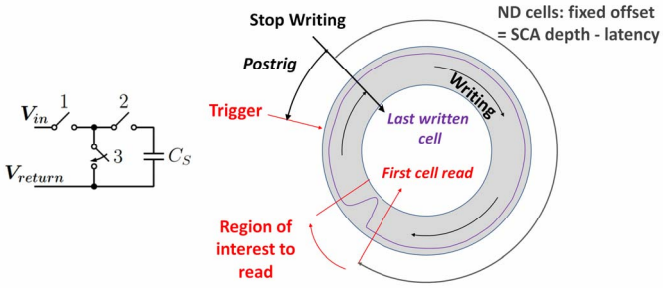

Fig. 6: Left: the 3-switch memory cell of SamPic0. Right: recording stops after trigger in order to perform readout and analog to digital conversion. Readout can target a region of interest, which can be only a subset of the whole channel.

The chip has been designed to offer a signal bandwidth of 1.5 GHz and a usable dynamic range close to 1 V. A special design has been studied in order to ensure a good quality (constant bandwidth and constant tracking duration) over all the 64 samples (even those located after trigger).

Analog memory is a circular buffer so it is continuously writing until triggering, the oldest cells being overwritten after one turn. As mentioned previously, when trigger occurs (optionally after a "postrig" delay), the sampling is stopped and the position of the write pointer is tagged in the analog memory. This information is used for medium precision timing but also as a basis for the optional Region of Interest (RoI) mode of readout (only few cells read starting from a

programmable offset from the trigger) for minimizing the readout deadtime.

D. Analog to Digital conversion

The schematic principle of the analog to digital conversion is shown in Fig. 7.

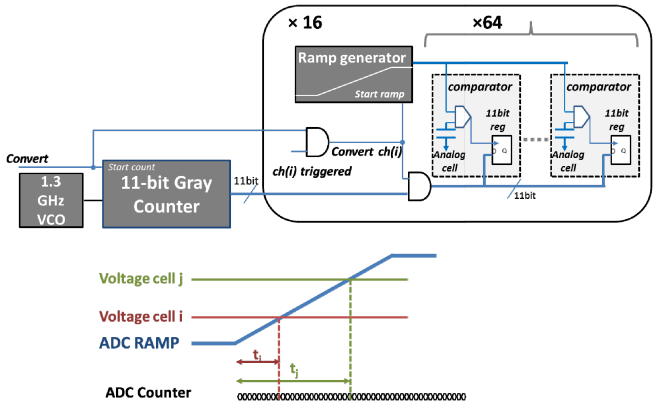

Fig. 7: schematic principle of the ramp analog to digital conversion.

At a given time, all the cells of the channels already triggered will be converted simultaneously. The sequence is the following:

- Start the on-chip 1.3 GHz Voltage Controlled Oscillator
- Enable the 64 ADC comparators of the enabled channel
- Start the on-chip 1.3 GHz gray-code counter whose outputs are sent to the channels to convert
- Simultaneously start the ramp generators of channels to convert: the slope is tunable (speed/precision tradeoff)

Conversion time depends on the number of bits chosen for its precision: 1.6 µs for 11bits, 800ns for 8 bits, and 400 ns for 9 bits … This is actually the main contribution to the input dead time. When the ramp crosses the voltage stored in the cell, the corresponding counter value is stored in a register. Once converted, a channel is immediately usable for recording a new event.

E. Readout philosophy

Readout is driven by Read and RCk signals (see Fig. 8).

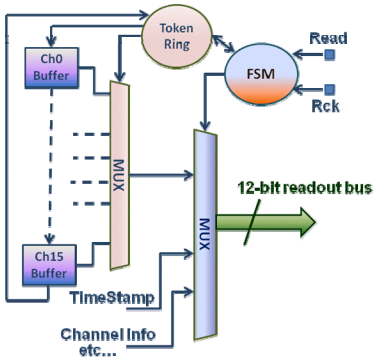

Fig. 8: schematic principle of the readout stages.

Data is read channel by channel, with a rotating priority mechanism to avoid reading always the same channel. As evoked above, an optional RoI readout is available to reduce the dead time (the number of cells read can be chosen dynamically). Event data is transmitted via a 12-bit parallel LVDS bus, including:

- Channel Identifier, Timestamps, Trigger Cell Index;
- The value of the converted cells (all or a selected set) of a given channel, sent sequentially.

This bus, whose standard speed of 1.92 Gbits/s (160 MWords/s), can potentially run up to 4.8 Gbits/s (400 MWords/s). It is worthwhile to notice that a channel is not in deadtime during readout, only during conversion (data register is really a buffer stage).

V. ACQUISITION MODULE AND SOFTWARE

In parallel to the chip design, we developed a complete electronics module for SamPic0 (see Fig. 9).

Fig. 9: SAMPIC acquisition module (left) and mezzanine (right).

The chip is mounted on a mezzanine board which thus houses 16 channels, also shown in Fig. 9, itself mounted on a mother board which can hold 2 mezzanines: we thus designed a native 32-channel module. Input connectors are of MCX type. The module is packaged in an autonomous metallic box (see Fig. 6) and makes use of an external compact AC/DC switching adaptor power supply. The module provides a USB and UDP interfaces. Optical links are implemented, but not yet active. Power consumption on the + 5 V is of 1.5 A for 32 channels.

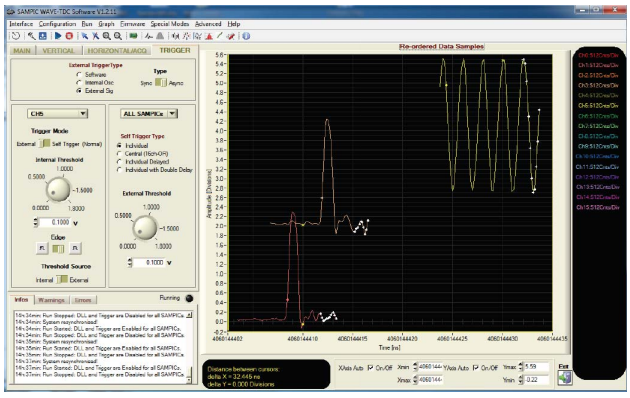

Fig. 10: the SAMPIC acquisition software in WTDC display mode.

We have also developed a graphical acquisition software which permits the full characterization of the chip and module. It is also already usable for small size experiments. It offers a special visualization for innovative WTDC mode. The latter permits visualizing the individual pieces of waveforms at their exact time location with respect to each other. This

functionality is illustrated by the snapshot of Fig. 10 on which the 3 waveforms plotted have different time origins.

Many configuration menus and panels are available, which offers a great flexibility for all types of measurements. A panel fully dedicated to time measurement permits realizing real time histograms of time difference between any pair of channels.

VI. CURRENT TEST STATUS

The chip behaves nearly as specified with only two identified problems:

- RoI readout: fails in some cases. Therefore we always read the whole depth of the SCAs for the measurements reported here;
- Central trigger which is not working correctly.

These 2 features are not absolutely necessary, their cause are identified, and have been corrected in a second version of the chip currently being processed.

The chip is usable as it is. Waveform sampling is ok:

- From 1.6 to 8.2 GS/s on all the channels;
- Up to 10.2 GS/s on 8 channels;
- Not yet thoroughly tested under 3 GS/s.

Readout works well between 50 and 175 MHz (>2 Gbits/s). We still need to test it at higher frequencies.

There is no evidence of cell leakage. Data is not damaged, even for storage times of few tens of µs.

VII. MEASUREMENTS AND CALIBRATION

A. *Calibration philosophy*

Characterization of this kind of circuit can lead to many different types of calibrations. Our goal always is to find the set with the best performance/complexity ratio, but also to find the right set for the highest level of performance.

SAMPIC actually offers very good performance with a reduced set of calibrations:

- Amplitude: cell pedestal and gain (linear or parabolic fit);
- Timing non uniformity, also known as time INL, (one offset per cell).

This leads to a limited volume of standard calibration data (6 Bytes per cell and per sampling frequency which corresponds to 8 kBytes per chip and per sampling frequency). It can thus easily be stored in the on-board EEPROM.

These simple corrections could even be applied in the FPGA.

B. *Power consumption*

The global power consumption of SamPic0 is less than 200 mW. Moreover, it depends for an important part of the choice of the current used by the LVDS output drivers, as shown in Fig. 11 (yellow vs orange sectors). The two other main contributors are the parts linked to the high frequency digital activity: the DLL and its buffers, and the sampling logics. Using the low current mode which works perfectly, the total consumption is of 150 mW, i-e less than 10mW per channel.

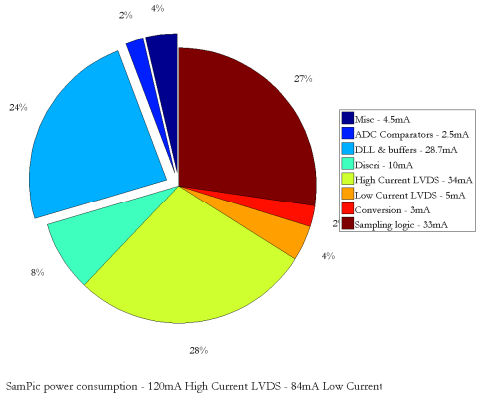

Fig. 11: distribution of SamPic0 power consumption.

C. *Noise.*

The massively parallel Wilkinson ADCs work well using a 1.3 GHz clock, which permits the conversion over 11 bits in 1.6 µs. Still in 11-bit mode, the ADC count (LSB) corresponds to 0.5 mV. As the voltage range is of 1 V, we get a dynamic range of ~ 10 bits rms.

The raw cell to cell pedestal spread is of ~ 5 mV RMS. After calibration and correction of this spread, the average noise is 0.95 mV RMS, with the noisiest cells at 1.2 mV RMS. There is no geometrical effect in the noise map of Fig. 11, which means that noise distribution is merely random. This does not change with sampling frequency.

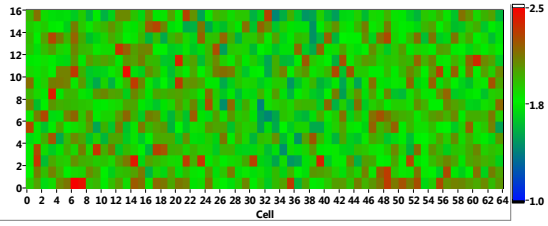

Fig. 12: noise map @6.4 GS/s. Baseline ~ 1100 ADC counts, 11-bit mode, soft trigger, FPN subtracted. 1st and 12 last cells of each acquisition removed. Average noise = 1.9 ADC count.

We also tested the conversion in 9-bit mode, thus with a LSB of 2 mV: there is only 15% of noise increase.

D. *ADC calibration and performance*

DC sweep of the channels input voltage is performed thanks to the possibility of fixing the baseline DC level via a DAC on the board. It permits DC transfer functions measurement of all the cells of all the channels of the chip as illustrated by the left plot of Fig.13.

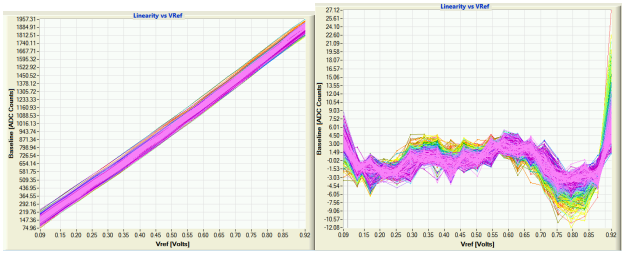

Fig. 13. Left: ADC linearity calibration plot for all the cells from all the channels of a SAMPIC chip. Right: residues to a 2nd degree polynomial fit of the data from the left plot.

The cell-to-cell spread of slopes is of the order or 1% rms with a random distribution (not related to channel). Peak to peak integral non-linearity is of 3%. Both effects are systematic and due to charge injection by switches. They can be easily corrected after calibration. For this purpose, from the same measurements, an individual cell fit is performed which can be either a linear fit or a 2nd degree polynomial one, which parameters are used automatically by the software to correct data during or after acquisition. The residues for a 2nd degree polynomial fits of the transfer functions from the left plot is shown on the right are plotted on Fig. 13.

Without any linearity or gain spread correction, resolution would be degraded to ~7-8 bits RMS that can be acceptable for most timing applications.

E. *Discriminator*

As the SAMPIC chip is mainly designed to operate in self trigger, it is important to characterize its triggering chain. For this purpose, a 3.1 kHz repetition rate, 150 mV amplitude, 1ns wide positive pulses are sent to the input of one channel which baseline is fixed to 390 mV.

The detected rate is plotted as a function of the discriminator threshold set by the internal DAC or externally in Fig. 14.

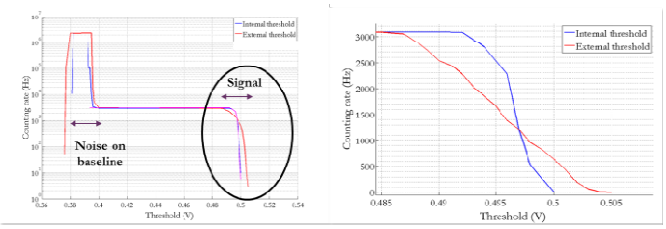

Fig. 14: detected hit rate as a function of the threshold for 150 mV, 1ns wide pulses with 3.1 kHz pulses. The baseline was set to 390 mV. Left: threshold sweep up to 500 mV with the rate in logarithmic scale. Right: Zoom on the region of the signal.

On the left plot of this figure, in logarithmic scale, we can see that the rate first increases then decreases for thresholds corresponding to the baseline, before reaching the 3.1 kHz rate of the signal. On this plot, we can see it is possible to self-trigger reliably for threshold ~10 mV above the baseline. After a plateau, the rate decreases for thresholds corresponding to the signal amplitude, as seen by the discriminator. For the very fast pulse used, because of the limited bandwidth of the discriminator, the threshold corresponding to a 150mV pulse is only of 100 mV. This region of the plot is zoomed, using a linear scale, on the right plot of Fig. 13. It is actually the standard S-curve usually used to characterize discriminators. By fitting this characteristic using an erfc function, we can extract a discriminator noise of 2 mV RMS if the threshold is set internally, increased to 8 mV RMS if the threshold is set externally. The reason for this higher noise for external threshold is still being investigated, but the nominal operation of the chip is with internal threshold. We can notice that the 2 mV RMS noise measured for the discriminator is consistent with the minimum detection level of 10 mV measured on the first part of the plot.

F. *Bandwidth and signal quality*

Signal quality is highlighted by the 64 samples taken on the 350 MHz sinewave (0.5 V peak-peak) shown in Fig. 15. This is a 'out of the box' single shot recorded @ 6.4 GS/s, with the sole ADC linearity correction.

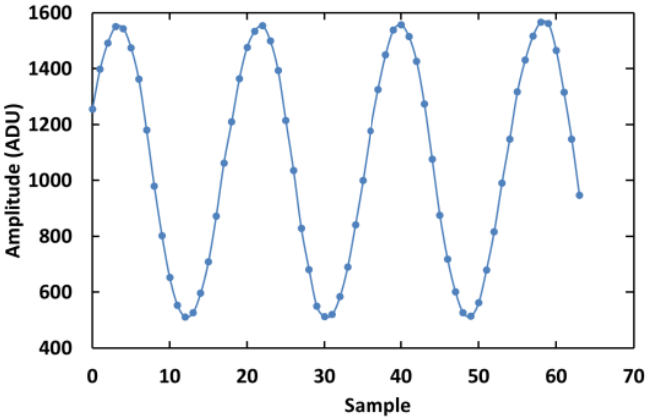

Fig. 15: raw 350 MHz sinewave sampled at 6.4 GS/s.

As one can notice, all of the 64 data points are usable, and the signal already looks very good.

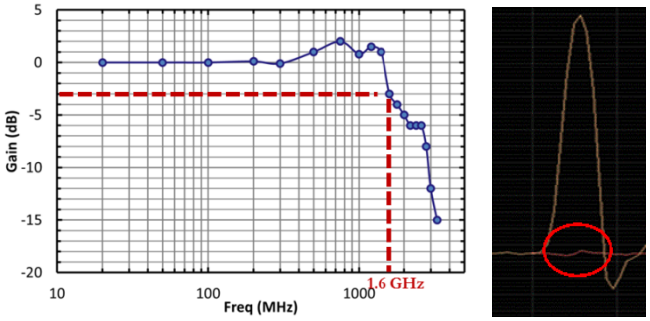

Fig. 16. Left: Frequency response of SAMPIC. Left: crosstalk between 2 channels (smaller than 1%).

Fig. 16 shows the frequency response of the chip measured with sinewaves similar to the one of Fig. 15. The -3dB bandwidth is in the order of 1.6 GHz, close from our expectations. It is constant all over the 64 cells of the analog memory. Ringing effects are probably due to problem of impedance matching at the board input.

The right plot of Fig. 16 shows that the crosstalk between channels is smaller than ±1%.

VIII. TIME PERFORMANCES

A. *Time resolution*

In order to estimate the resolution of the time measurement, we use a high-end generator, providing after splitting, 2 pulses with 2.5 ns distance, 300 ps risetime, 1 ns FWHM, 800 mV peak, sent on 2 channels of a SamPic0 chip. The 2 pulses, shown in Fig. 17, are recorded in self-trigger mode at 6.4

GS/s, 11-bit mode, but the measured timing performance remain unchanged for sampling frequencies up to 10 GS/s.

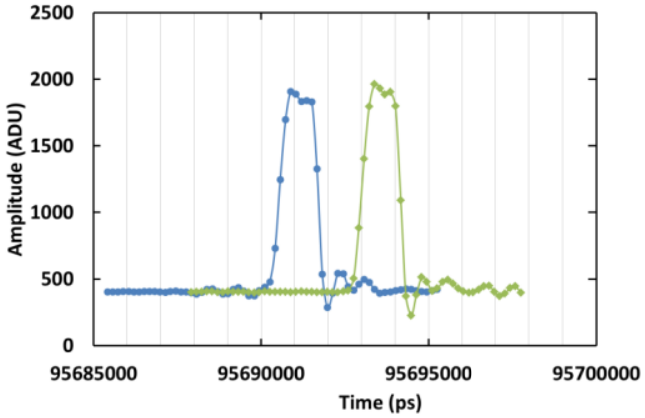

Fig. 17: the two pulses recorded at 6.4 GS/s (160 ps / sample) used for timing measurements as recorded by SamPic0.

After non-linearity and pedestal common correction, the timing for each pulse is calculated online using a digital CFD algorithm and interpolation as described in [8] or [9].

The time differences distributions measured in these conditions are shown in Fig. 18. Without any time correction, we already get 18 ps RMS for Time Difference Resolution (TDR), which is already at the level of the best (calibrated and corrected) TDC and sufficient for a lot of applications.

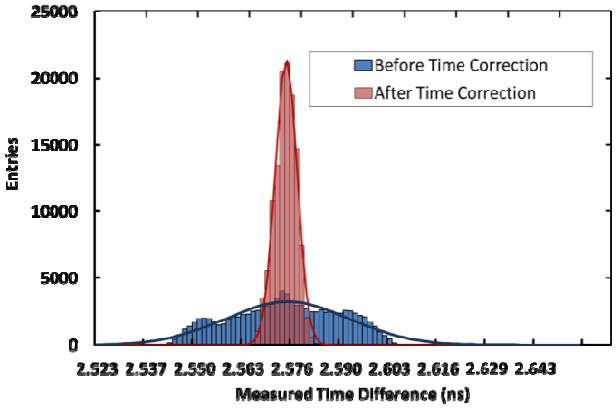

Fig. 18. Left: Δt timing distribution without any timing correction ~ 18 ps rms. Right: Δt timing distribution after TINL correction ~ 3.5 ps rms.

We know from previous work that this non-Gaussian distribution is mainly due to the spread of the delays (also called Time integral non-linearity or TINL) in the DLL and that it can be easily calibrated and reliably corrected. For this purpose, we have used the method described in [8] using the amplitude of segment of sinewaves crossing the origins that permits a very fast calibration procedure.

Once the TINL correction is simply applied, the TDR becomes as good as 3.6 ps RMS. Looking at the plots, on which all events are plotted, one can notice that there is neither tail in the distributions, nor hit "out of time" due to metastabilities, also no problem of boundaries between ranges validating then the "three ranges" architecture of SAMPIC.

B. Time measurement as a function of the delay and the rate

The dependency of the TDR on the delay has been studied using two setups. To generate small delays we introduce a cable between the splitter and one of the SAMPIC's input. For larger cable delays, this method is no more usable, as the amplitude of the delayed signal diminishes and its risetime increases, both effect affecting the TDR as shown later in VIII.C. However, as shown in Fig. 19, the latter increases from 2.7 ps RMS to 4.5 ps RMS for delays up to 10 ns. After this value, the TDR remains flat.

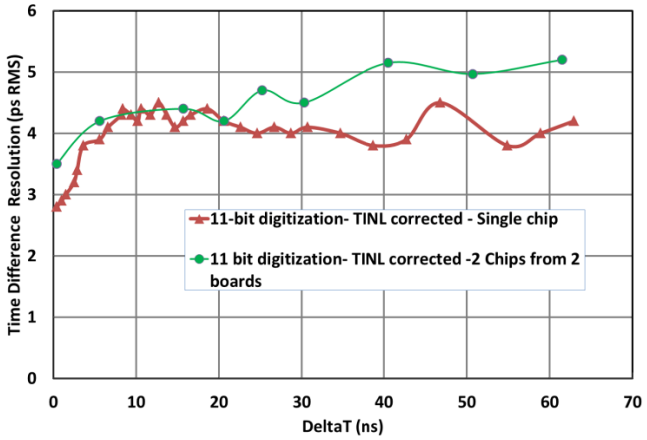

Fig. 19: time difference resolution vs delay made by cables.

The shape of this characteristic can be explained if we keep on mind that at 6.4 GS/s the total DLL duration is of 10ns. For a delay of 0 ns, the two pulses are recorded during the same DLL cycle. For delays larger than 10 ns, they are captured during different DLL cycles, so that the jitters from the clock and the phase comparator are now added. For intermediate values the probability to record the two pulses within two different DLL cycles is proportional to the delay explaining consequently the progressive increase of the resolution.

As shown in Fig. 19, similar results are obtained using two SAMPIC chips from different mezzanines. In this case, as the two chips don't share the same DLL, the timing measurements on the two pulses are uncorrelated so that we can claim that the single pulse resolution is better than 3.2 ps RMS (4.5/√2) after TINL correction. For the measurements using two chips, we can notice a slight increase of the TDR for the largest delays. This tiny effect was only noticed for larger delays (not shown here) when using a simple chip. The different behaviour is mainly related to the different setup used for the two-chip measurements (slower generator providing 0.8-ns risetime, 2-ns FWHM pulses, and different cables, which reduces the signal slope and thus introduces extra jitter due to electronics noise as shown on Fig 22).

As shown in Fig. 20, the input rate does not affect the quality of the timing measurement, event for rates of few MHz.

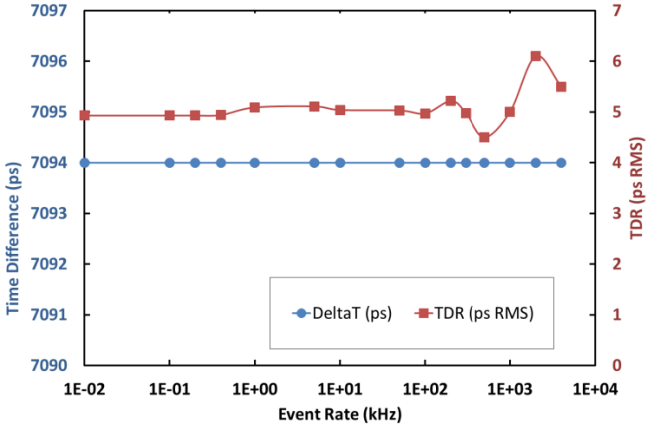

Fig. 20: measured time difference and TDR vs input hit rate (1 ns FWHM, 400 ps risetime, 700 mV amplitude, and 7.1 ns delay pulses.

For larger delays we repeat the test using signals provided by two channels of a Tektronix AFG 3252 [10] Arbitrary Waveform Generator (AWG). The 800 mV, 2.5-ns risetime, 4-ns FWHM, test pulses are slower than the previous ones but can be delayed digitally up to 10 µs. As shown in Fig. 21, the measured TDR is constant and better than 10 ps RMS over the whole measurement range. This corresponds to 1 ppm of the full range and is far better than the 100 ps jitter specified for the AWG. Moreover, on the whole 10 µs delay range the difference between the programmed and measured delays is within +/-15 ps (+/- 1.5 ppm), better than the precision specified for the AWG and showing a structure probably due to the AWG internal design.

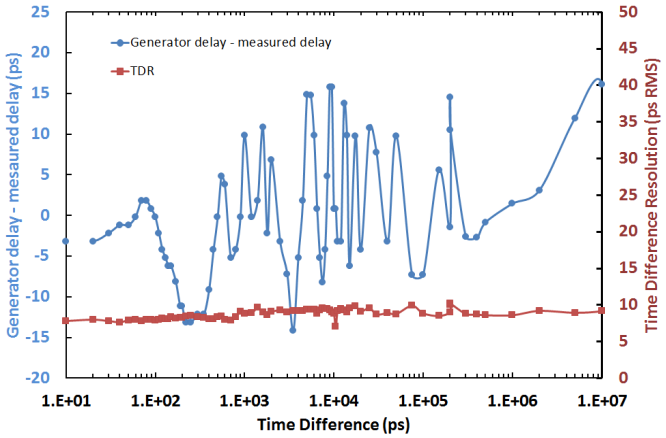

Fig. 21: Difference between the time measured using SAMPIC and the one programmed on the AWG and TDR as a function of the time difference for long delays.

C. *Timing Precision as a function of the amplitude*

The TDR variation as function of the pulse amplitude and risetime is plotted in Fig. 22. For this measurement, a 2 ns-FWHM pulse is attenuated before being split towards two SAMPIC channels. Two kinds of attenuator, with different bandwidths have been used providing pulses with risetimes of respectively 500 and 800 ps. The measurements (symbols) are within very good agreement with the theoretical expectation (lines) given by (1) which is the quadratic sum of a constant term (sampling jitter) with a contribution proportional to the signal risetime divided by its signal over noise [11].

$$\sigma(\Delta t) = \sqrt{2} \times \sqrt{{\sigma_j}^2 + \alpha \times \left(\frac{\sigma_n}{Slope}\right)^2} \qquad (1)$$

assuming:

- α =2/3 (case of the perfect CFD);
- slope is the local value of dV/dt of the signal;
- Voltage noise σ_n = 1.1 mV RMS, consistent with the previous measurement;
- Sampling jitter σ_j = 2.8 ps RMS, this number requires further investigations.

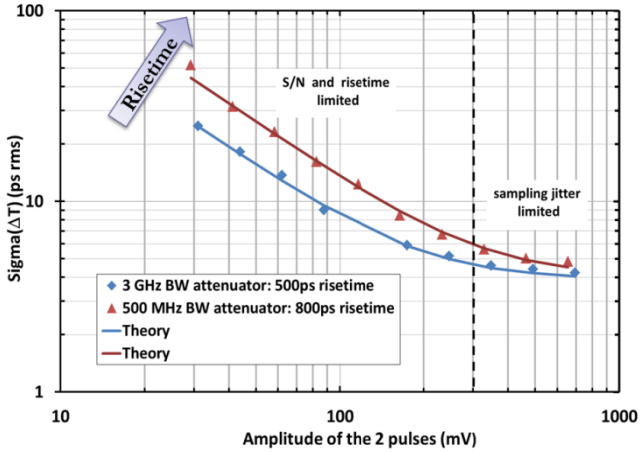

Fig. 22: Variation of TDR with the amplitude of the pulses for two different risetimes. The symbols are for measurements, the lines are corresponding to a fit using the quadratic sum model.

For both attenuators, the measured TDR is better than 15 ps RMS for amplitudes larger than 100mV and with the faster one a TDR better than 20 ps RMS is already reached for pulses as small as 40 mV.

IX. Summary of Performances

Table I: Main features and measured performance of SAMPIC0

Parameter	Value	Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption	180 (1.8V supply)	mW
Discriminator noise	2	mV RMS
SCA depth	64	Cells
Sampling speed	<3-8.4 (10.2 for 8 channels only)	GSPS
Bandwidth	1.6	GHz
Range (unipolar)	~ 1	V
ADC resolution	8 to 11 (trade-off time/resolution)	bits
SCA noise	< 1	mV RMS
Dynamic range	> 10	bits RMS
Conversion time	0.2 (8 bits) - 1.6 (11 bits)	µs
Readout time (can be probably be /2)	25 + 6.2/sample	ns
Single Pulse Time precision before correction	<15	ps RMS
Single Pulse Time precision after time INL correction	<4	ps RMS

Table I summarizes the main features and performances of the SAMPIC0 chip.

X. Conclusion and Future Developments

We have developed a multi-channel scalable acquisition system (ASIC, boards, software) for picosecond time measurement using the new WTDC (Waveform Time to

Digital Converter) concept integrated in the new SAMPIC ASIC.

The module works with even better performance than expected:

- 1.6 GHz Bandwidth;
- Up to 10 GS/s;
- Low noise (trigger and acquisition);
- << 5ps rms single pulse timing resolution.

It already meets our initial requirements, and is already usable for tests with detectors. Further work is ongoing on:

- Readout (firmware + software) optimization;
- Fine characterization of this first prototype;
- Characterization with fast detectors;
- A second prototype submitted in December 2014 on which the bugs detected on SAMPIC0 have been fixed and few minor improvements performed.

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